EN25Q80A
8 Megabit Serial Flash Memory with 4Kbyte Uniform Sector

FEATURES

- Single power supply operation
- Full voltage range: 2.7-3.6 volt

- Serial Interface Architecture
- SPI Compatible: Mode 0 and Mode 3

- 8 M-bit Serial Flash
- 8 M-bit/1024 K-byte/4096 pages
- 256 bytes per programmable page

- Standard, Dual or Quad SPI
- Standard SPI: CLK, CS#, DI, DO, WP#
- Dual SPI: CLK, CS#, DQ_0, DQ_1, WP#
- Quad SPI: CLK, CS#, DQ_0, DQ_1, DQ_2, DQ_3

- High performance
- 100MHz clock rate for one data bit
- 80MHz clock rate for two data bits
- 80MHz clock rate for four data bits

- Low power consumption
- 12 mA typical active current
- 1 μA typical power down current

- Uniform Sector Architecture:
- 256 sectors of 4-Kbyte
- 16 blocks of 64-Kbyte
- Any sector or block can be erased individually

- Software and Hardware Write Protection:
- Write Protect all or portion of memory via software
- Enable/Disable protection with WP# pin

- High performance program/erase speed
- Page program time: 1.3ms typical
- Sector erase time: 90ms typical
- Block erase time 500ms typical
- Chip erase time: 8 seconds typical

- Lockable 256 byte OTP security sector

- Minimum 100K endurance cycle

- Package Options
- 8 pins SOP 150mil body width
- 8 pins VSOP 150mil body width
- 8 pins SOP 200mil body width
- 8 contact VDFN
- 8 pins PDIP
- 24 balls TFBGA (6x8mm)
- All Pb-free packages are RoHS compliant

- Industrial temperature Range

GENERAL DESCRIPTION

The EN25Q80A is an 8 Megabit (1024K-byte) Serial Flash memory, with advanced write protection mechanisms. The EN25Q80A supports the standard Serial Peripheral Interface (SPI), and a high performance Dual output as well as Quad I/O using SPI pins: Serial Clock, Chip Select, Serial DQ_0(DI), DQ_1(DO), DQ_2(WP#) and DQ_3(NC). SPI clock frequencies of up to 80MHz are supported allowing equivalent clock rates of 160MHz for Dual Output and 320MHz for Quad Output when using the Dual/Quad Output Fast Read instructions. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

The EN25Q80A is designed to allow either single Sector/Block at a time or full chip erase operation. The EN25Q80A can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

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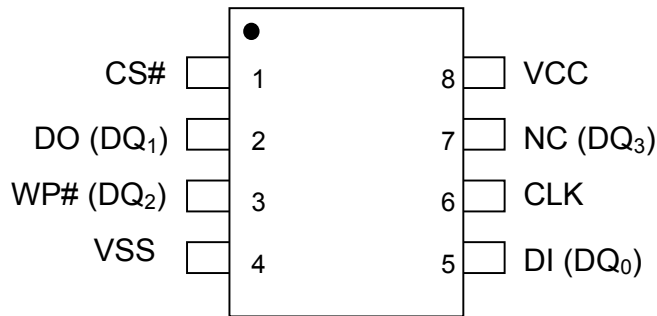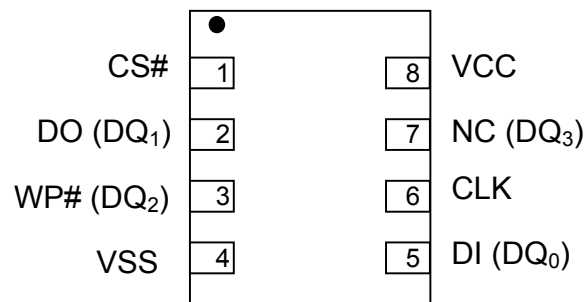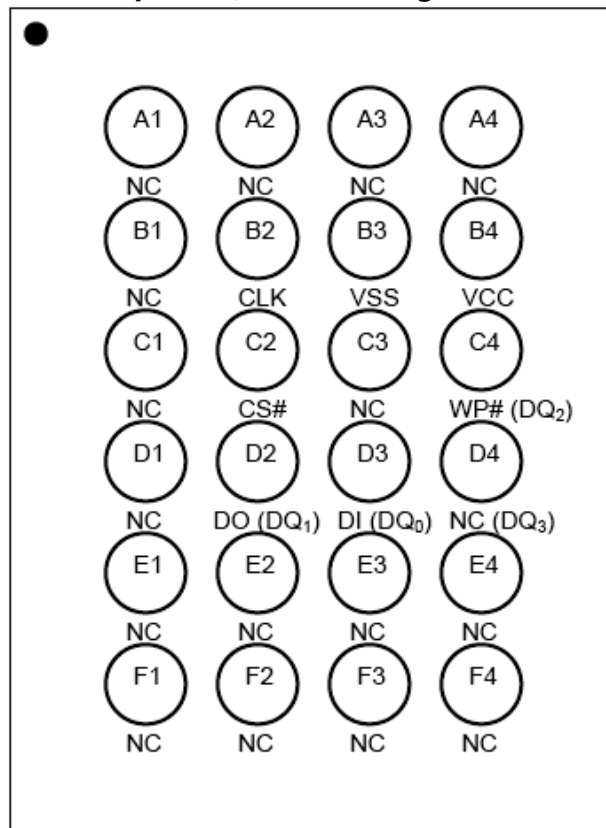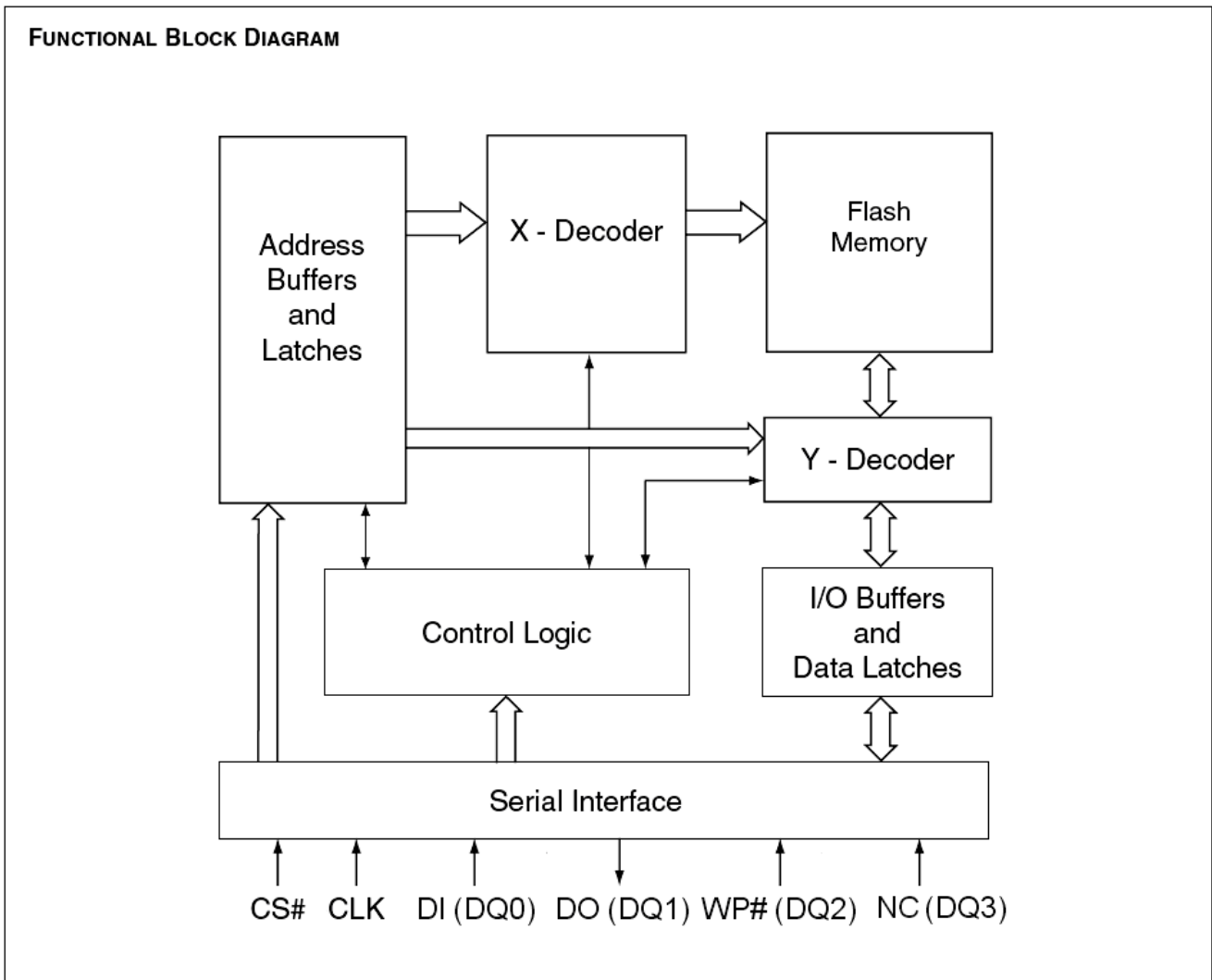
Rev. H, Issue Date: 2012/10/23

Figure.1 CONNECTION DIAGRAMS

8 - LEAD SOP / VSOP/ PDIP

8 - LEAD VDFN

Top View, Balls Facing Down

24 - Ball TFBGA

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Figure 2. BLOCK DIAGRAM

FUNCTIONAL BLOCK DIAGRAM

Note:
1. DQ_0 and DQ_1 are used for Dual and Quad instructions.
2. $DQ_0 \sim DQ_3$ are used for Quad instructions.

Table 1. Pin Names

Symbol	Pin Name
CLK	Serial Clock Input
DI (DQ$_0$)	Serial Data Input (Data Input Output 0) ^{*1}
DO (DQ$_1$)	Serial Data Output (Data Input Output 1) ^{*1}
CS#	Chip Enable
WP# (DQ$_2$)	Write Protect (Data Input Output 2) ^{*2}
NC(DQ$_3$)	Not Connect (Data Input Output 3) ^{*2}
Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground
NC	No Connect

Note:
1. DQ$_0$ and DQ$_1$ are used for Dual and Quad instructions.
2. DQ$_0$ ~ DQ$_3$ are used for Quad instructions.

SIGNAL DESCRIPTION

Serial Data Input, Output and IOs (DI, DO and DQ$_0$, DQ$_1$, DQ$_2$, DQ$_3$)

The EN25Q80A support standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge CLK.

Dual and Quad SPI instruction use the bidirectional IO pins to serially write instruction, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

Serial Clock (CLK)
The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

Chip Select (CS#)
The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO, or DQ$_0$, DQ$_1$, DQ$_2$ and DQ$_3$) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

Write Protect (WP#)
The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1and BP2) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. The WP# function is only available for standard SPI and Dual SPI operation, when during Quad SPI, this pin is the Serial Data IO (DQ$_2$) for Quad I/O operation.

MEMORY ORGANIZATION

The memory is organized as:
- 1,048,576 bytes
- Uniform Sector Architecture
  16 blocks of 64-Kbyte
  256 sectors of 4-Kbyte
- 4096 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

**Table 2.   Uniform Block Sector Architecture (Continued)**

Block	Sector	Address range	
15	255	0FF000h	0FFFFFh
	⋮	⋮	⋮
	240	0F0000h	0F0FFFh
14	239	0EF000h	0EFFFFh
	⋮	⋮	⋮
	224	0E0000h	0E0FFFh
13	223	0DF000h	0DFFFFh
	⋮	⋮	⋮
	208	0D0000h	0D0FFFh
12	207	0CF000h	0CFFFFh
	⋮	⋮	⋮
	192	0C0000h	0C0FFFh
11	191	0BF000h	0BFFFFh
	⋮	⋮	⋮
	176	0B0000h	0B0FFFh
10	175	0AF000h	0AFFFFh
	⋮	⋮	⋮
	160	0A0000h	0A0FFFh
9	159	09F000h	09FFFFh
	⋮	⋮	⋮
	144	090000h	090FFFh
8	143	08F000h	08FFFFh
	⋮	⋮	⋮
	128	080000h	080FFFh
7	127	07F000h	07FFFFh
	⋮	⋮	⋮
	112	070000h	070FFFh
6	111	06F000h	06FFFFh
	⋮	⋮	⋮
	96	060000h	060FFFh
5	95	05F000h	05FFFFh
	⋮	⋮	⋮
	80	050000h	050FFFh
4	79	04F000h	04FFFFh
	⋮	⋮	⋮
	64	040000h	040FFFh
3	63	03F000h	03FFFFh
	⋮	⋮	⋮
	48	030000h	030FFFh
2	47	02F000h	02FFFFh
	⋮	⋮	⋮
	32	020000h	020FFFh
1	31	01F000h	01FFFFh
	⋮	⋮	⋮
	16	010000h	010FFFh
0	15	00F000h	00FFFFh
	⋮		
	4	004000h	004FFFh
	3	003000h	003FFFh
	2	002000h	002FFFh
	1	001000h	001FFFh
	0	000000h	000FFFh

OPERATING FEATURES

Standard SPI Modes

The EN25Q80A is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3, as shown in Figure 3, concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of the CLK. Data output on the DO pin is clocked out on the falling edge of CLK.

Figure 3. SPI Modes
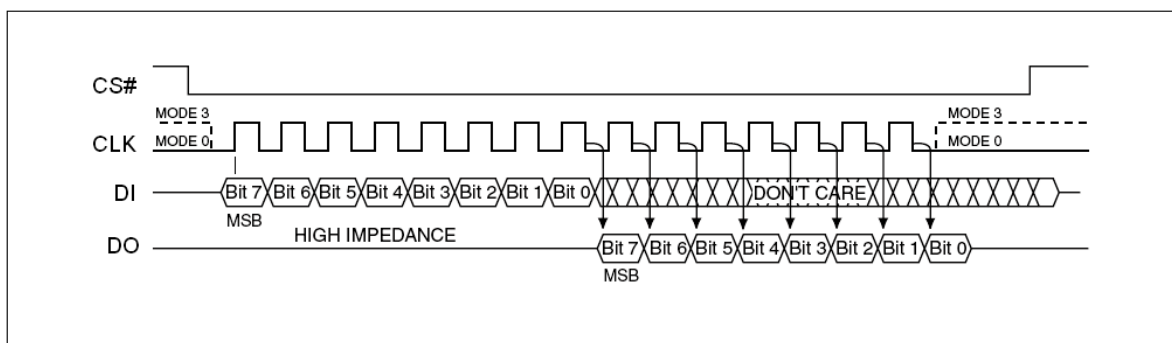
Dual SPI Instruction

The EN25Q80A supports Dual SPI operation when using the " Dual Output Fast Read and Dual I/O Fast Read " (3Bh and BBh) instructions. These instructions allow data to be transferred to or from the Serial Flash memory at two to three times the rate possible with the standard SPI. The Dual Read instructions are ideal for quickly downloading code from Flash to RAM upon power-up (code-shadowing) or for application that cache code-segments to RAM for execution. The Dual output feature simply allows the SPI input pin to also serve as an output during this instruction. When using Dual SPI instructions the DI and DO pins become bidirectional I/O pins; DQ_0 and DQ_1. All other operations use the standard SPI interface with single output signal.

Quad SPI Instruction

The EN25Q80A supports Quad output operation when using the Quad I/O Fast Read (EBh).This instruction allows data to be transferred to or from the Serial Flash memory at four to six times the rate possible with the standard SPI. The Quad Read instruction offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or for application that cache code-segments to RAM for execution. The EN25Q80A also supports full Quad Mode function while using the Enable Quad I/O (EQIO) (38h). When using Quad SPI instruction the DI and DO pins become bidirectional I/O pins; DQ_0 and DQ_1, and the WP# and NC pins become DQ_2 and DQ_3 respectively.

Figure 4. Quad SPI Modes
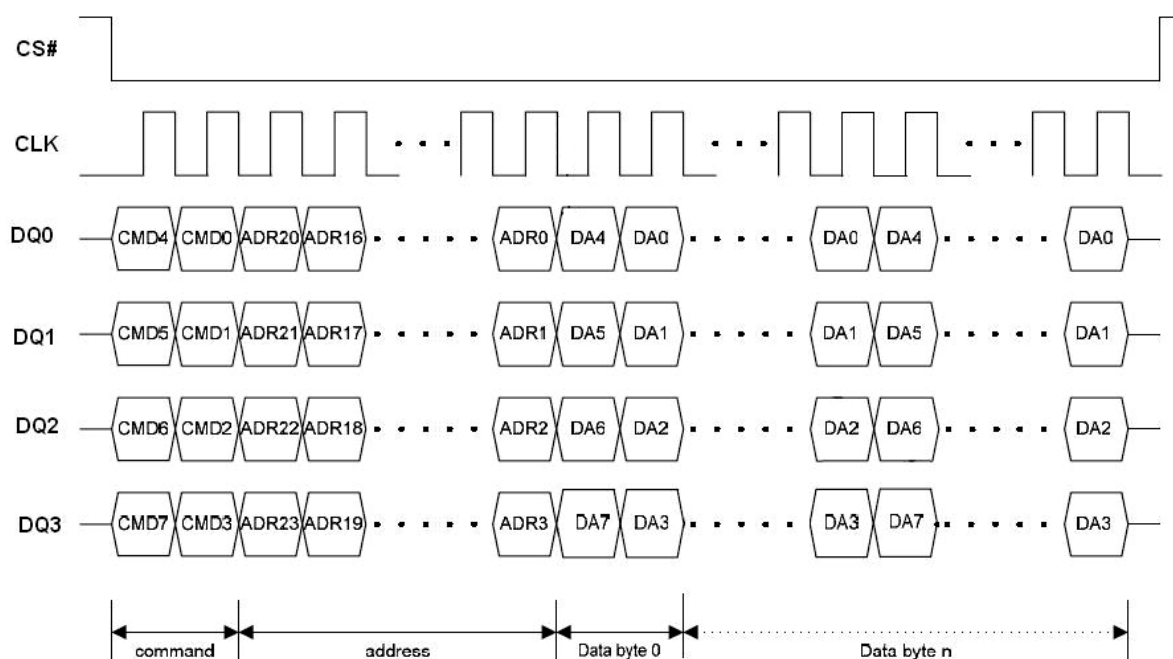
Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).

To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0) provided that they lie in consecutive addresses on the same page of memory.

Sector Erase, Block Erase and Chip Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved a sector at a time, using the Sector Erase (SE) instruction, a block at a time using the Block Erase (BE) instruction or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration t_{SE} t_{BE} or t_{CE}). The Erase instruction must be preceded by a Write Enable (WREN) instruction.

Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE, BE or CE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, t_{BE} or t_{CE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes into the Stand-by Power mode. The device consumption drops to I_{CC1}.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Device ID (RDI) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

Status Register. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions.

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions.

WPDIS bit. The Write Protect disable (WPDIS) bit, non-volatile bit, when it is reset to "0" (factory default) to enable WP# function or is set to "1" to disable WP# function (can be floating during SPI mode.)

SRP bit / OTP_LOCK bit The Status Register Protect (SRP) bit operates in conjunction with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRP, BP2, BP1, BP0) become read-only bits.

In OTP mode, this bit serves as OTP_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP_LOCK bit value is equal 0, after OTP_LOCK bit is programmed with 1 by WRSR command, the OTP sector is protected from program and erase operation. The OTP_LOCK bit can only be programmed once.

Note : In OTP mode, the WRSR command will ignore any input data and program OTP_LOCK bit to 1, user must clear the protect bits before entering OTP mode and program the OTP code, then execute WRSR command to lock the OTP sector before leaving OTP mode.

Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the EN25Q80A provides the following data protection mechanisms:
- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  – Power-up
  – Write Disable (WRDI) instruction completion or Write Status Register (WRSR) instruction completion or Page Program (PP) instruction completion or Sector Erase (SE) instruction completion or Block Erase (BE) instruction completion or Chip Erase (CE) instruction completion

- The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect (WP#) signal allows the Block Protect (BP2, BP1, BP0) bits and Status Register Protect (SRP) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Table 3. Protected Area Sizes Sector Organization

Status Register Content			Memory Content			
BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	None	None	None	None
0	0	1	Sector 0 to 253	000000h-0FDFFFh	1016KB	Lower 254/256
0	1	0	Sector 0 to 251	000000h-0FBFFFh	1008KB	Lower 252/256
0	1	1	Sector 0 to 247	000000h-0F7FFFh	992KB	Lower 248/256
1	0	0	Sector 0 to 239	000000h-0EFFFFh	960KB	Lower 240/256
1	0	1	Sector 0 to 223	000000h-0DFFFFh	896KB	Lower 224/256
1	1	0	Sector 0 to 191	000000h-0BFFFFh	768KB	Lower 192/256
1	1	1	All	000000h-0FFFFFh	1024KB	All

INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first. Serial Data Input (DI) is sampled on the first rising edge of Serial Clock (CLK) after Chip Select (CS#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (DI), each bit being latched on the rising edges of Serial Clock (CLK).

The instruction set is listed in Table 4. Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Select (CS#) must be driven High after the last bit of the instruction sequence has been shifted in. In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Read Status Register (RDSR) or Release from Deep Power-down, and Read Device ID (RDI) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (CS#) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select (CS#) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (CS#) must driven High when the number of clock pulses after Chip Select (CS#) being driven Low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

In the case of multi-byte commands of Page Program (PP), and Release from Deep Power Down (RES) minimum number of bytes specified has to be given, without which, the command will be ignored.

In the case of Page Program, if the number of byte after the command is less than 4 (at least 1 data byte), it will be ignored too. In the case of SE and BE, exact 24-bit address is a must, any less or more will cause the command to be ignored.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 4A. Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
EQIO	38h						
RSTQIO[1]	FFh						
Write Enable	06h						
Write Disable / Exit OTP mode	04h						
Read Status Register	05h	(S7-S0)[2]					continuous[3]
Write Status Register	01h	S7-S0					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase / OTP erase	20h	A23-A16	A15-A8	A7-A0			
Block Erase	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(4)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(5)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(6)		
Enter OTP mode	3Ah						

Notes:
1. Device accepts eight-clocks command in Standard SPI mode, or two-clocks command in Quad SPI mode.
2. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the DO pin.
3. The Status Register contents will repeat continuously until CS# terminate the instruction.
4. The Device ID will repeat continuously until CS# terminates the instruction.
5. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction.
   00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID.
6. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity.

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Table 4B. Instruction Set (Read Instruction)

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous
Dual Output Fast Read	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, ...) [1]	(one byte per 4 clocks, continuous)
Dual I/O Fast Read	BBh	A23-A8[2]	A7-A0, dummy [2]	(D7-D0, ...) [1]			(one byte per 4 clocks, continuous)
Quad I/O Fast Read	EBh	A23-A0, dummy [4]	(dummy, D7-D0) [5]	(D7-D0, ...) [3]			(one byte per 2 clocks, continuous)

Notes:

1. Dual Output data
    DQ_0 = (D6, D4, D2, D0)
    DQ_1 = (D7, D5, D3, D1)

2. Dual Input Address
    DQ_0 = A22, A20, A18, A16, A14, A12, A10, A8 ; A6, A4, A2, A0, dummy 6, dummy 4, dummy 2, dummy 0
    DQ_1 = A23, A21, A19, A17, A15, A13, A11, A9 ; A7, A5, A3, A1, dummy 7, dummy 5, dummy 3, dummy 1

3. Quad Data
    DQ_0 = (D4, D0, ……)
    DQ_1 = (D5, D1, ……)
    DQ_2 = (D6, D2, …...)
    DQ_3 = (D7, D3, …...)

4. Quad Input Address
    DQ_0 = A20, A16, A12,   A8, A4, A0, dummy 4, dummy 0
    DQ_1 = A21, A17, A13,   A9, A5, A1, dummy 5, dummy 1
    DQ_2 = A22, A18, A14, A10, A6, A2, dummy 6, dummy 2
    DQ_3 = A23, A19, A15, A11, A7, A3, dummy 7, dummy 3

5. Quad I/O Fast Read Data
    DQ_0 = (dummy 12, dummy   8, dummy 4, dummy 0, D4, D0)
    DQ_1 = (dummy 13, dummy   9, dummy 5, dummy 1, D5, D1)
    DQ_2 = (dummy 14, dummy 10, dummy 6, dummy 2, D6, D2)
    DQ_3 = (dummy 15, dummy 11, dummy 7, dummy 3, D7, D3)

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Table 5. Manufacturer and Device Identification

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			13h
90h	1Ch		13h
9Fh	1Ch	3014h	

Enable Quad I/O (EQIO) (38h)

The Enable Quad I/O (EQIO) instruction will enable the flash device for Quad SPI bus operation. Upon completion of the instruction, all instructions thereafter will be 4-bit multiplexed input/output until a power cycle or " Reset Quad I/O instruction " instruction, as shown in Figure 5. The device did not support the Read Data Bytes (READ) (03h), Dual Output Fast Read (3Bh) and Dual Input/Output FAST_READ (BBh) modes while the Enable Quad I/O (EQIO) (38h) turns on.
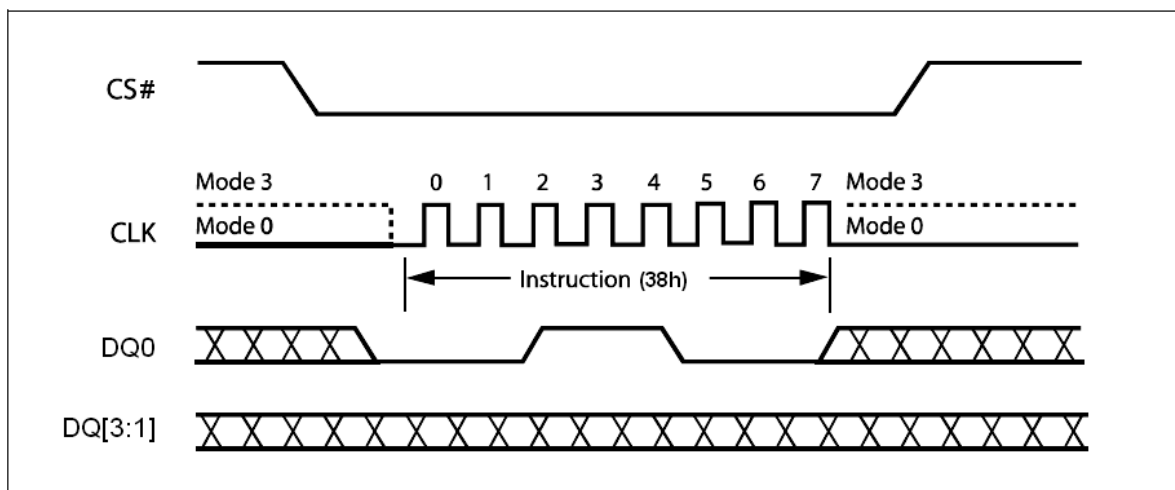
Figure 5. Enable Quad I/O Sequence Diagram

Reset Quad I/O (RSTQIO) (FFh)

The Reset Quad I/O instruction resets the device to 1-bit Standard SPI operation. To execute a Reset Quad I/O operation, the host drives CS# low, sends the Reset Quad I/O command cycle (FFh) then, drives CS# high. This command can't be used in Standard SPI mode.

Write Enable (WREN) (06h)

The Write Enable (WREN) instruction (Figure 6) sets the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) instruction.

The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

The instruction sequence is shown in Figure 7.1 while using the Enable Quad I/O (EQIO) (38h) command.
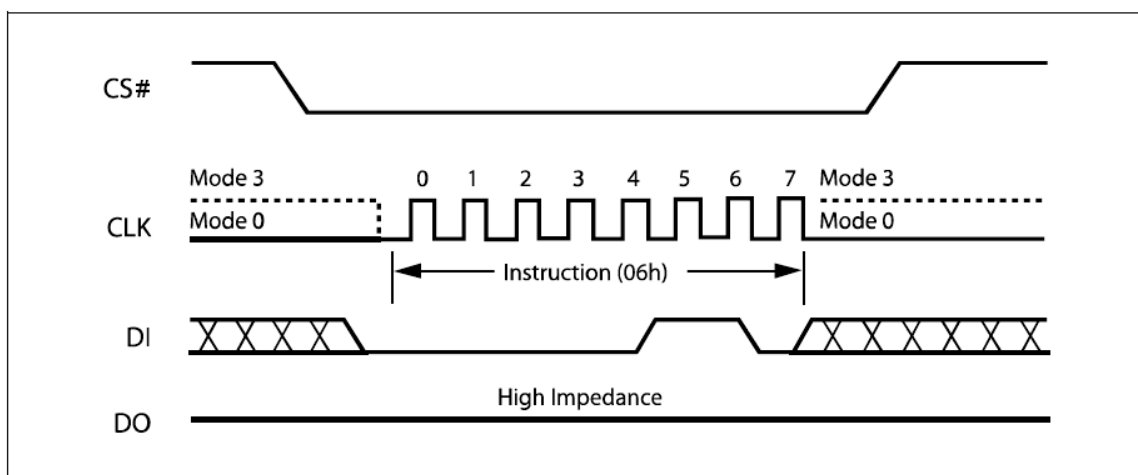
Figure 6. Write Enable Instruction Sequence Diagram

Write Disable (WRDI) (04h)

The Write Disable instruction (Figure 7) resets the Write Enable Latch (WEL) bit in the Status Register to a 0 or exit from OTP mode to normal mode. The Write Disable instruction is entered by driving Chip Select (CS#) low, shifting the instruction code "04h" into the DI pin and then driving Chip Select (CS#) high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase (BE) and Chip Erase instructions.

The instruction sequence is shown in Figure 7.1 while using the Enable Quad I/O (EQIO) (38h) command.
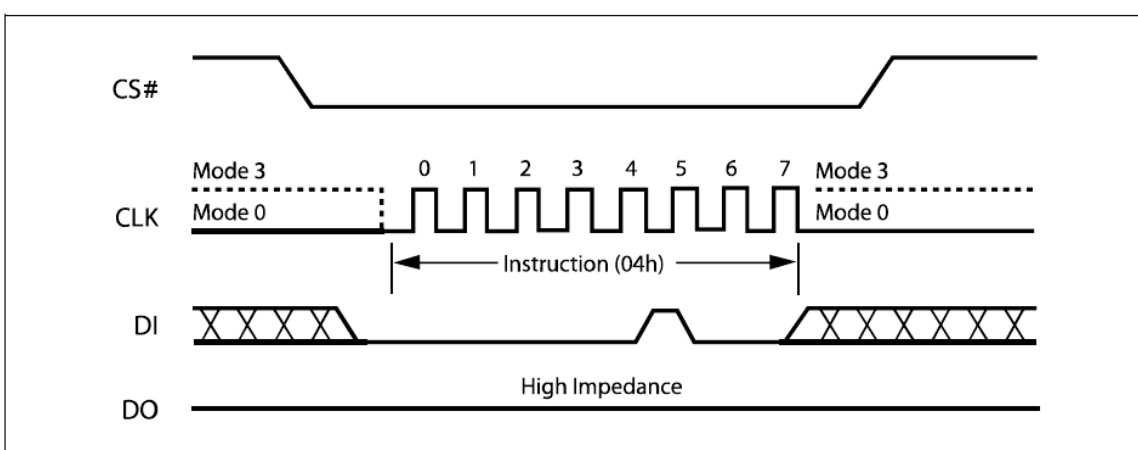
Figure 7. Write Disable Instruction Sequence Diagram
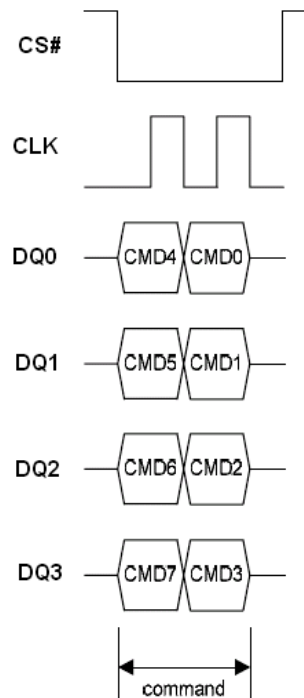
Figure 7.1 Write Enable/Disable Instruction Sequence under EQIO Mode

Read Status Register (RDSR) (05h)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 8.

The instruction sequence is shown in Figure 8.1 while using the Enable Quad I/O (EQIO) (38h) command.
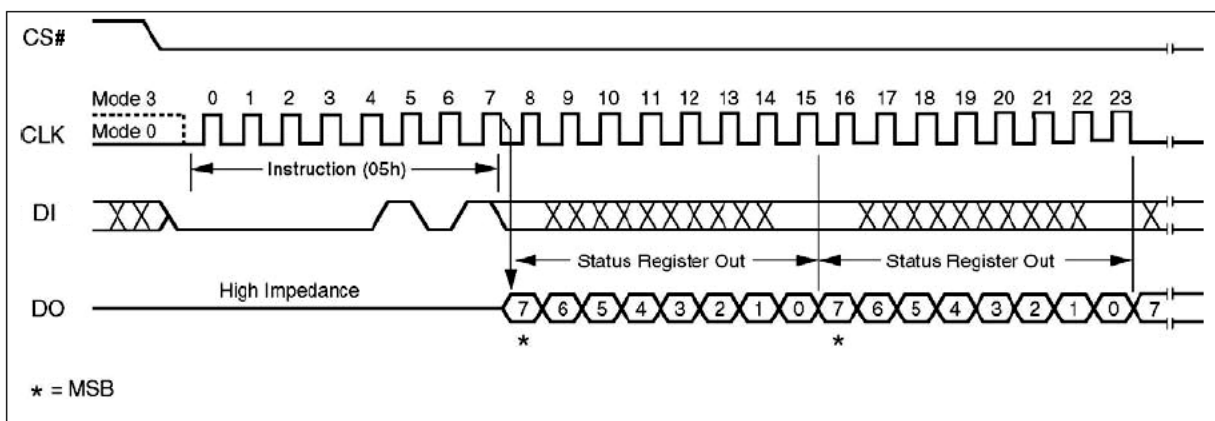
Figure 8. Read Status Register Instruction Sequence Diagram

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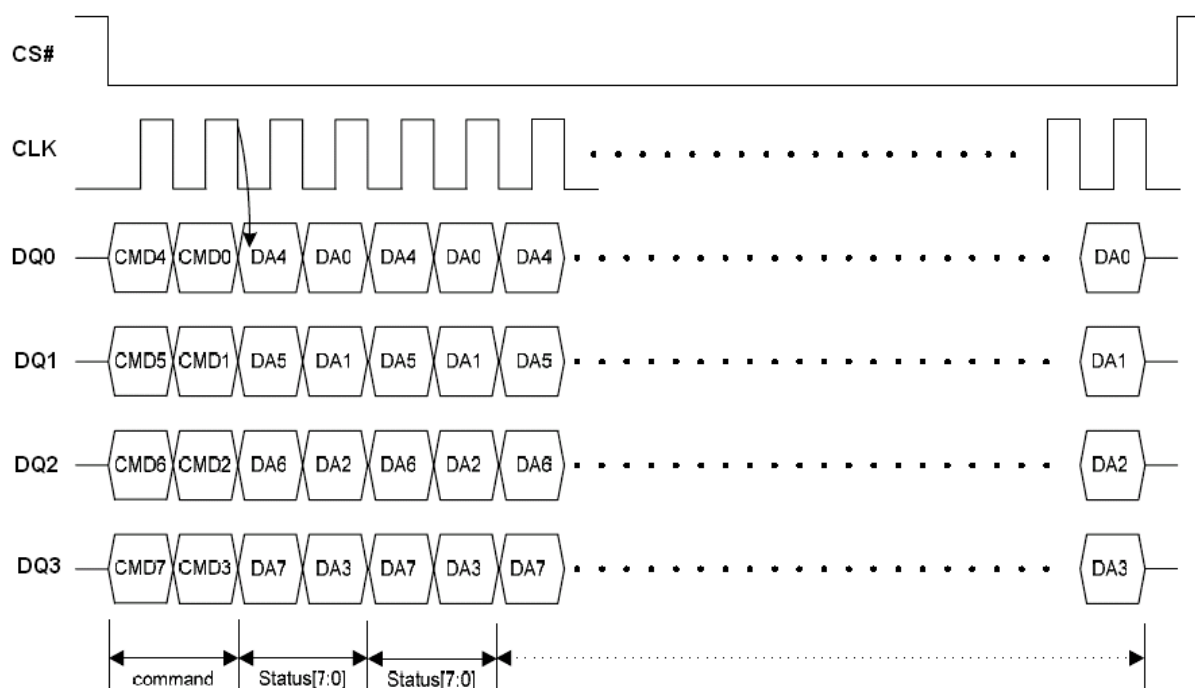
Figure 8.1 Read Status Register Instruction Sequence under EQIO Mode

Table 6. Status Register Bit Locations

	S7	S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WPDIS (WP# disable)	Reserved bits	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit)
1 = status register write disable	1 = OTP sector is protected	1 = WP# disable 0 = WP# enable		(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit		Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note
1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".

The status and control bits of the Status Register are as follows:

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 3.) becomes protected against Page Program (PP) Sector Erase (SE) and , Block Erase (BE), instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) instruction is executed if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0.

Reserved bit. Status register bit locations 5 is reserved for future use. Current devices will read 0 for this bit location. It is recommended to mask out the reserved bit when testing the Status Register. Doing this will ensure compatibility with future devices.

WPDIS bit. The Write Protect disable (WPDIS) bit, non-volatile bit, when it is reset to "0" (factory default) to enable WP# function or is set to "1" to disable WP# function (can be floating during SPI mode.)

SRP bit / OTP_LOCK bit. The Status Register Protect (SRP) bit operates in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRP, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

In OTP mode, this bit serves as OTP_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP_LOCK bit value is equal 0, after OTP_LOCK bit is programmed with 1 by WRSR command, the OTP sector is protected from program and erase operation. The OTP_LOCK bit can only be programmed once.

Note : In OTP mode, the WRSR command will ignore any input data and program OTP_LOCK bit to 1, user must clear the protect bits before enter OTP mode and program the OTP code, then execute WRSR command to lock the OTP sector before leaving OTP mode.

Write Status Register (WRSR) (01h)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).
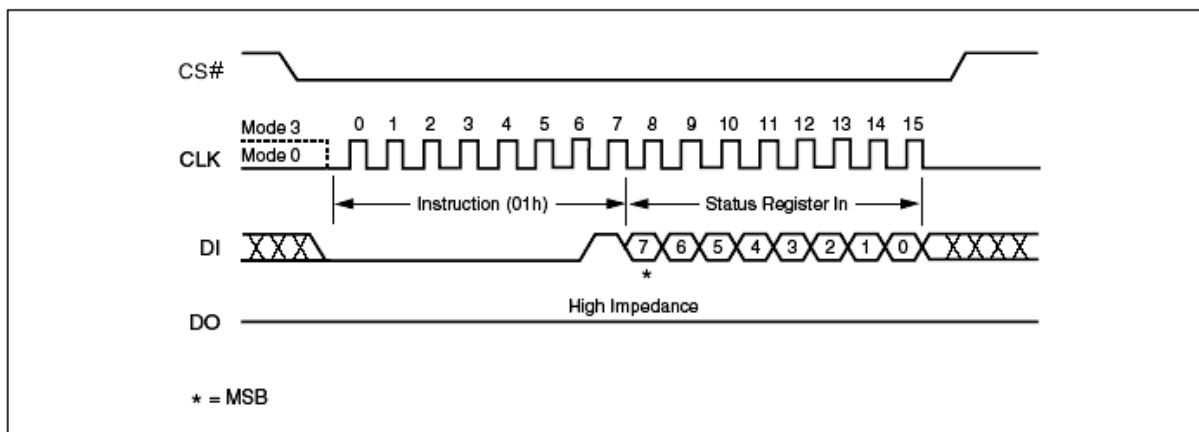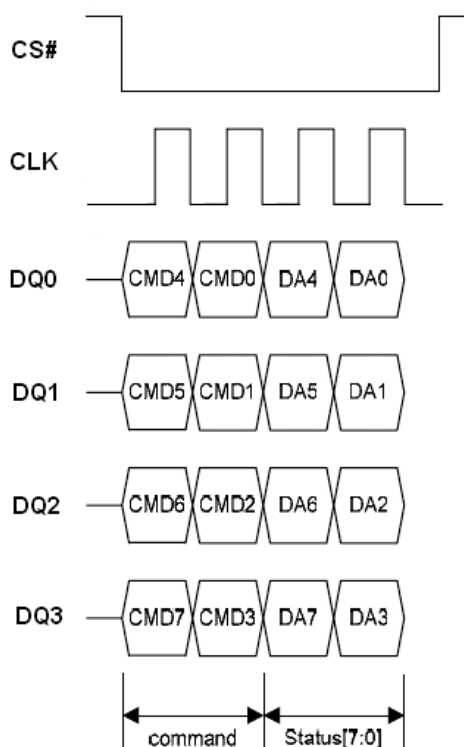
The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte on Serial Data Input (DI).

The instruction sequence is shown in Figure 9. The Write Status Register (WRSR) instruction has no effect on S5, S1 and S0 of the Status Register. S5 is always read as 0. Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 3. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

The instruction sequence is shown in Figure 9.1 while using the Enable Quad I/O (EQIO) (38h) command.

NOTE : In the OTP mode, WRSR command will ignore input data and program OTP_LOCK bit to 1.

Figure 9. Write Status Register Instruction Sequence Diagram

Figure 9.1 Write Status Register Instruction Sequence under EQIO Mode

Read Data Bytes (READ) (03h)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.
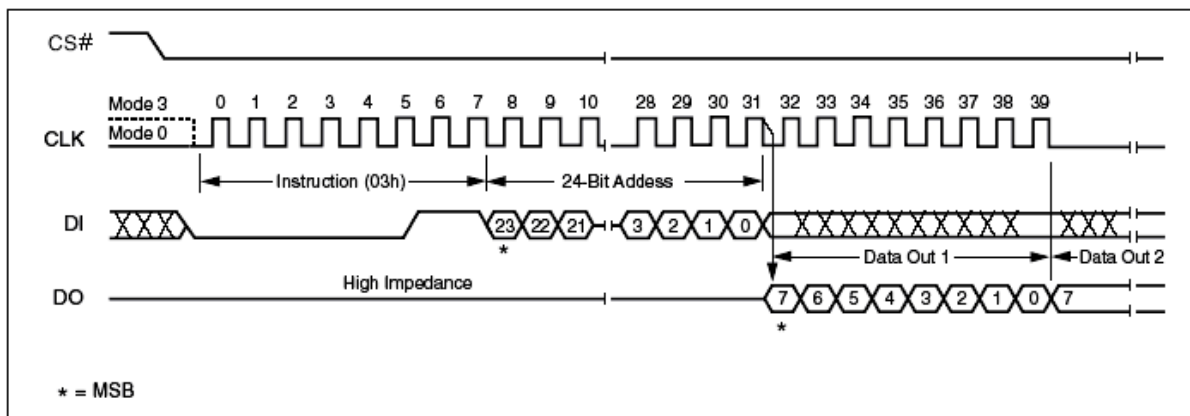

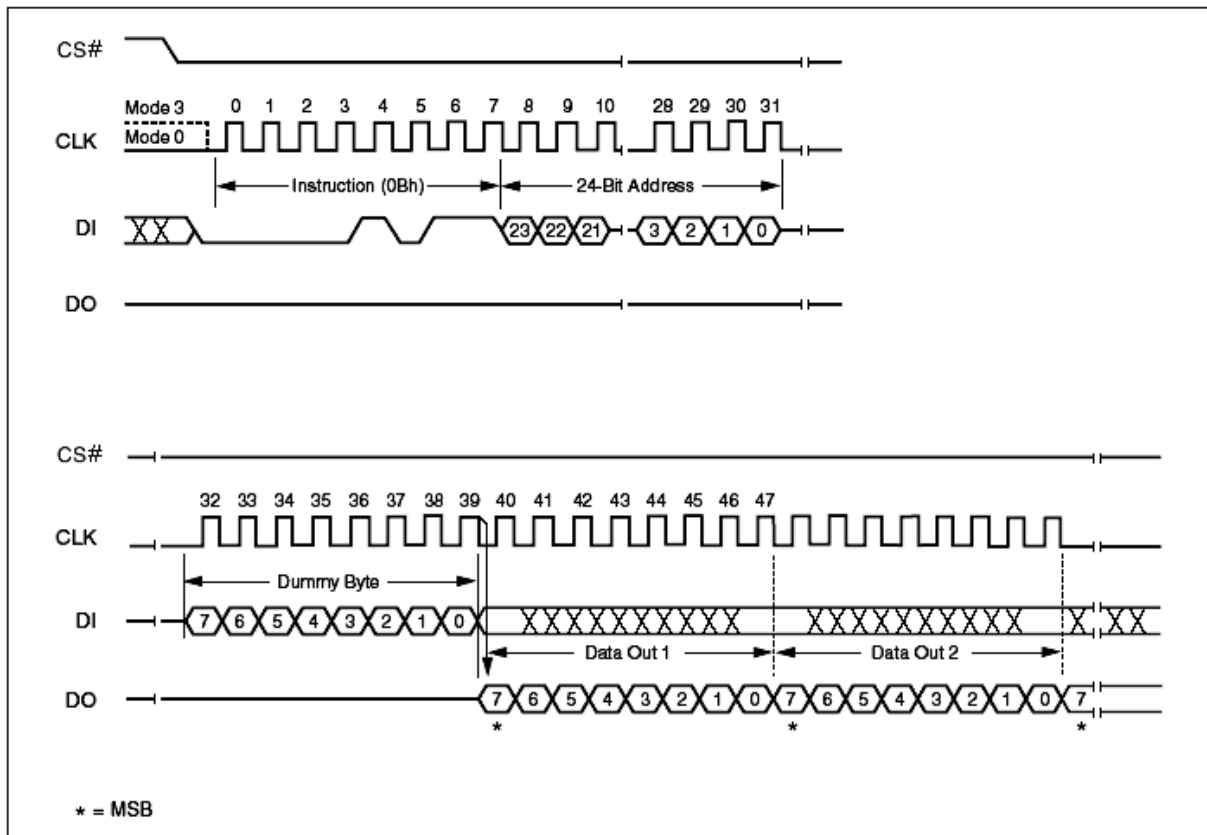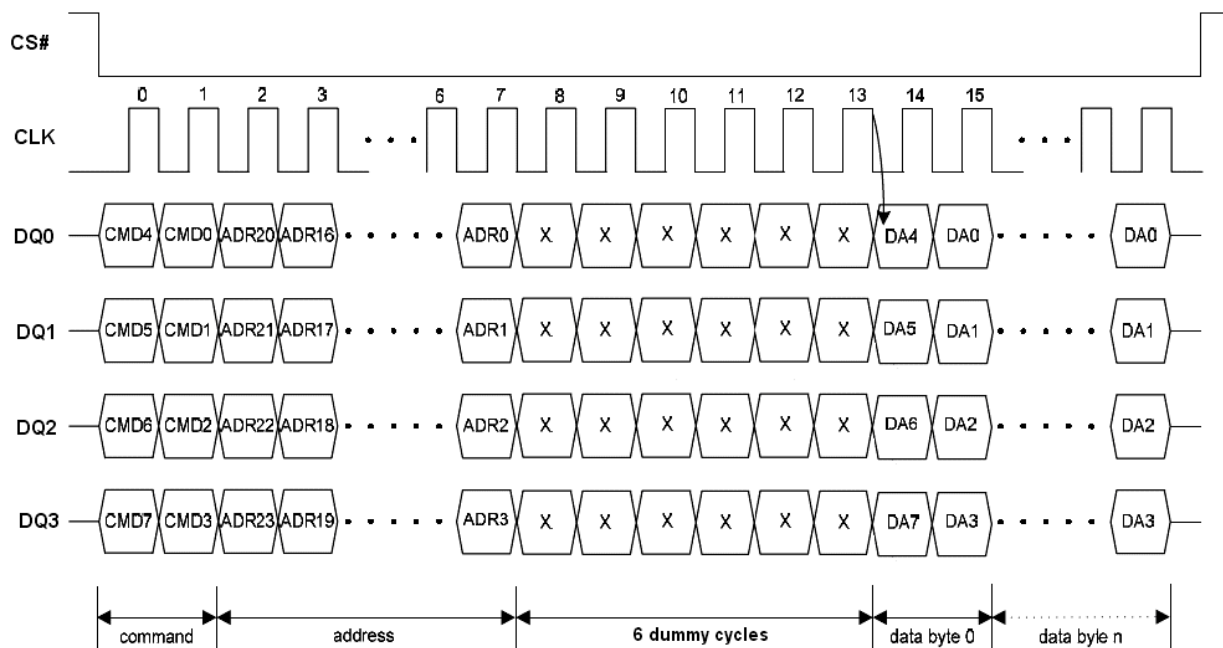
Figure 10. Read Data Instruction Sequence Diagram

Read Data Bytes at Higher Speed (FAST_READ) (0Bh)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 11. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

The instruction sequence is shown in Figure 11.1 while using the Enable Quad I/O (EQIO) (38h) command.

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Figure 11. Fast Read Instruction Sequence Diagram

Figure 11.1 Fast Read Instruction Sequence under EQIO Mode

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Dual Output Fast Read (3Bh)

The Dual Output Fast Read (3Bh) is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DQ_0 and DQ_1, instead of just DQ_0. This allows data to be transferred from the EN25Q80A at twice the rate of standard SPI devices. The Dual Output Fast Read instruction is ideal for quickly downloading code from to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Dual Output Fast Read instruction can operation at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy clocks after the 24-bit address as shown in Figure 12. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clock is "don't care". However, the DI pin should be high-impedance prior to the falling edge of the first data out clock.
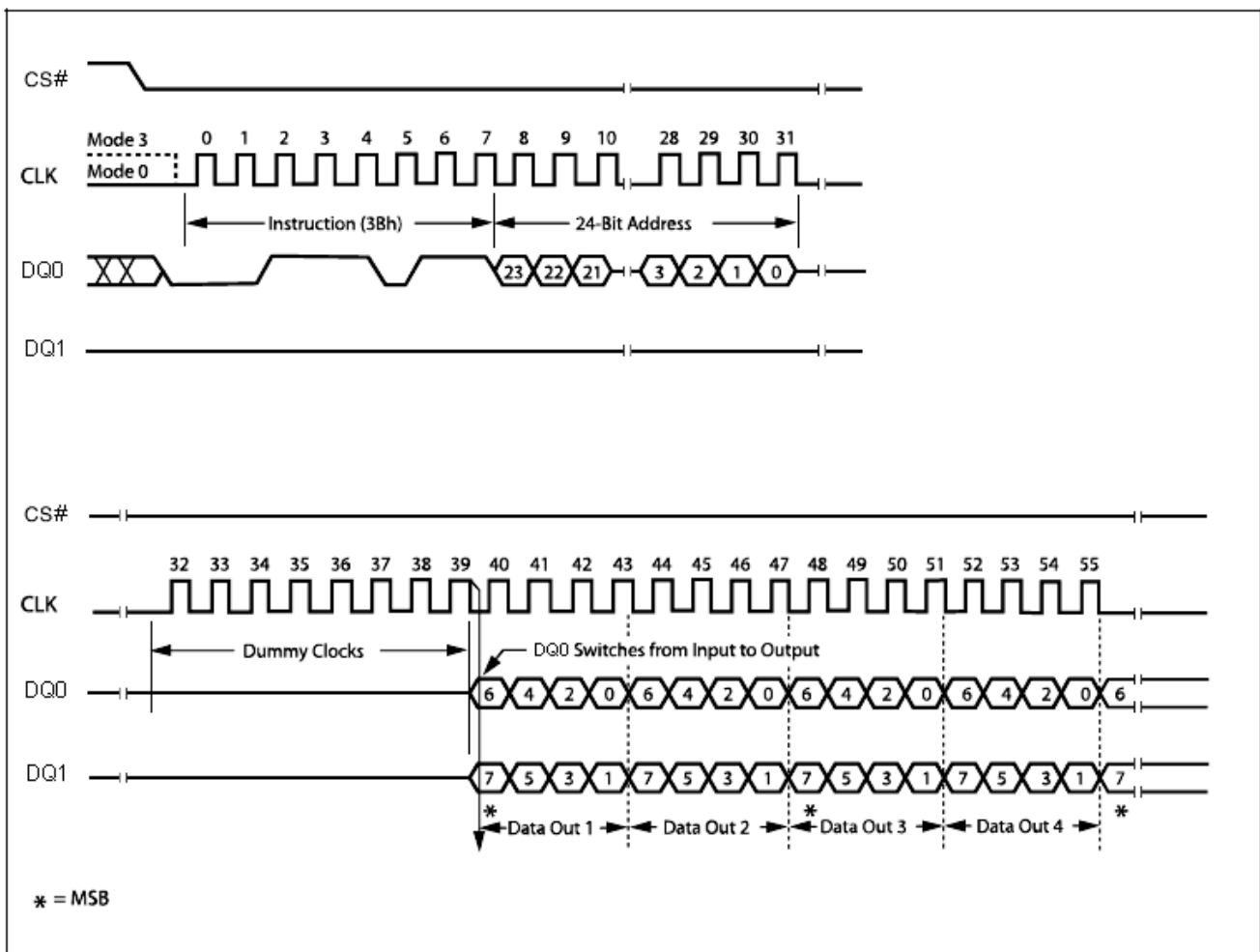

Figure 12. Dual Output Fast Read Instruction Sequence Diagram

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Dual Input / Output FAST_READ (BBh)

The Dual I/O Fast Read (BBh) instruction allows for improved random access while maintaining two IO pins, DQ_0 and DQ_1. It is similar to the Dual Output Fast Read (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The Dual I/O Fast Read instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of CLK, and data of every two bits (interleave 2 I/O pins) shift out on the falling edge of CLK at a maximum frequency. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Dual I/O Fast Read instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing Dual I/O Fast Read instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit, as shown in Figure 13.
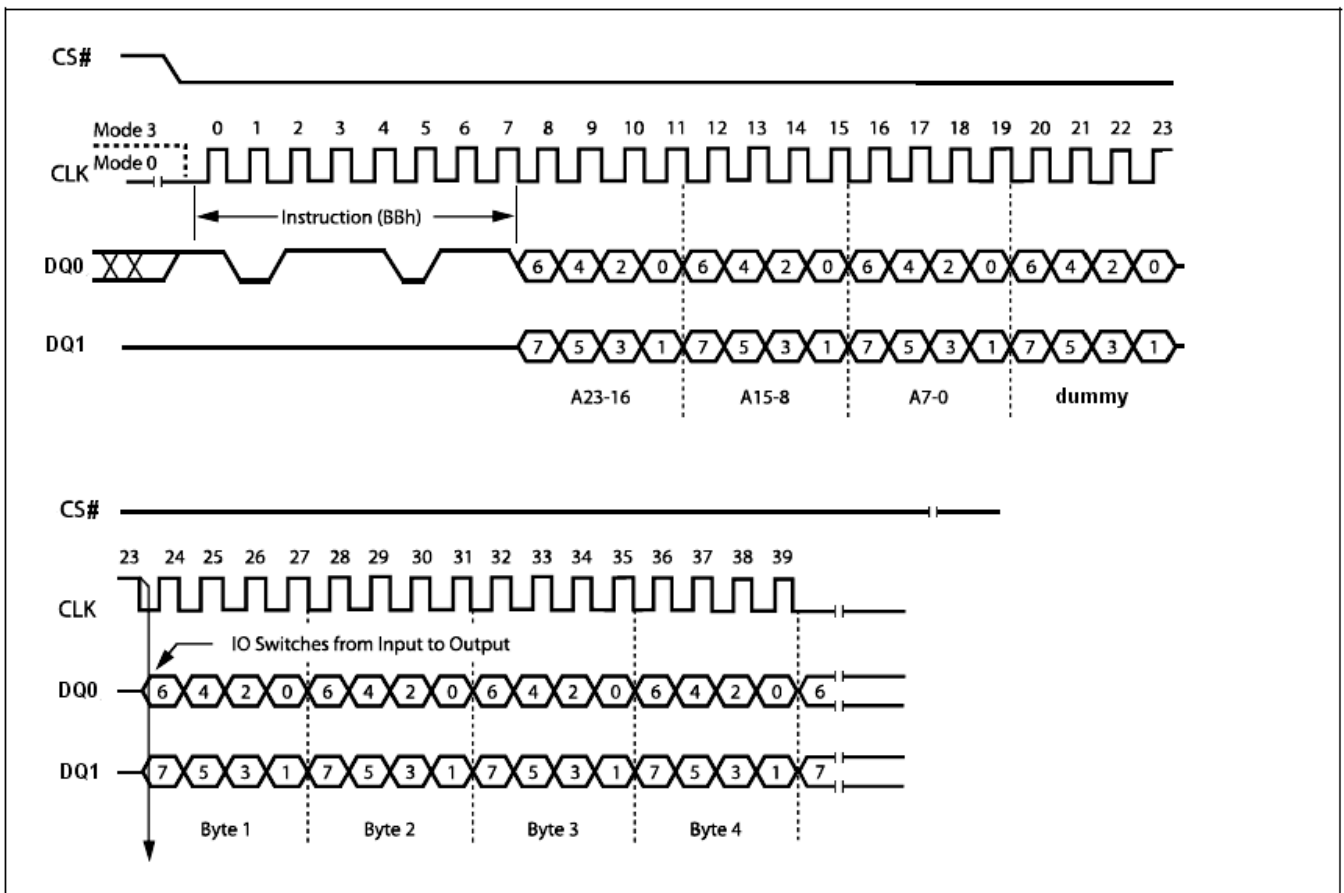

Figure 13. Dual Input / Output Fast Read Instruction Sequence Diagram

Quad Input / Output FAST_READ (EBh)

The Quad Input/Output FAST_READ (EBh) instruction is similar to the Dual I/O Fast Read (BBh) instruction except that address and data bits are input and output through four pins, DQ_0, DQ_1, DQ_2 and DQ_3 and six dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Quad Input/Output FAST_READ (EBh) instruction enable quad throughput of Serial Flash in read mode. The address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift our on the falling edge of CLK at a maximum frequency F_R. The first address can be any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Quad Input/Output FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing Quad Input/Output FAST_READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing Quad Input/Output FAST_READ (EBh) instruction is: CS# goes low -> sending Quad Input/Output FAST_READ (EBh) instruction -> 24-bit address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> 6 dummy cycles -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> to end Quad Input/Output FAST_READ (EBh) operation can use CS# to high at any time during data out, as shown in Figure 14.

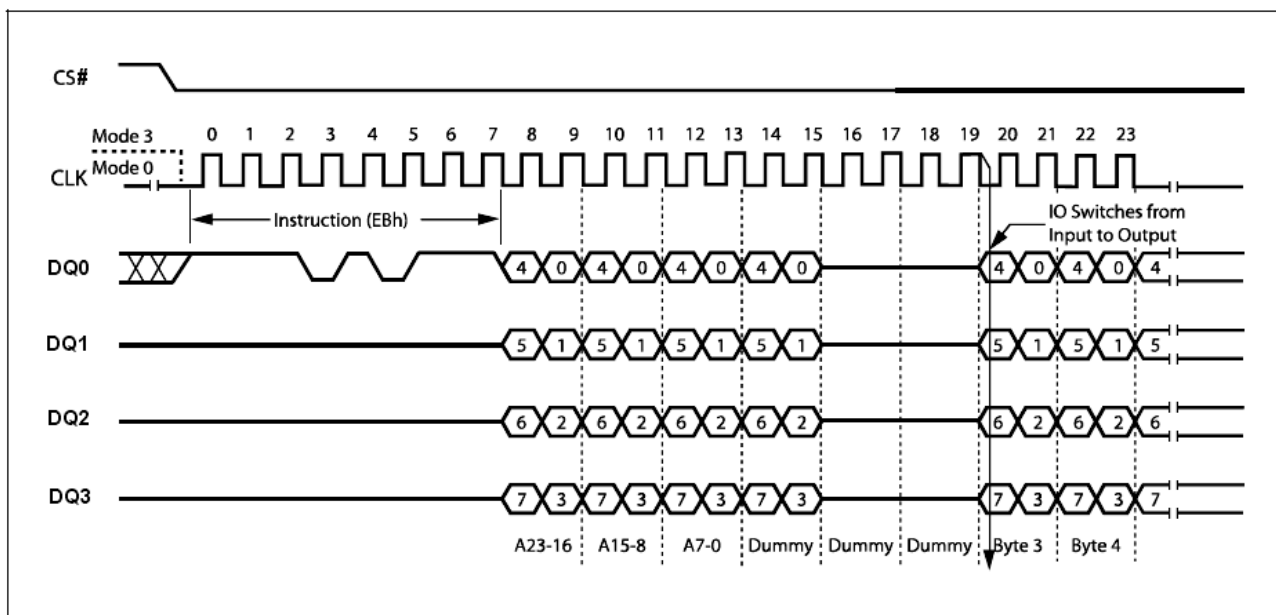The instruction sequence is shown in Figure 14.1 while using the Enable Quad I/O (EQIO) (38h) command.

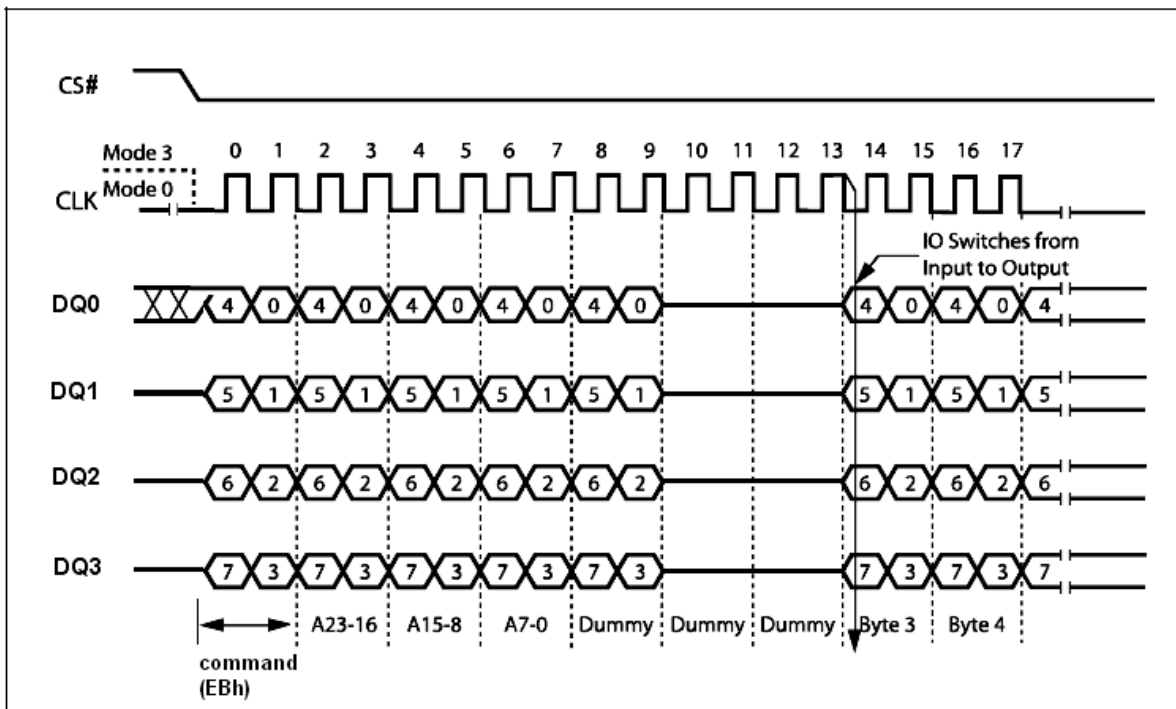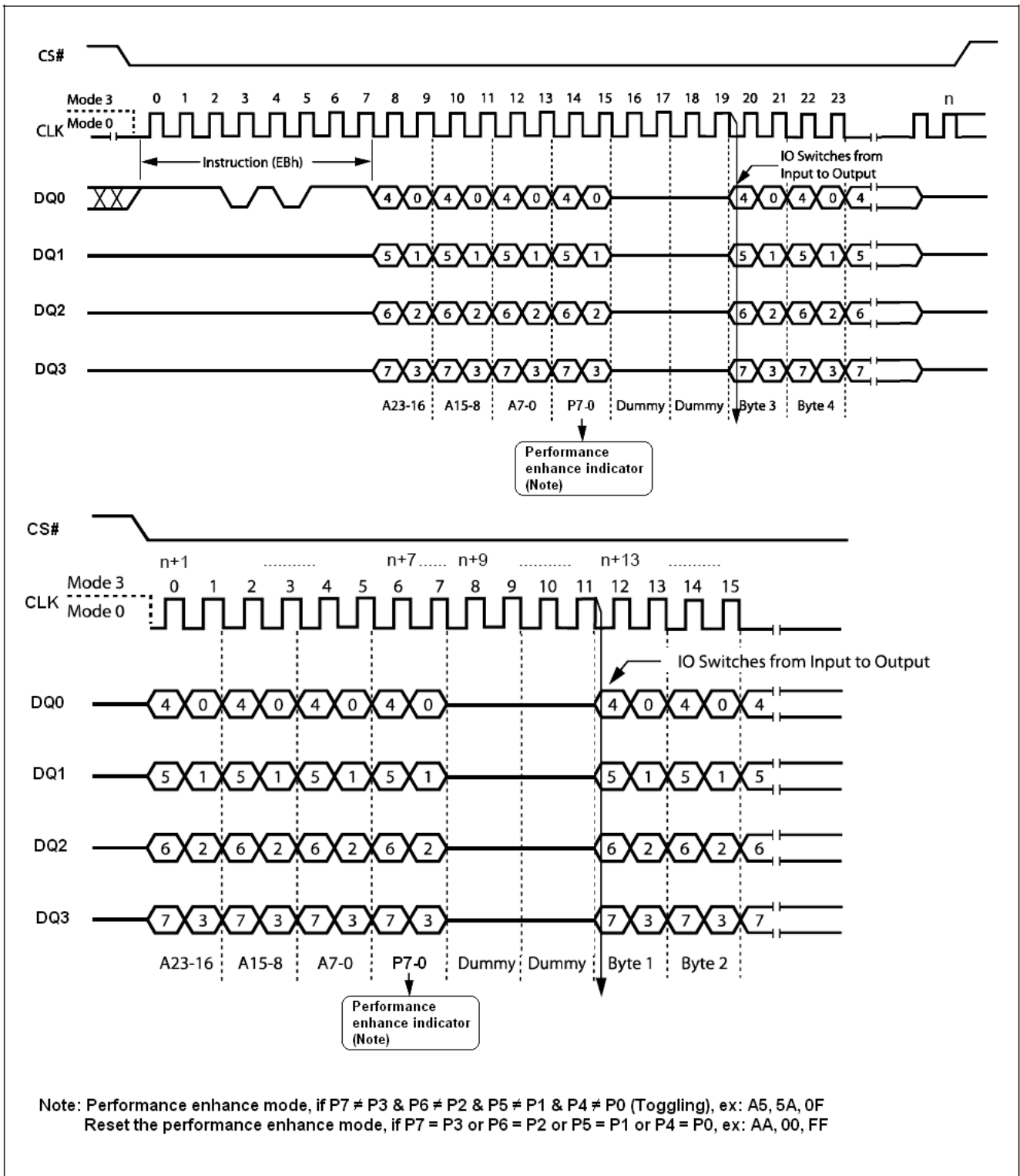**Figure 14. Quad Input / Output Fast Read Instruction Sequence Diagram**

Figure 14.1. Quad Input / Output Fast Read Instruction Sequence under EQIO Mode
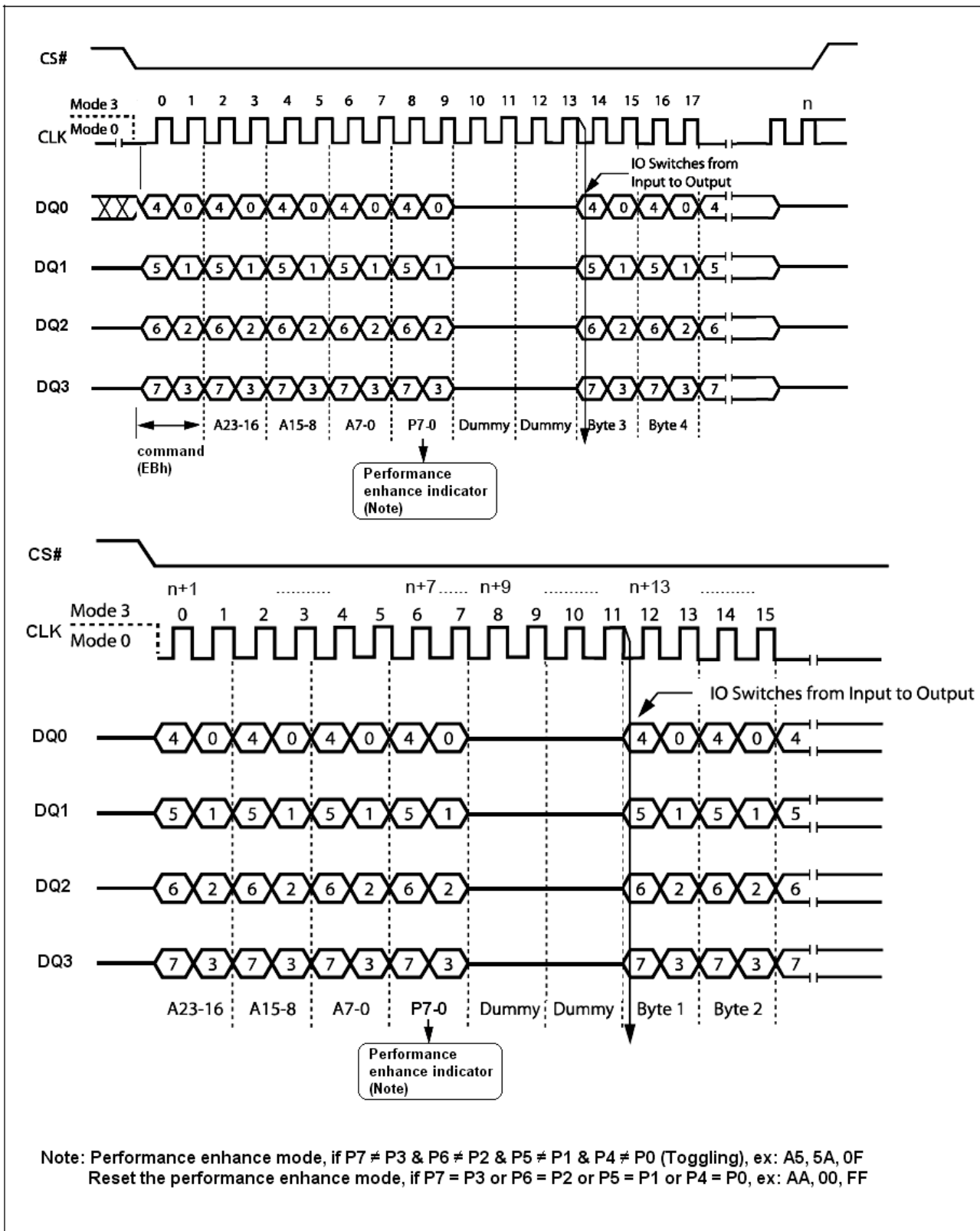
Another sequence of issuing Quad Input/Output FAST_READ (EBh) instruction especially useful in random access is : CS# goes low -> sending Quad Input/Output FAST_READ (EBh) instruction -> 24-bit address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> performance enhance toggling bit P[7:0] -> 4 dummy cycles -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 till CS# goes high -> CS# goes low (reduce Quad Input/Output FAST_READ (EBh) instruction) -> 24-bit random access address, as shown in Figure 15.

In the performance – enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0] = A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next Quad Input/Output FAST_READ (EBh) instruction. Once P[7:4] is no longer toggling with P[3:0] ; likewise P[7:0] = FFh, 00h, AAh or 55h. And afterwards CS# is raised, the system then will escape from performance enhance mode and return to normal operation.

While Program/ Erase/ Write Status Register is in progress, Quad Input/Output FAST_READ (EBh) instruction is rejected without impact on the Program/ Erase/ Write Status Register current cycle.

The instruction sequence is shown in Figure 15.1 while using the Enable Quad I/O (EQIO) (38h) command.

Figure 15. Quad Input/Output Fast Read Enhance Performance Mode Sequence Diagram

This Data Sheet may be revised by subsequent versions or modifications due to changes in technical specifications.

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Figure 15.1 Quad Input/Output Fast Read Enhance Performance Mode Sequence under EQIO Mode

Note: Performance enhance mode, if P7 ≠ P3 & P6 ≠ P2 & P5 ≠ P1 & P4 ≠ P0 (Toggling), ex: A5, 5A, 0F
Reset the performance enhance mode, if P7 = P3 or P6 = P2 or P5 = P1 or P4 = P0, ex: AA, 00, FF

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Page Program (PP) (02h)

The Page Program (PP) instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (DI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 16. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select (CS#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select (CS#) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.

The instruction sequence is shown in Figure 16.1 while using the Enable Quad I/O (EQIO) (38h) command.
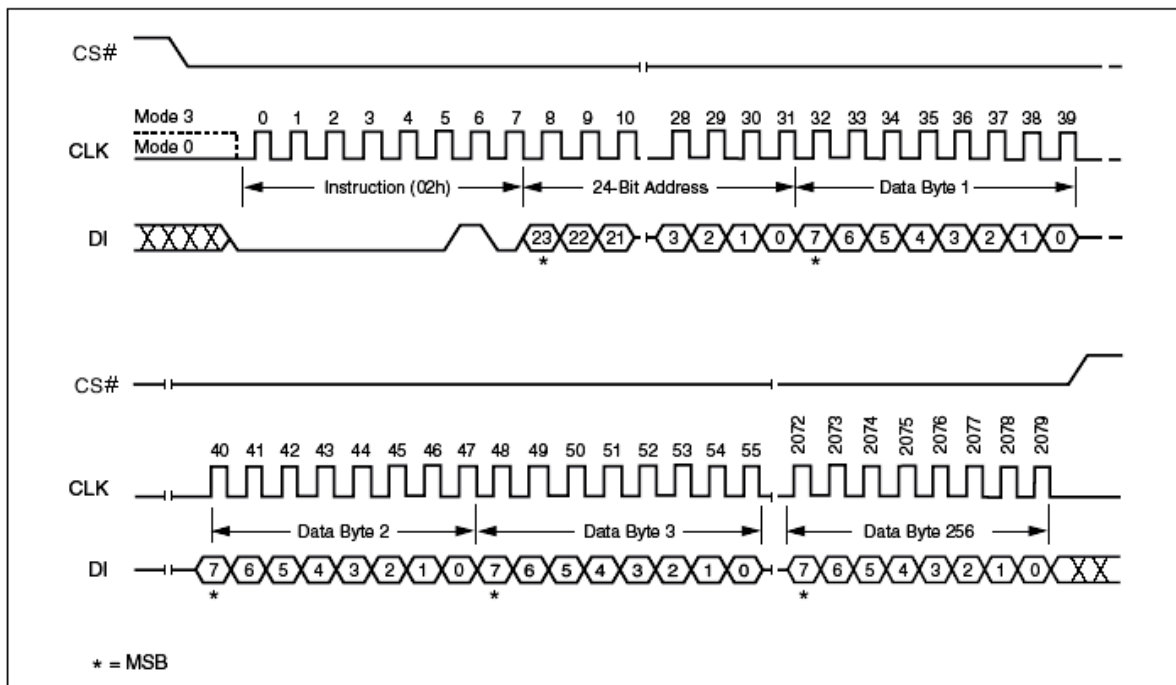

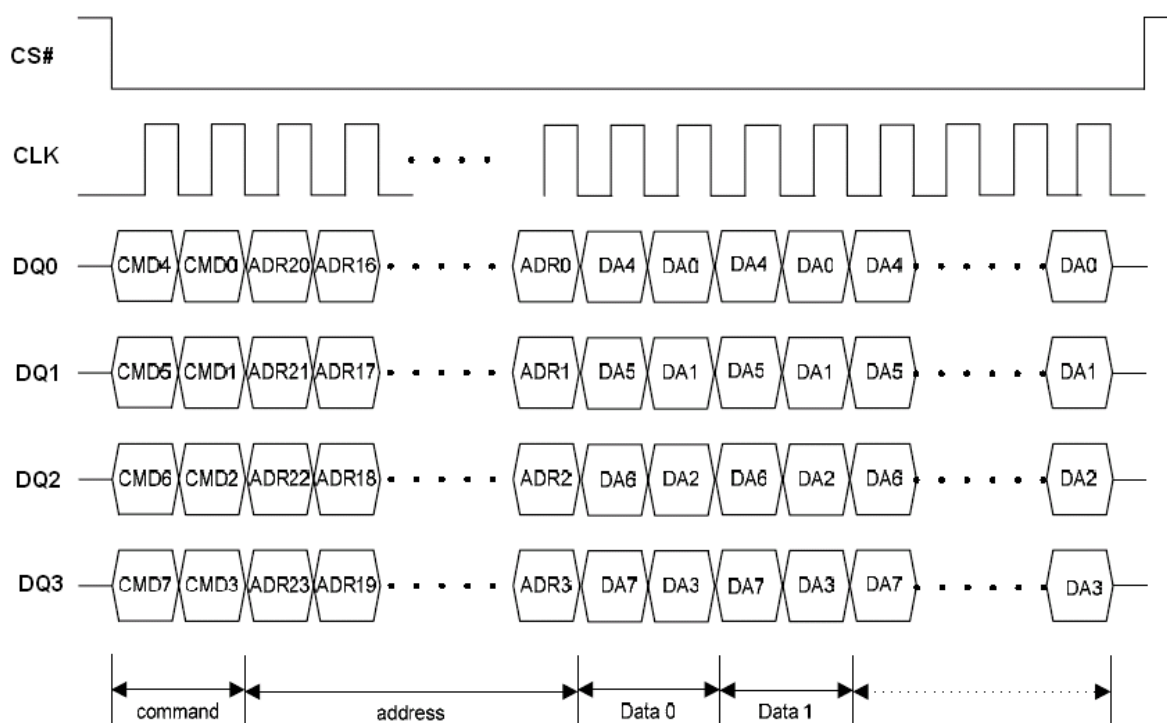**Figure 16. Page Program Instruction Sequence Diagram**

Figure 16.1 Program Instruction Sequence under EQIO Mode

Sector Erase (SE) (20h)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Sector (see Table 2) is a valid address for the Sector Erase (SE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 17. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a sector which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.

The instruction sequence is shown in Figure 18.1 while using the Enable Quad I/O (EQIO) (38h) command.
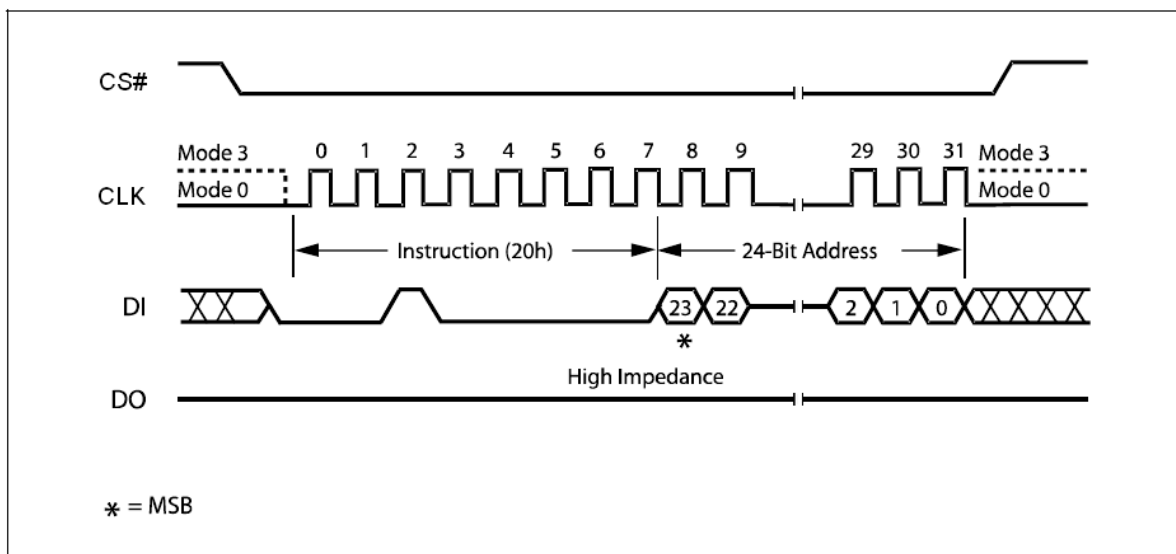
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Figure 17. Sector Erase Instruction Sequence Diagram
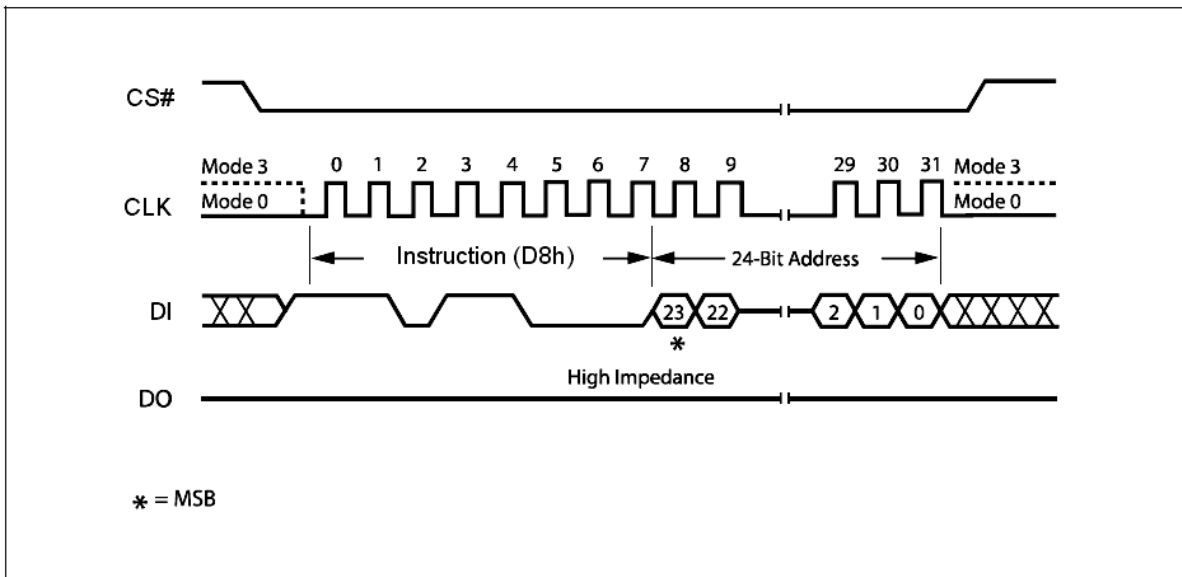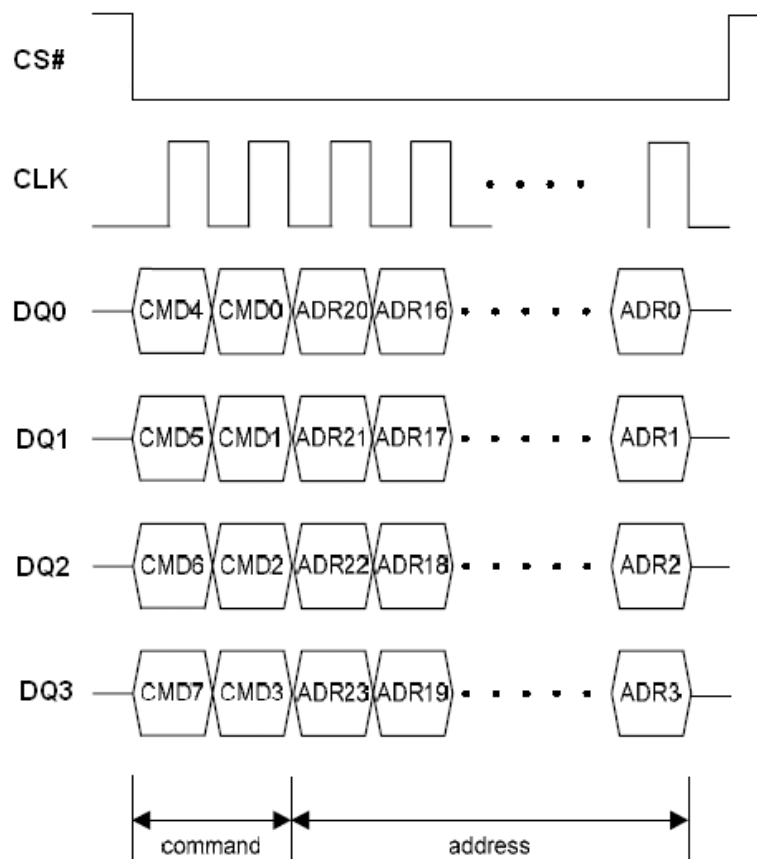
Block Erase (BE) (D8h)

The Block Erase (BE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Block Erase (BE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three address bytes on Serial Data Input (DI). Any address inside the Block (see Table 2) is a valid address for the Block Erase (BE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 18. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Block Erase (BE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Block Erase (BE) instruction applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 3) is not executed.

The instruction sequence is shown in Figure 18.1 while using the Enable Quad I/O (EQIO) (38h) command.

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Figure 18. Block Erase Instruction Sequence Diagram

Figure 18.1 Block/Sector Erase Instruction Sequence under EQIO Mode

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Chip Erase (CE) (C7h/60h)

The Chip Erase (CE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Chip Erase (CE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 19. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Chip Erase instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Chip Erase (CE) instruction is executed only if all Block Protect (BP2, BP1, BP0) bits are 0. The Chip Erase (CE) instruction is ignored if one, or more blocks are protected.

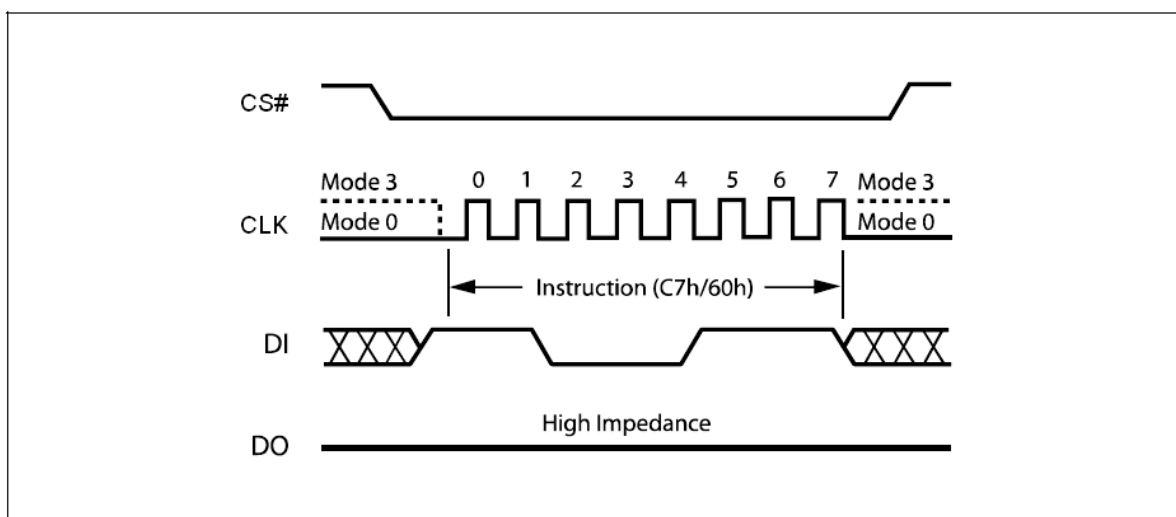The instruction sequence is shown in Figure 19.1 while using the Enable Quad I/O (EQIO) (38h) command.

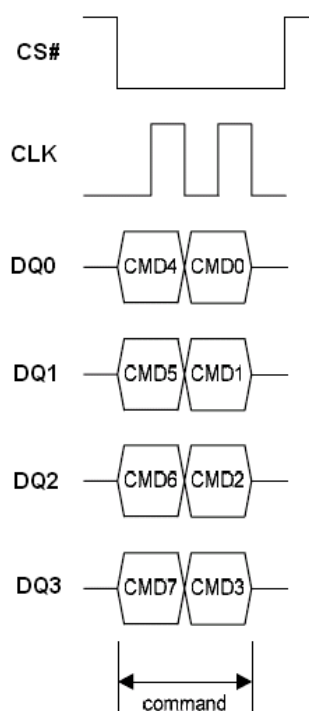**Figure 19. Chip Erase Instruction Sequence Diagram**

Figure 19.1 Chip Erase Sequence under EQIO Mode

Deep Power-down (DP) (B9h)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select (CS#) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in Table 9.)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Device ID (RDI) instruction also allows the Device ID of the device to be output on Serial Data Output (DO).

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode. The Deep Power-down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 20. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select (CS#) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.
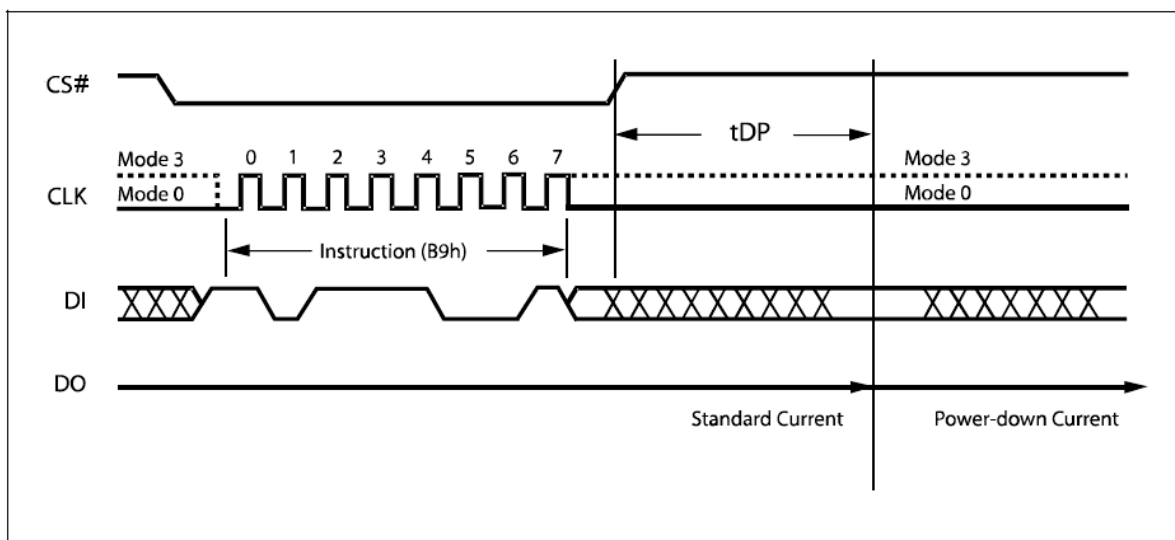
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Figure 20. Deep Power-down Instruction Sequence Diagram

Release from Deep Power-down and Read Device ID (RDI)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

Please note that this is not the same as, or even a subset of, the JEDEC 16-bit Electronic Signature that is read by the Read Identifier (RDID) instruction. The old-style Electronic Signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit Electronic Signature, and the Read Identifier (RDID) instruction.

When used only to release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code "ABh" and driving CS# high as shown in Figure 21. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code "ABh" followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 22. The Device ID value for the EN25Q80A are listed in Table 5. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by t_{RES2}, and Chip Select (CS#) must remain High for at least t_{RES2} (max), as specified in Table 11. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Device ID (RDI) instruction always provides access to the 8bit Device ID of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Device ID (RDI) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.
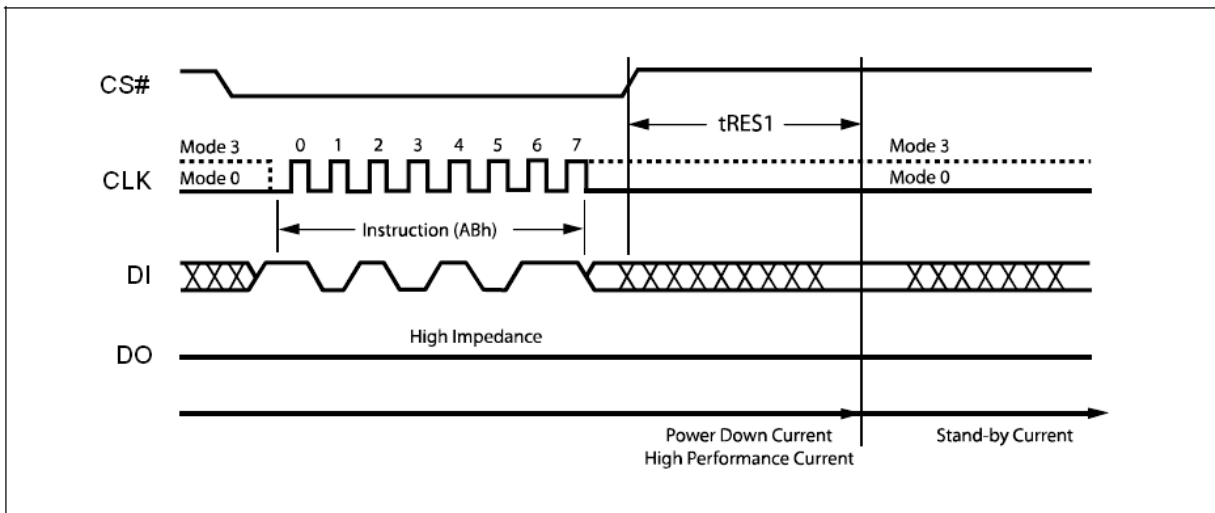
Figure 21. Release Power-down Instruction Sequence Diagram
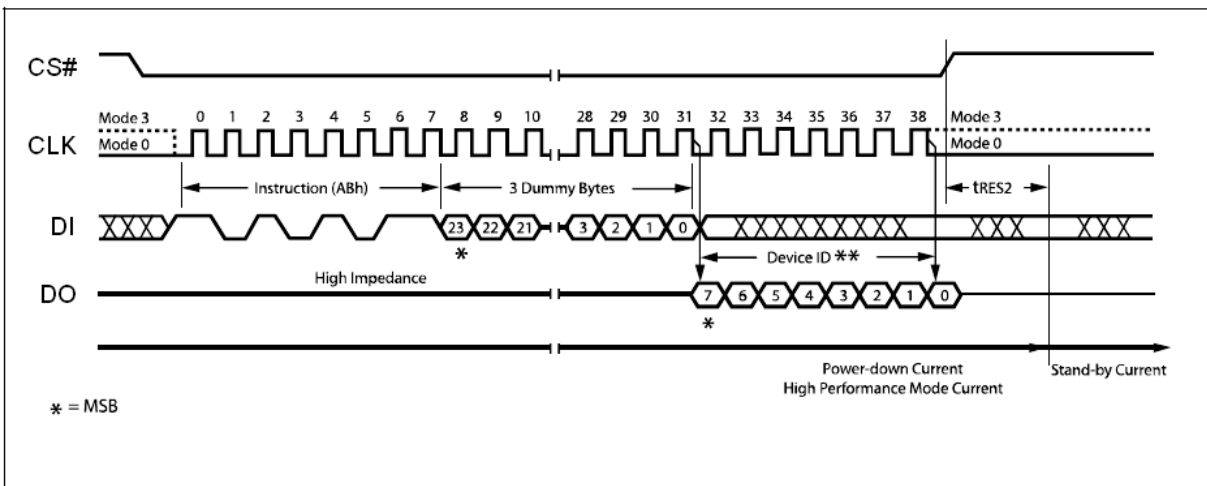
Figure 22. Release Power-down / Device ID Instruction Sequence Diagram

Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Eon (1Ch) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 23. The Device ID values for the EN25Q80A are listed in Table 5. If the 24-bit address is initially set to 000001h the Device ID will be read first

The instruction sequence is shown in Figure 23.1 while using the Enable Quad I/O (EQIO) (38h) command.

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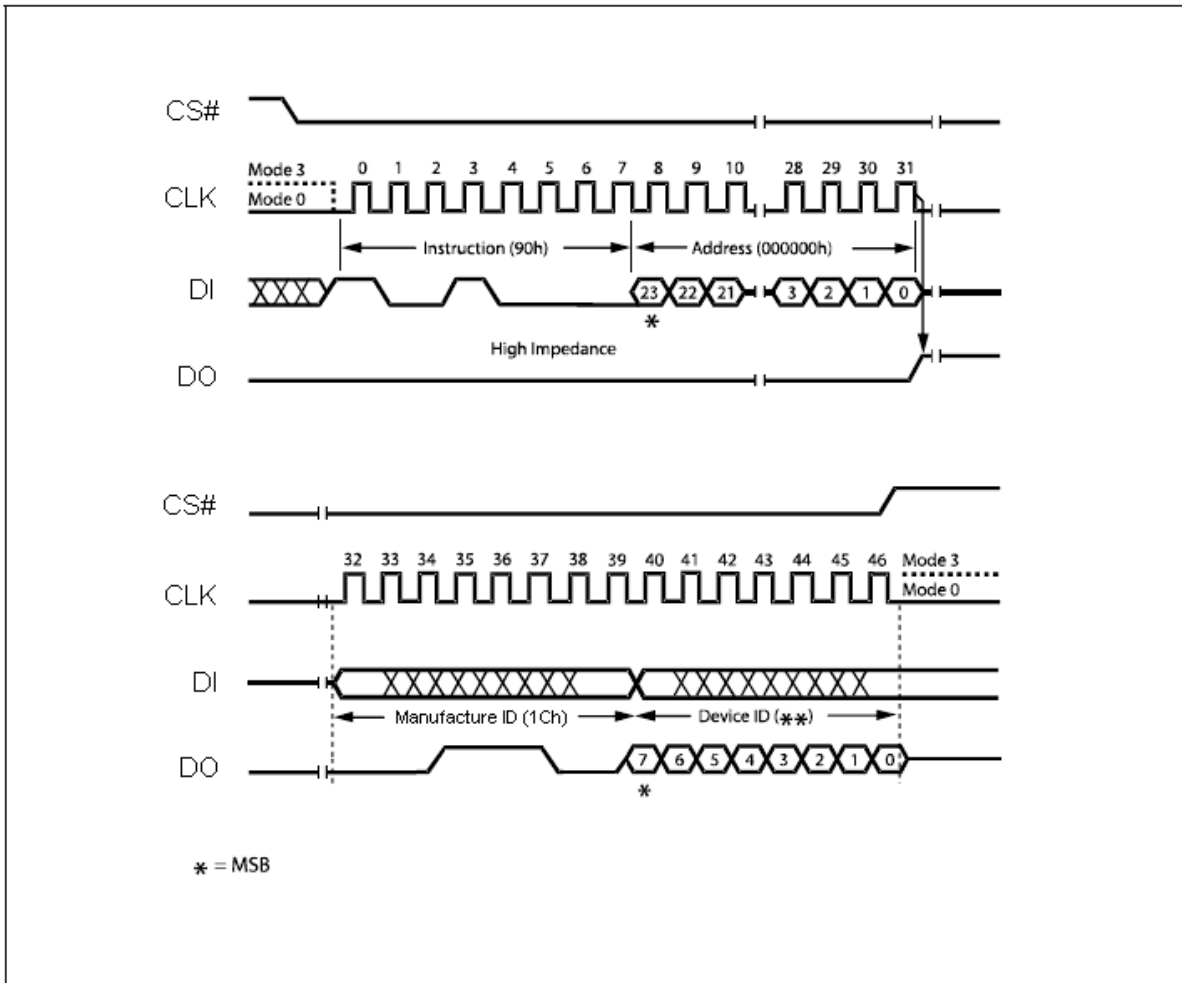
Figure 23. Read Manufacturer / Device ID Diagram
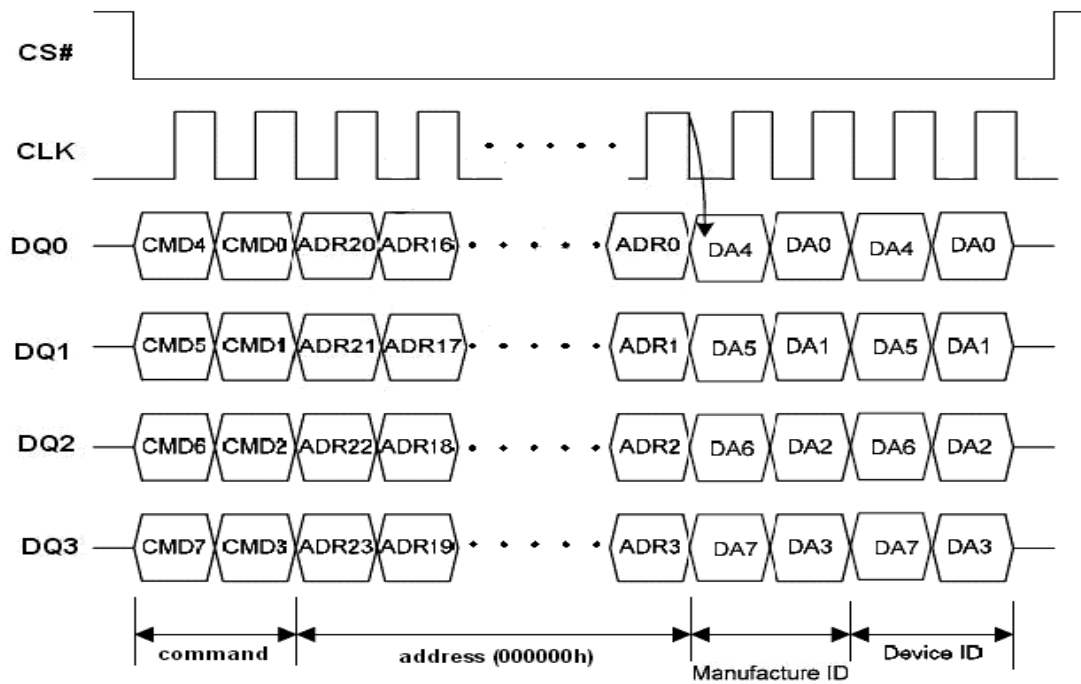
Figure 23.1. Read Manufacturer / Device ID Diagram under EQIO Mode

Read Identification (RDID) (9Fh)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte , and the memory capacity of the device in the second byte .

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) instruction should not be issued while the device is in Deep Power down mode.

The device is first selected by driving Chip Select Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output , each bit being shifted out during the falling edge of Serial Clock . The instruction sequence is shown in Figure 24. The Read Identification (RDID) instruction is terminated by driving Chip Select High at any time during data output.

When Chip Select is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

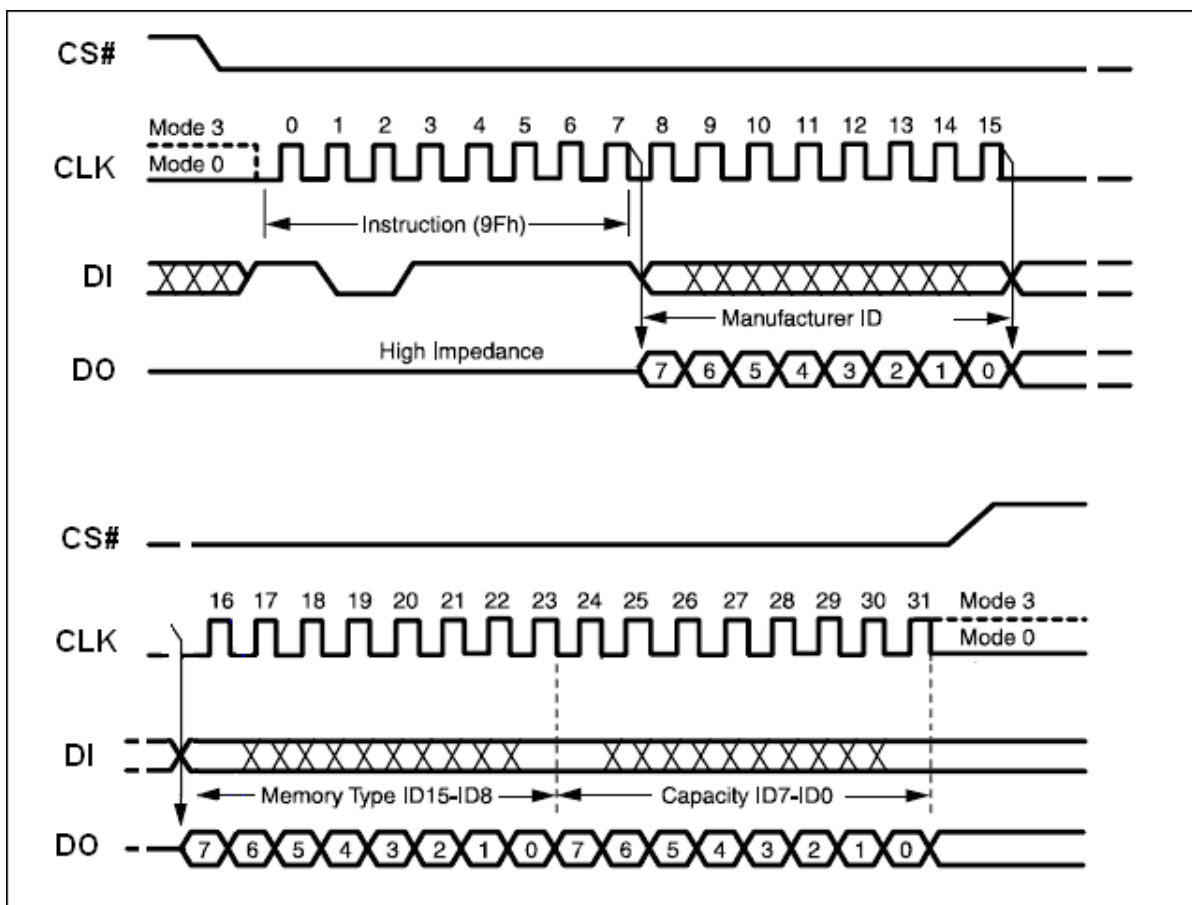The instruction sequence is shown in Figure 24.1 while using the Enable Quad I/O (EQIO) (38h) command.
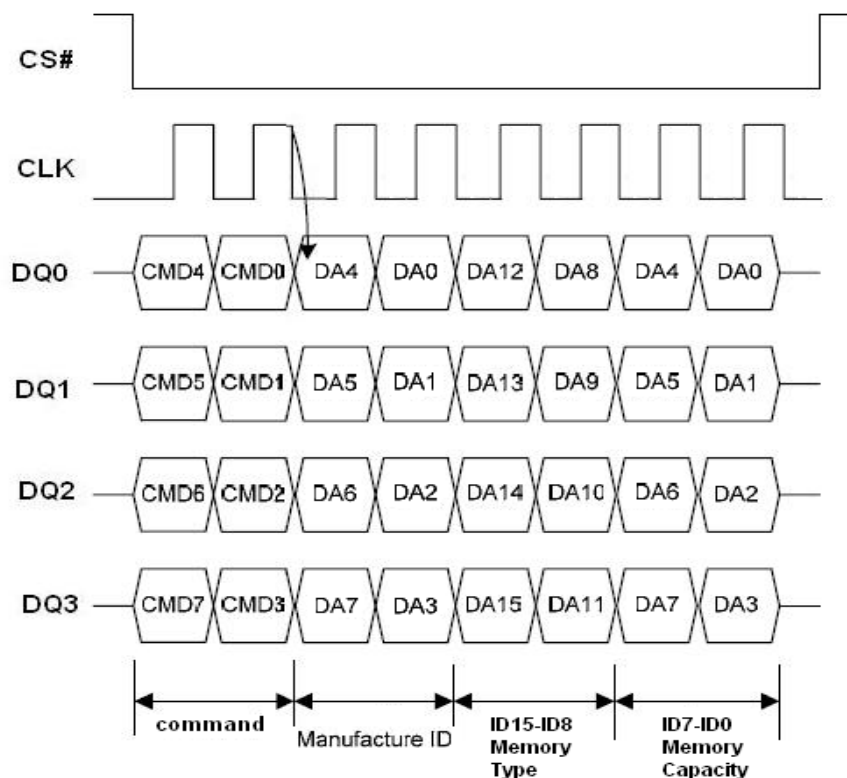

Figure 24. Read Identification (RDID)

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Figure 24.1. Read Identification (RDID) under EQIO Mode

Enter OTP Mode (3Ah)

This Flash has an extra 256 bytes OTP sector, user must issue ENTER OTP MODE command to read, program or erase OTP sector. After entering OTP mode, the OTP sector is mapping to sector 255, **SRP bit** becomes OTP_LOCK bit and can be read with RDSR command. Program / Erase command will be disabled when OTP_LOCK bit is '1'

WRSR command will ignore the input data and program OTP_LOCK bit to 1.
User must clear the protect bits before enter OTP mode.
OTP sector can only be program and erase before OTP_LOCK bit is set to '1' and BP [2:0] = '000'. In OTP mode, user can read other sectors, but program/erase other sectors only allowed when OTP_LOCK bit equal to '0'.

User can use WRDI (04h) command to exit OTP mode.

The instruction sequence is shown in Figure 25.1 while using the Enable Quad I/O (EQIO) (38h) command.
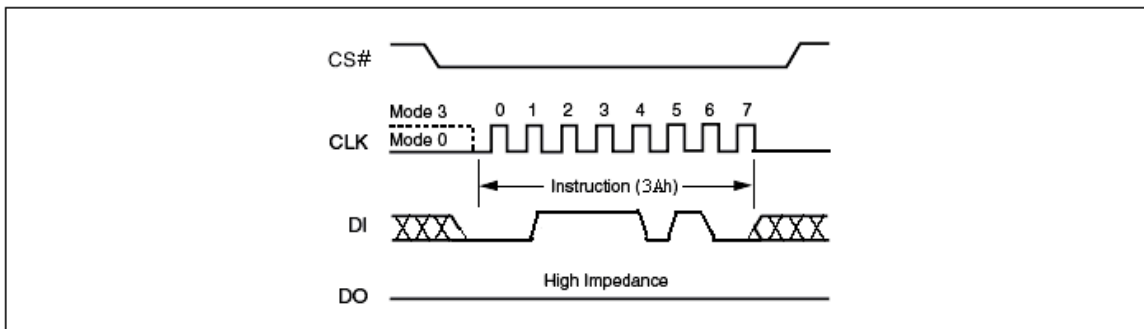
Erase OTP Command (20h)

User can use Sector Erase (20h) command only to erase OTP data.

Table 7. OTP Sector Address

Sector	Sector Size	Address Range
255	256 byte	0FF000h – 0FF0FFh

Note: The OTP sector is mapping to sector 255

Figure 25. Enter OTP Mode
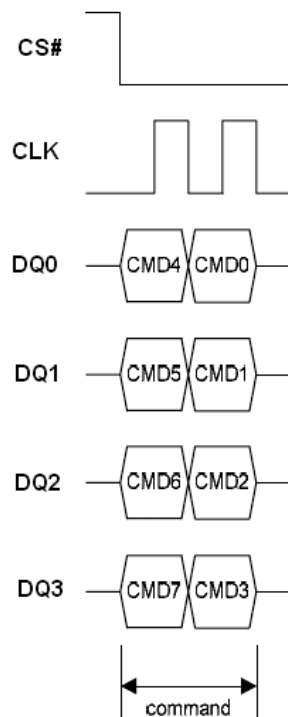
Figure 25.1 Enter OTP Mode Sequence under EQIO Mode

Power-up Timing
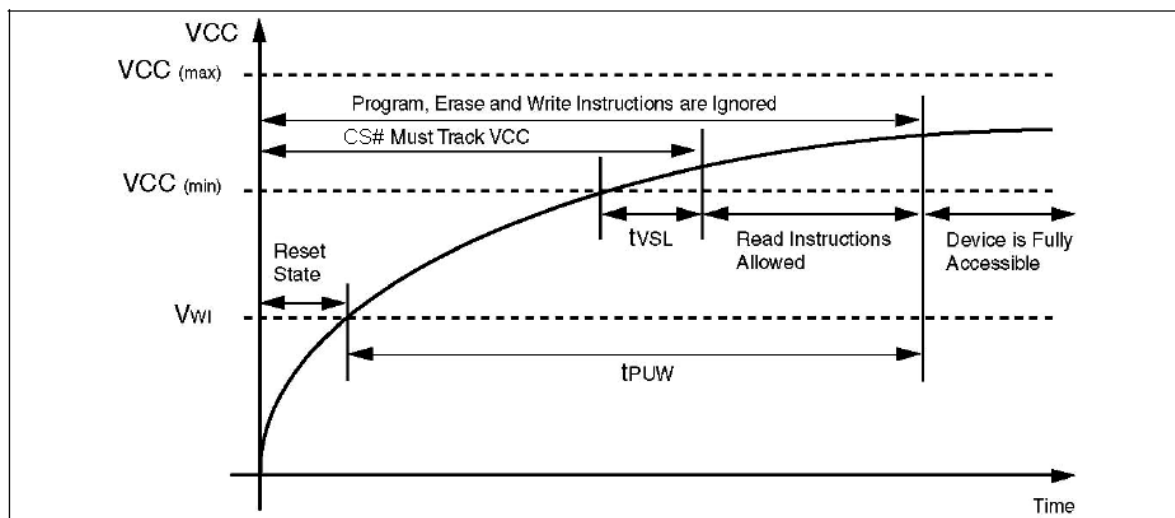
Figure 26. Power-up Timing

Table 8. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}(1)	VCC(min) to CS# low	10		µs
t_{PUW}(1)	Time delay to Write instruction	1	10	ms
V_{WI}(1)	Write Inhibit Voltage	1	2.5	V

Note:
1.The parameters are characterized only.
2. VCC (max.) is 3.6V and VCC (min.) is 2.7V

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Table 9. DC Characteristics

(T_a = - 40°C to 85°C; V_{CC} = 2.7-3.6V)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current			± 2	µA
I_{LO}	Output Leakage Current			± 2	µA
I_{CC1}	Standby Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}		20	µA
I_{CC2}	Deep Power-down Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}		20	µA
I_{CC3}	Operating Current (READ)	CLK = 0.1 V_{CC} / 0.9 V_{CC} at 100MHz, DQ = open		25	mA
		CLK = 0.1 V_{CC} / 0.9 V_{CC} at 80MHz, DQ = open		20	mA
I_{CC4}	Operating Current (PP)	CS# = V_{CC}		28	mA
I_{CC5}	Operating Current (WRSR)	CS# = V_{CC}		18	mA
I_{CC6}	Operating Current (SE)	CS# = V_{CC}		25	mA
I_{CC7}	Operating Current (BE)	CS# = V_{CC}		25	mA
V_{IL}	Input Low Voltage		− 0.5	0.2 V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = −100 µA	V_{CC}-0.2		V

Table 10. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	20/30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}		V
	Input Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}		V
	Output Timing Reference Voltages	V_{CC} / 2		V

Notes:
1. C_L = 20 pF when CLK=100MHz, C_L = 30 pF when CLK = 80MHz,
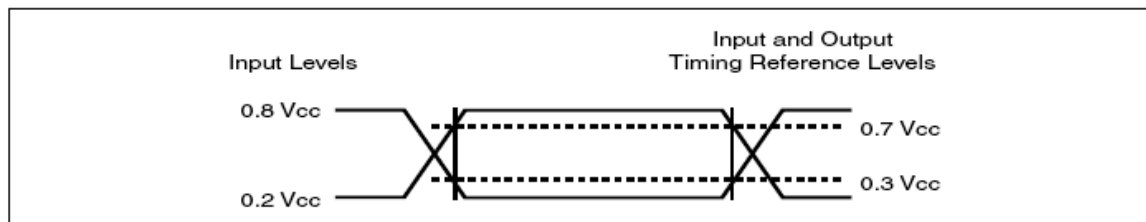
Figure 27. AC Measurement I/O Waveform

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Table 11. AC Characteristics

$(T_a = -40°C \text{ to } 85°C; V_{CC} = 2.7\text{-}3.6V)$

Symbol	Alt	Parameter	Min	Typ	Max	Unit
F_R	f_C	Serial Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, WRSR	D.C.		100	MHz
		Serial Clock Frequency for: Dual Output Fast Read and Quad I/O Fast Read	D.C.		80	MHz
f_R		Serial Clock Frequency for READ, RDSR, RDID	D.C.		50	MHz
t_{CH}[1]		Serial Clock High Time	4			ns
t_{CL}[1]		Serial Clock Low Time	4			ns
t_{CLCH}[2]		Serial Clock Rise Time (Slew Rate)	0.1			V / ns
t_{CHCL}[2]		Serial Clock Fall Time (Slew Rate)	0.1			V / ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time	5			ns
t_{CHSH}		CS# Active Hold Time	5			ns
t_{SHCH}		CS# Not Active Setup Time	5			ns
t_{CHSL}		CS# Not Active Hold Time	5			ns
t_{SHSL}	t_{CSH}	CS# High Time for read CS# High Time for program/erase	15 50			ns ns
t_{SHQZ}[2]	t_{DIS}	Output Disable Time			6	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	2			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{CLQV}	t_V	Output Valid from CLK			8	ns
t_{WHSL}[3]		Write Protect Setup Time before CS# Low	20			ns
t_{SHWL}[3]		Write Protect Hold Time after CS# High	100			ns
t_{DP}[2]		CS# High to Deep Power-down Mode			3	µs
t_{RES1}[2]		CS# High to Standby Mode without Electronic Signature read			3	µs
t_{RES2}[2]		CS# High to Standby Mode with Electronic Signature read			1.8	µs
t_W		Write Status Register Cycle Time		10	15	ms
t_{PP}		Page Programming Time		1.3	5	ms
t_{SE}		Sector Erase Time		0.09	0.3	s
t_{BE}		Block Erase Time		0.5	2	s
t_{CE}		Chip Erase Time		8	20	s

Note: 1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/f_C$

2. Value guaranteed by characterization, not 100% tested in production.

3. Only applicable as a constraint for a Write status Register instruction when Status Register Protect Bit is set at 1.

This Data Sheet may be revised by subsequent versions or modifications due to changes in technical specifications.

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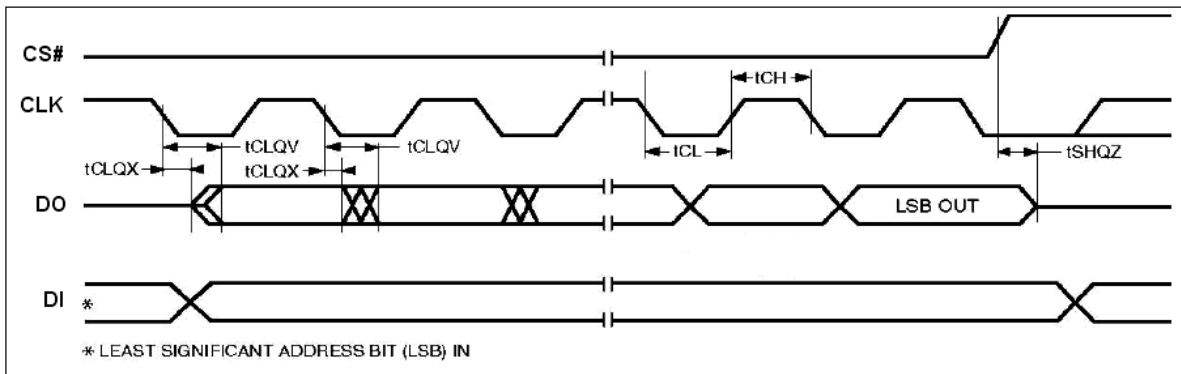
Figure 28. Serial Output Timing
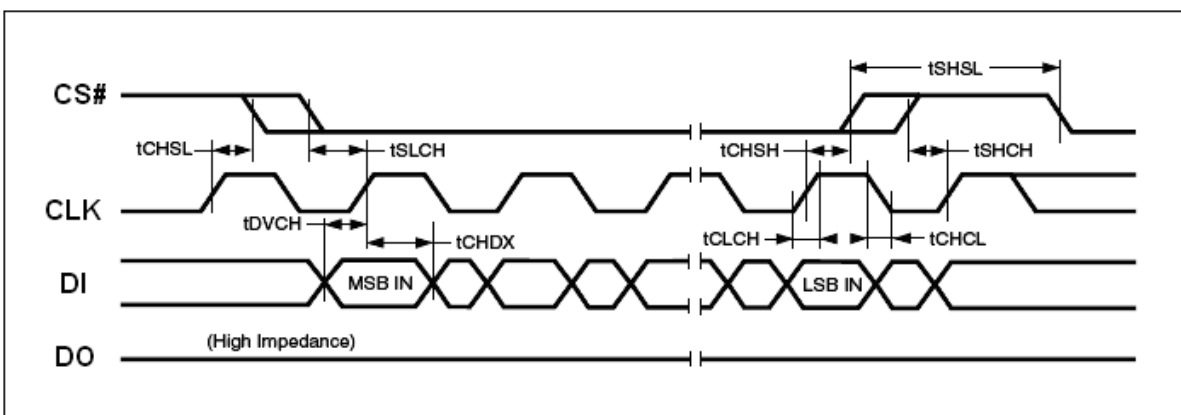
Figure 29. Input Timing

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ABSOLUTE MAXIMUM RATINGS

Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

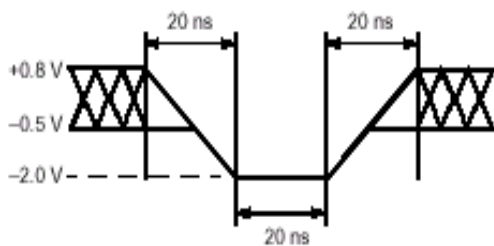| Parameter	Value	Unit
Storage Temperature	-65 to +150	°C
Plastic Packages	-65 to +125	°C
Output Short Circuit Current[1]	200	mA
Input and Output Voltage (with respect to ground) [2]	-0.5 to +4.0	V
Vcc	-0.5 to +4.0	V

Notes:
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC voltage on input or I/O pins is -0.5 V. During voltage transitions, inputs may undershoot V_{ss} to -1.0V for periods of up to 50ns and to -2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is $V_{cc} + 0.5$ V. During voltage transitions, outputs may overshoot to $V_{cc} + 1.5$ V for periods up to 20ns. See figure below.

RECOMMENDED OPERATING RANGES [1]

Parameter	Value	Unit
Ambient Operating Temperature Industrial Devices	-40 to 85	°C
Operating Supply Voltage Vcc	Full: 2.7 to 3.6	V

Notes:
1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.

Maximum Negative Overshoot Waveform
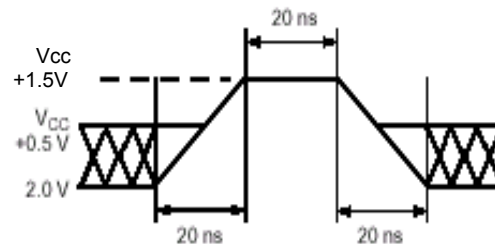
Maximum Positive Overshoot Waveform

This Data Sheet may be revised by subsequent versions or modifications due to changes in technical specifications.

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Table 12. DATA RETENTION and ENDURANCE

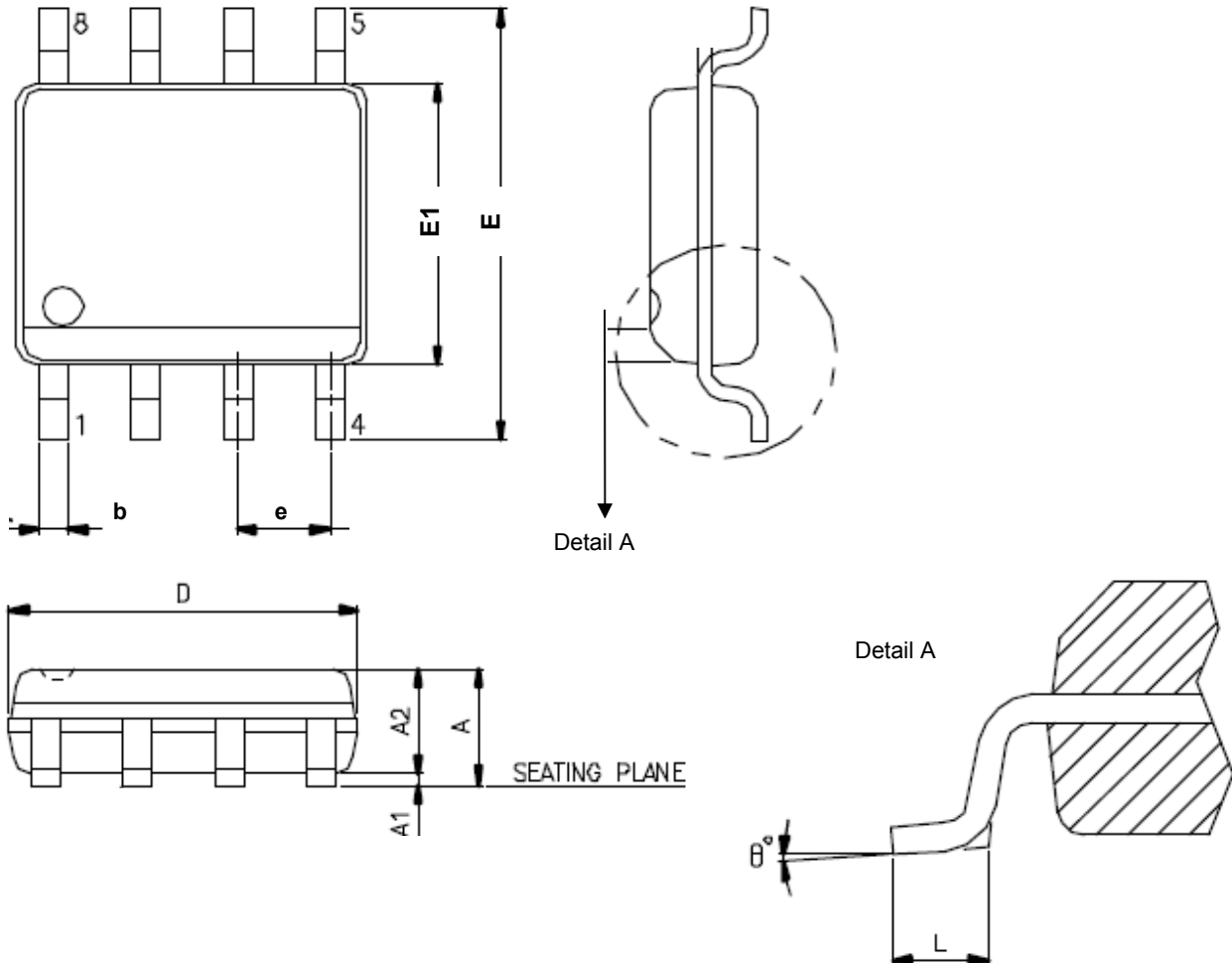| Parameter Description	Test Conditions	Min	Unit
Data Retention Time	150°C	10	Years
	125°C	20	Years
Erase/Program Endurance	-40 to 85 °C	100k	cycles

Table 13. CAPACITANCE

(V_{CC} = 2.7-3.6V)

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0		8	pF

Note : Sampled only, not 100% tested, at T_A = 25°C and a frequency of 20MHz.

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PACKAGE MECHANICAL

Figure 30. SOP 8 (150 mil)

Detail A

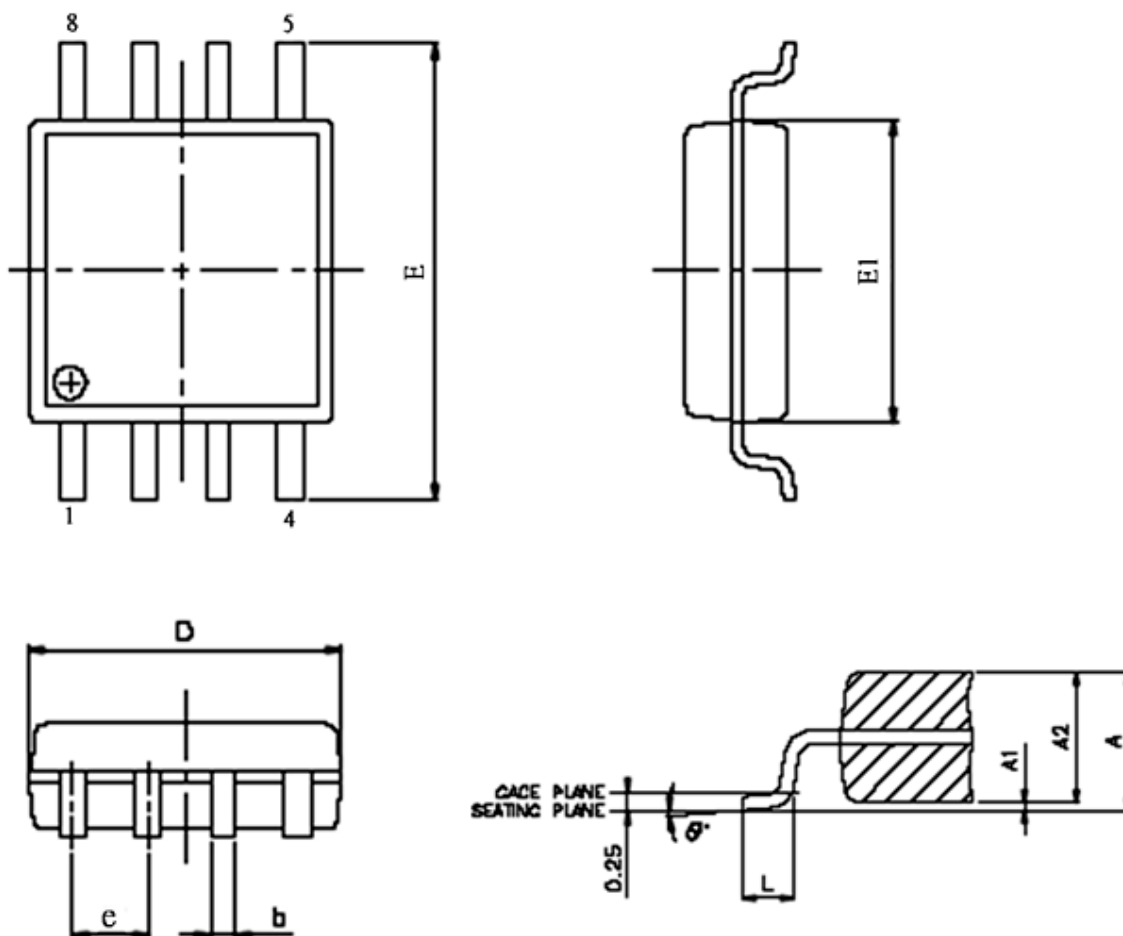| SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	1.35	- - -	1.75
A1	0.10	- - -	0.25
A2	- - -	- - -	1.50
D	4.80	- - -	5.00
E	5.80	- - -	6.20
E1	3.80	- - -	4.00
e	- - -	1.27	- - -
b	0.33	- - -	0.51
L	0.4	- - -	1.27
θ	0^0	- - -	8^0

Note : 1. Coplanarity: 0.1 mm
2. Max. allowable mold flash is 0.15 mm
at the pkg ends, 0.25 mm between leads.

Figure 31. VSOP 8 (150 mil)
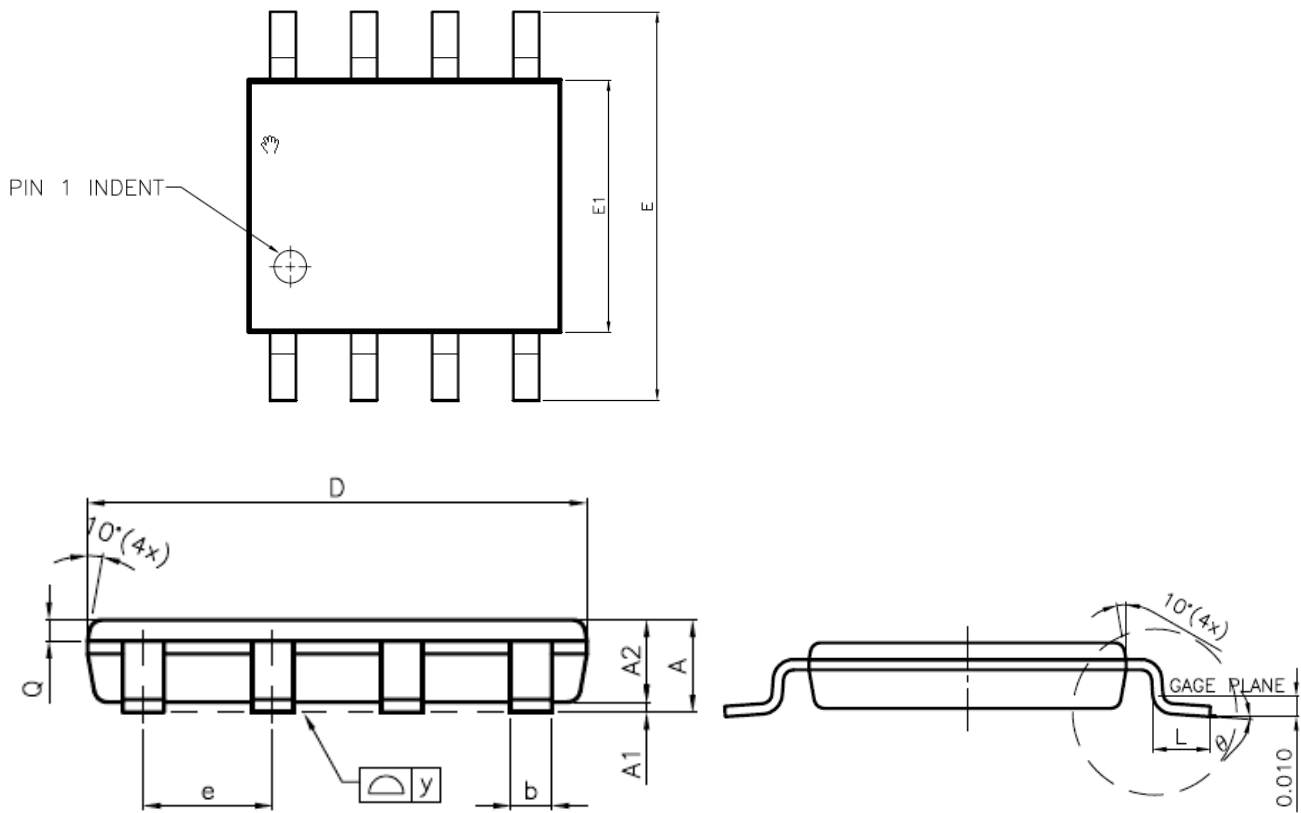
SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	--	--	0.90
A1	0.05	0.10	0.15
A2	0.65	0.70	0.75
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	- - -	1.27	- - -
b	0.33	0.41	0.51
L	0.40	0.71	1.27
θ	0	--	10

Note : 1. Coplanarity: 0.1 mm
2. Max. allowable mold flash is 0.15 mm
at the pkg ends, 0.25 mm between leads.

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Figure 32. SOP 200 mil (official name = 208 mil)

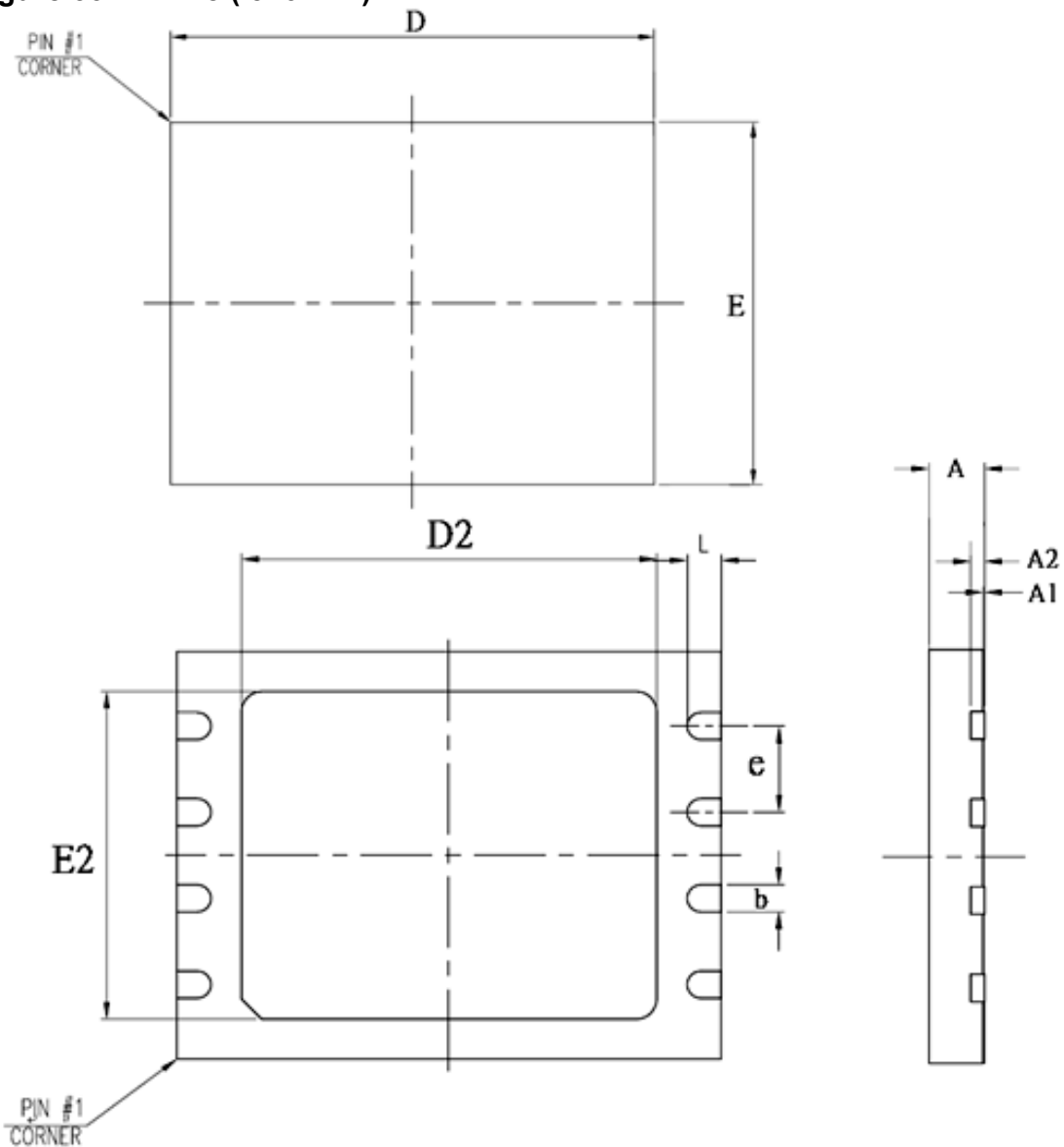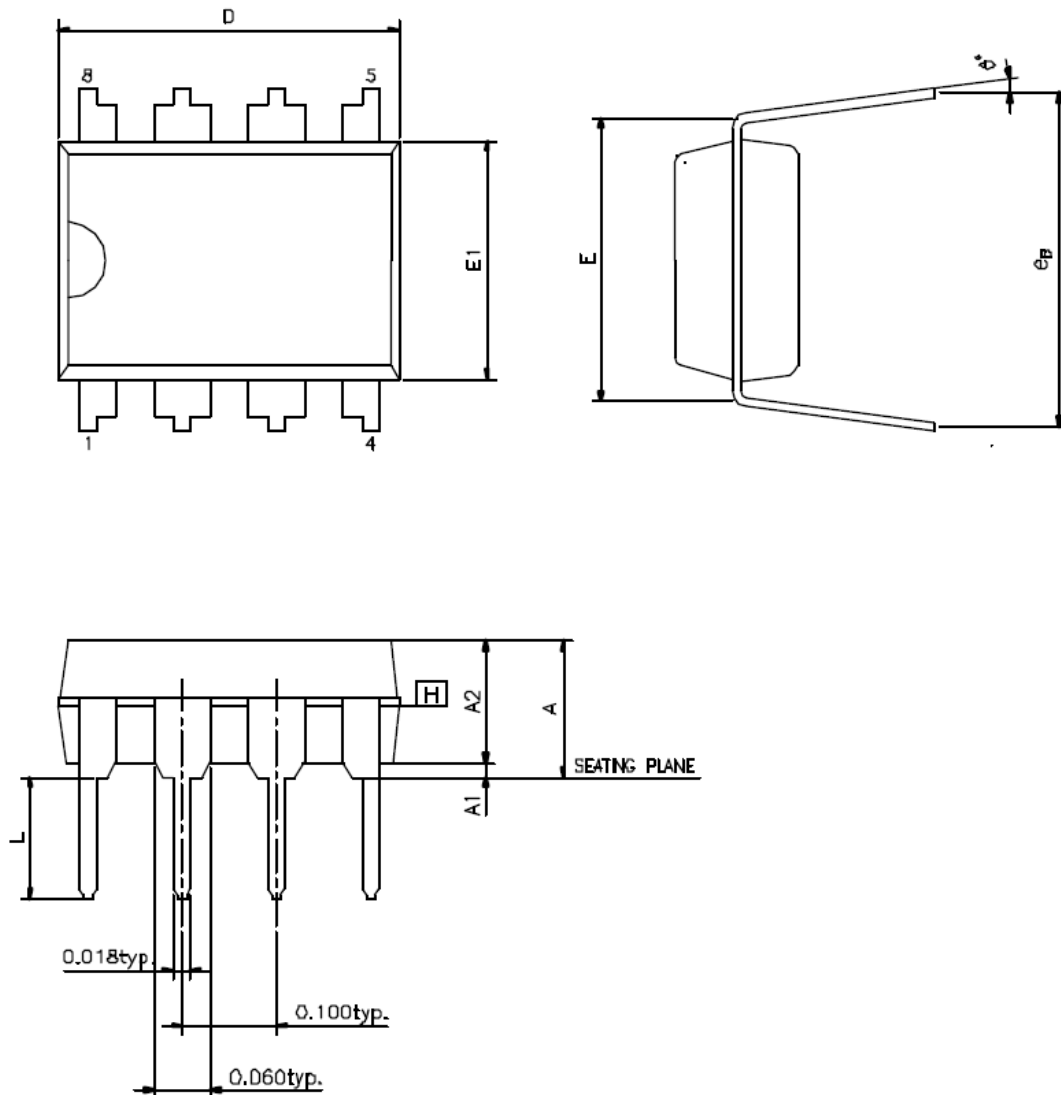| SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	1.75	1.975	2.20
A1	0.05	0.15	0.25
A2	1.70	1.825	1.95
D	5.15	5.275	5.40
E	7.70	7.90	8.10
E1	5.15	5.275	5.40
e	- - -	1.27	- - -
b	0.35	0.425	0.50
L	0.5	0.65	0.80
θ	0^0	4^0	8^0

Note : 1. Coplanarity: 0.1 mm
2. Max. allowable mold flash is 0.15 mm
at the pkg ends, 0.25 mm between leads.

Figure 33. VDFN8 (5x6mm)

Controlling dimensions are in millimeters (mm).

SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.04
A2	- - -	0.20	- - -
D	5.90	6.00	6.10
E	4.90	5.00	5.10
D2	3.30	3.40	3.50
E2	3.90	4.00	4.10
e	- - -	1.27	- - -
b	0.35	0.40	0.45
L	0.55	0.60	0.65

Note : 1. Coplanarity: 0.1 mm

Figure 34. PDIP8

SYMBOL	DIMENSION IN INCH		
	MIN.	NOR	MAX
A	- - -	- - -	0.210
A1	0.015	- - -	- - -
A2	0.125	0.130	0.135
D	0.355	0.365	0.400
E	0.300	0.310	0.320
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.310	0.350	0.375
Θ^0	0	7	15

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Figure 35. 24-ball Thin Profile Fine-Pitch Ball Grid Array (6 x 8 mm) Package
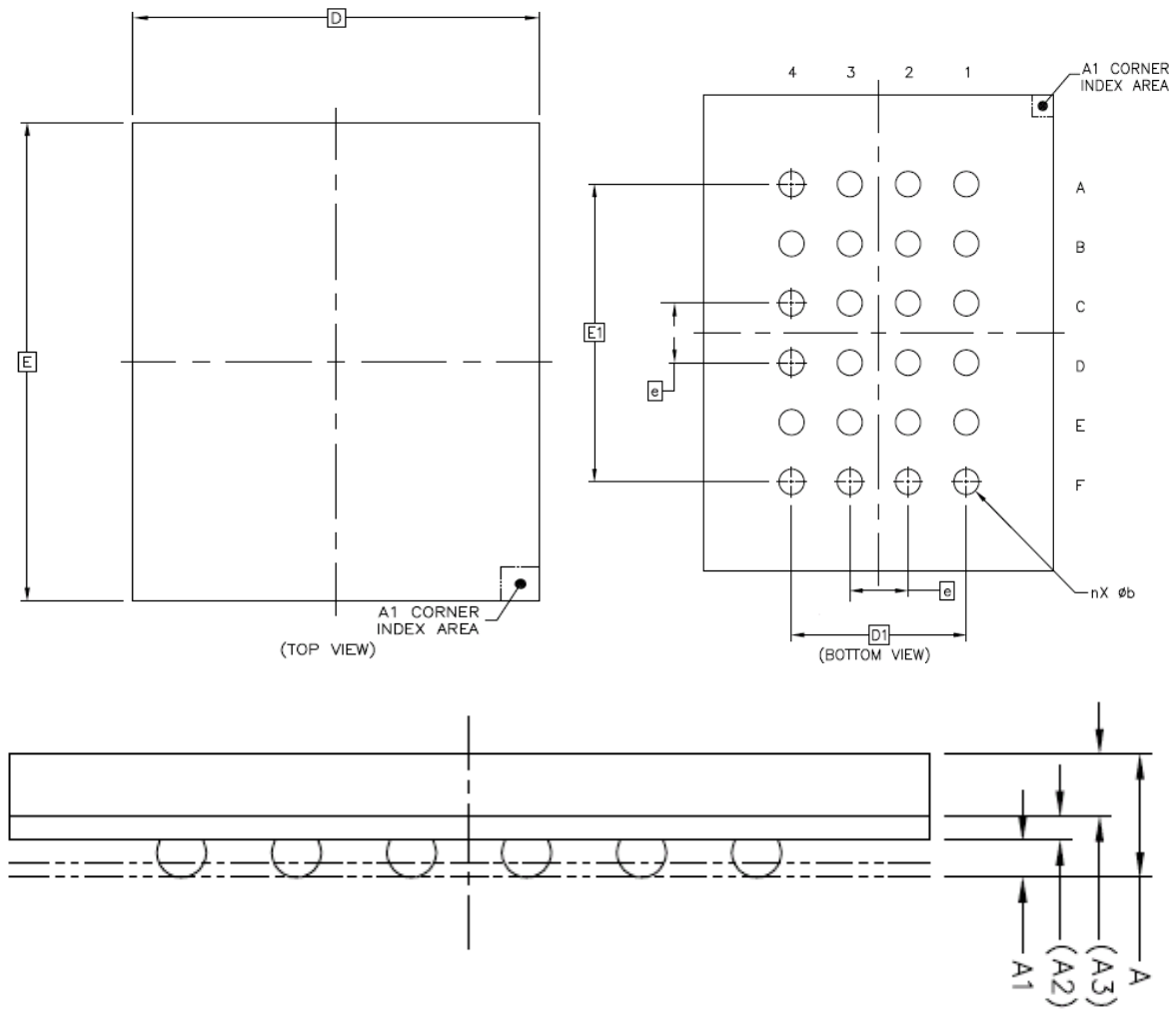
SYMBOL	DIMENSION IN MM		
	MIN.	NOR.	MAX
A	- - -	- - -	1.20
A1	0.27	- - -	0.37
A2	0.21 REF		
A3	0.54 REF		
D	6 BSC		
E	8 BSC		
D1	- - -	3.00	- - -
E1	- - -	5.00	- - -
e	- - -	1.00	- - -
b	- - -	0.40	- - -

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Purpose

Eon Silicon Solution Inc. (hereinafter called "Eon") is going to provide its products' top marking on ICs with < cFeon > from January 1st, 2009, and without any change of the part number and the compositions of the ICs. Eon is still keeping the promise of quality for all the products with the same as that of Eon delivered before. Please be advised with the change and appreciate your kindly cooperation and fully support Eon's product family.

Eon products' New Top Marking

cFeon

cFeon Top Marking Example:

> **cFeon**
>
> **Part Number: XXXX-XXX**
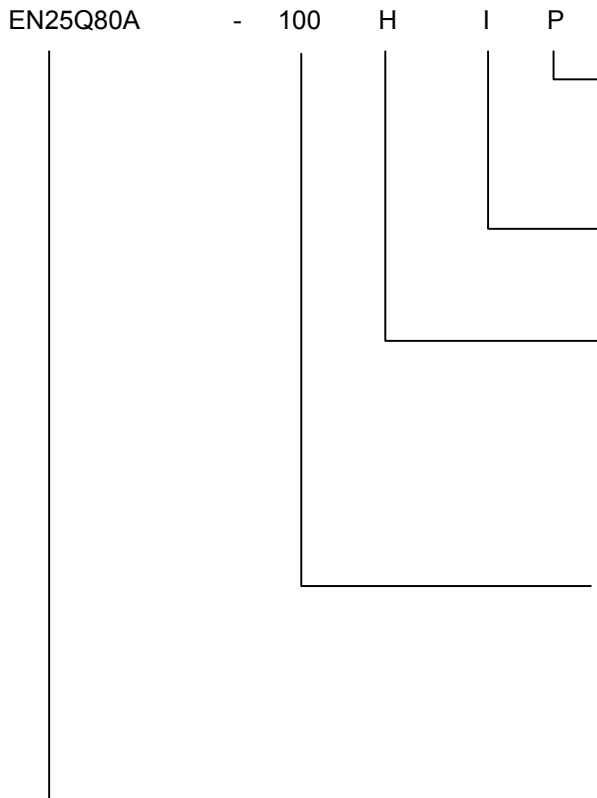> **Lot Number: XXXXX**
> **Date Code: XXXXX**

For More Information

Please contact your local sales office for additional information about Eon memory solutions.

ORDERING INFORMATION

EN25Q80A   - 100   H   I   P

PACKAGING CONTENT
P = RoHS compliant

TEMPERATURE RANGE
 I = Industrial (-40°C to +85°C)

PACKAGE
G = 8-pin 150mil SOP
RB = 8-pin 150mil VSOP
H = 8-pin 200mil SOP
W = 8-pin VDFN
Q = 8-pin PDIP
BB = 24-ball TFBGA (6 x 8 x 1.2mm)

SPEED
100 = 100 Mhz

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
25Q = 3V Serial Flash with 4KB Uniform-Sector,
        Dual and Quad I/O
80A = 8 Megabit (1024K x 8)

Revisions List

Revision No	Description	Date
A	Initial Release	2009/01/16
B	Remove the Block Erase "52h" command on page 9, 22 and 23.	2009/04/06

C	1. Update Page program Block and Chip erase time (typ.) parameter on page 1 and 39.
	   (1). Block erase: from 0.4s to 0.5s
	   (2). Chip erase: from 2s to 3.5s
	2. Add Figure 4. Quad SPI Modes on page 7.
	3. Update the Protected Area Sizes definition of BP2、BP1 and BP0 in table 3 on page 8.
	4. Add the description of OTP erase command on page 9 and page 35.
	5. Add Figure 7.1 Write Enable/Disable Instruction Sequence under EQIO Mode on page 14.
	6. Add Figure 8.1 Read Status Register Instruction Sequence under EQIO Mode on page 15.
	7. Add Figure 9.1 Write Status Register Instruction Sequence under EQIO Mode on page 17.
	8. Add Figure 11.1 Fast Read Instruction Sequence under EQIO Mode on page 19.
	9. Add Figure 14.1. Quad Input / Output Fast Read Instruction Sequence under EQIO Mode on page 23.
	10. Add Figure 15.1 Quad Input/Output Fast Read Enhance Performance Mode Sequence under EQIO Mode on page 25.
	11. Add Figure 16.1 Program Instruction Sequence under EQIO Mode on page 27.
	12. Add Figure 18.1 Block/Sector Erase Instruction Sequence under EQIO Mode on page 29.
	13. Add Figure 19.1 Chip Erase Sequence under EQIO Mode on page 31.
	14. Add Figure 23.1. Read Manufacturer / Device ID Diagram under EQIO Add Mode on page 34.
	15. Add Figure 24.1. Read Identification (RDID) under EQIO Mode on page 36.
	16. Add Figure 25.1 Enter OTP Mode Sequence under EQIO Mode on page 37.
	17. Modify t_{CSH} CS# High Time from 100ns to 15ns for read and 50ns for program/erase in Table 11 on page 40
		2009/07/27

D	Modify Table 9. DC Characteristics I_{CC1} (Standby) and I_{CC2} (Deep Power-down) Current from 5μA to 20μA on page 39.	2009/10/13
E	Revise the description of Reset Quad I/O (FFh) command on page 12.	2010/07/19
F	Correct the typo of 6 dummy clocks for EBh command on page 22.	2011/07/14
G	Add 24 balls TFBGA (6x8mm) package.	2012/03/12
H	Add 8-pin 150mil VSOP package option.	2012/10/23

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