EN25QH256
256 Megabit Serial Flash Memory with 4Kbyte Uniform Sector

FEATURES

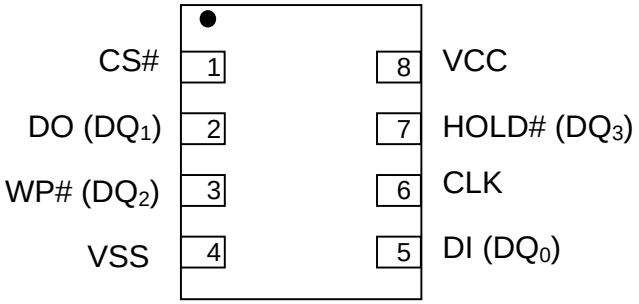
- Single power supply operation
  - Full voltage range: 2.7-3.6 volt
- Serial Interface Architecture
  - SPI Compatible: Mode 0 and Mode 3
- 256 M-bit Serial Flash
  - 256 M-bit/32,768 K-byte/131,072 pages
  - 256 bytes per programmable page
- Standard, Dual or Quad SPI
  - Standard SPI: CLK, CS#, DI, DO, WP#, HOLD#
  - Dual SPI: CLK, CS#, DQ_0, DQ_1, WP#, HOLD#
  - Quad SPI: CLK, CS#, DQ_0, DQ_1, DQ_2, DQ_3
- High performance
  - 80MHz clock rate for Standard SPI
  - 80MHz clock rate for two data bits
  - 50MHz clock rate for four data bits
- Low power consumption
  - 12 mA typical active current
  - 1 μA typical power down current
- Uniform Sector Architecture:
  - 8192 sectors of 4-Kbyte
  - 512 blocks of 64-Kbyte
  - Any sector or block can be erased individually
- Software and Hardware Write Protection:
  - Write Protect all or portion of memory via software
  - Enable/Disable protection with WP# pin
- High performance program/erase speed
  - Page program time: 0.8ms typical
  - Sector erase time: 50ms typical
  - Block erase time 400ms typical
  - Chip erase time: 100 seconds typical
- Lockable 512 byte OTP security sector
- Support Serial Flash Discoverable Parameters (SFDP) signature
- Read Unique ID Number
- Support High Bank Latch Mode
- Minimum 100K endurance cycle
- Package Options
  - 8 contact VDFN (6x8mm)
  - 16 pins SOP 300mil body width
  - 24 balls BGA (6x8mm)
  - All Pb-free packages are RoHS compliant
- Industrial temperature Range

GENERAL DESCRIPTION

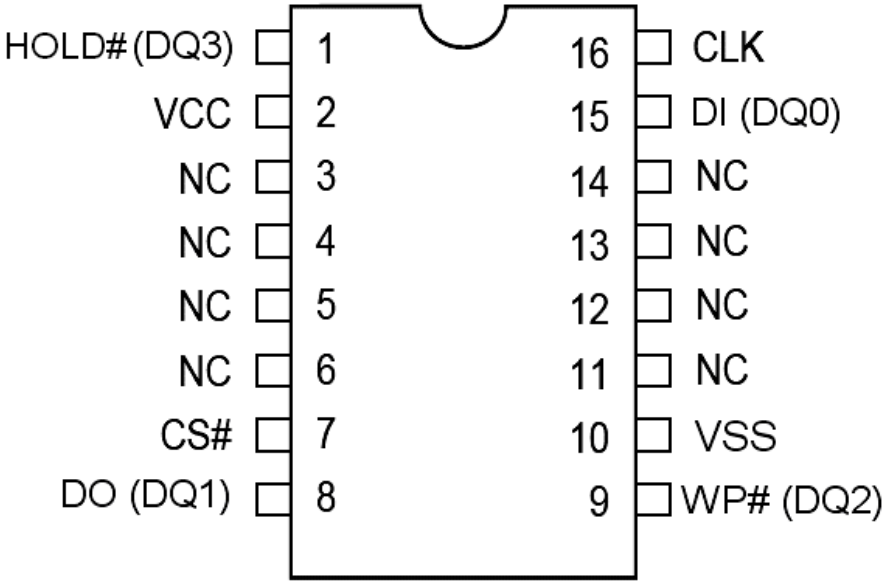
The EN25QH256 is a 256 Megabit (32,768 K-byte) Serial Flash memory, with enhanced write protection mechanisms. The EN25QH256 supports the standard Serial Peripheral Interface (SPI), and a high performance Dual/Quad output as well as Dual/Quad I/O using SPI pins: Serial Clock, Chip Select, Serial DQ_0(DI), DQ_1(DO), DQ_2(WP#) and DQ_3(HOLD#). SPI clock frequencies of up to 80MHz are supported allowing equivalent clock rates of 160MHz (80MHz x 2) for Dual Output when using the Dual Output Fast Read instructions, and SPI clock frequencies of up to 50MHz are supported allowing equivalent clock rates of 200MHz (50MHz x 4) for Quad Output when using the Quad Output Fast Read instructions. The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.

The EN25QH256 is designed to allow either single Sector/Block at a time or full chip erase operation. The EN25QH256 can be configured to protect part of the memory as the software protected mode. The device can sustain a minimum of 100K program/erase cycles on each sector or block.

Figure.1 CONNECTION DIAGRAMS

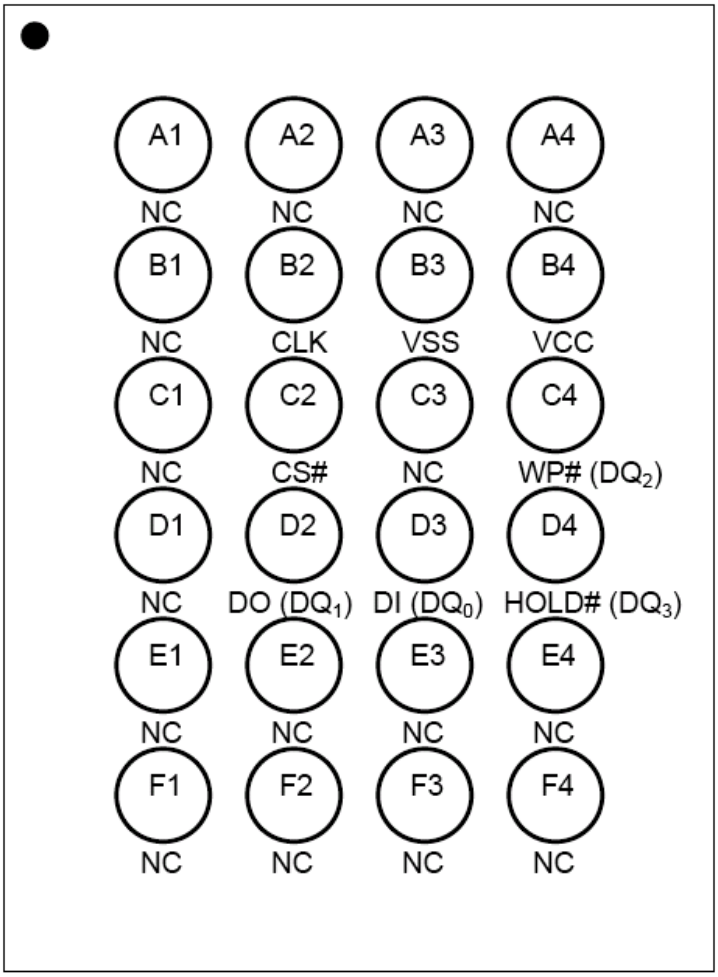


8 - LEAD VDFN



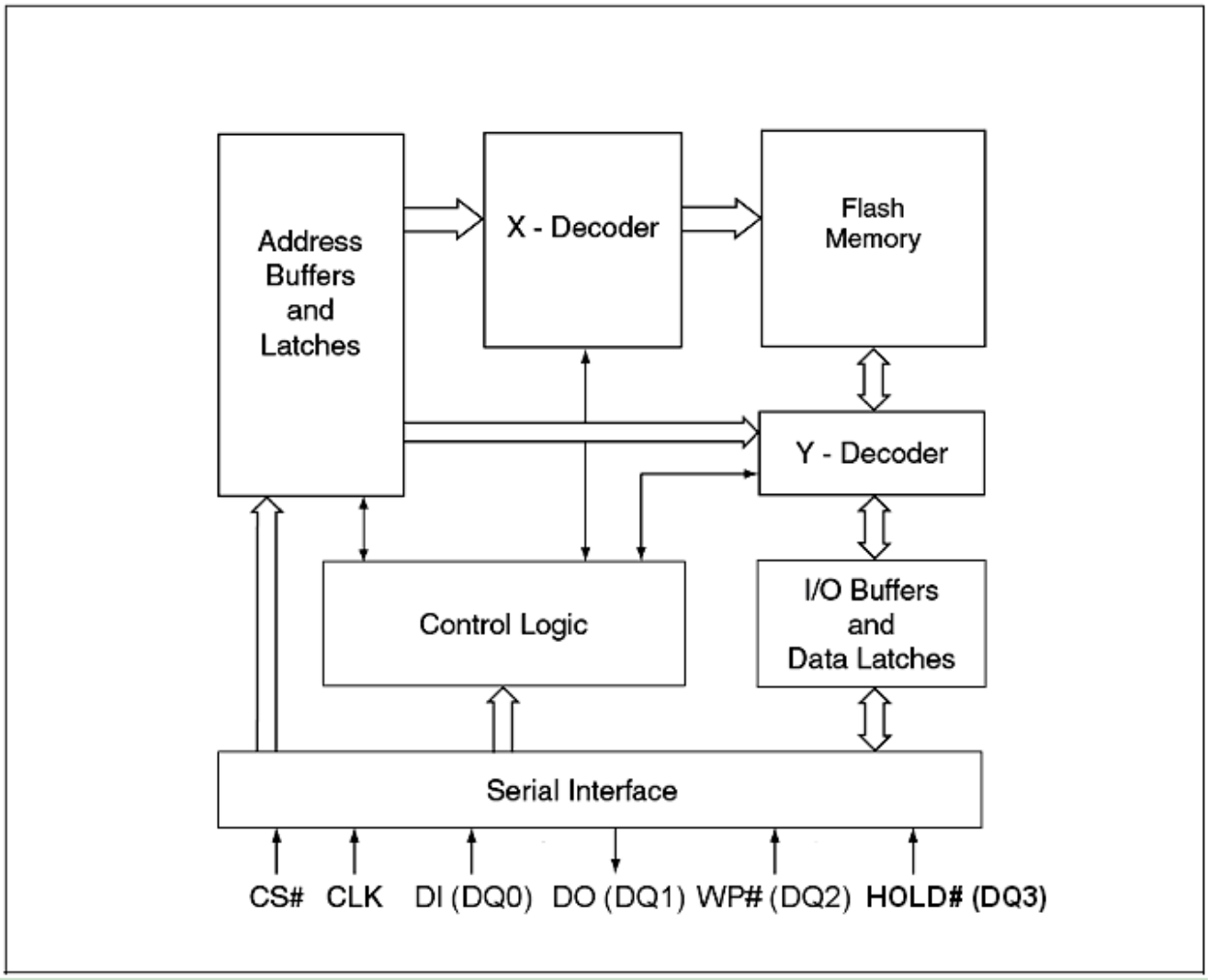
16 - LEAD SOP

Top View, Balls Facing Down



24 - Ball BGA

Figure 2. BLOCK DIAGRAM



Note:
1. DQ_0 and DQ_1 are used for Dual and Quad instructions.
2. DQ_0 ~ DQ_3 are used for Quad instructions.

Table 1. Pin Names

Symbol	Pin Name
CLK	Serial Clock Input
DI (DQ_0)	Serial Data Input (Data Input Output 0) *1
DO (DQ_1)	Serial Data Output (Data Input Output 1) *1
CS#	Chip Select
WP# (DQ_2)	Write Protect (Data Input Output 2) *2
HOLD# (DQ_3)	HOLD# pin (Data Input Output 3) *2
Vcc	Supply Voltage (2.7-3.6V)
Vss	Ground
NC	No Connect

Note:
1. DQ_0 and DQ_1 are used for Dual and Quad instructions.
2. DQ_2 ~ DQ_3 are used for Quad instructions.

SIGNAL DESCRIPTION

Serial Data Input, Output and IOs (DI, DO and DQ_0, DQ_1, DQ_2, DQ_3)

The EN25QH256 support standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge CLK.

Dual and Quad SPI instruction use the bidirectional IO pins to serially write instruction, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK.

Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Mode")

Chip Select (CS#)

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output (DO, or DQ_0, DQ_1, DQ_2 and DQ_3) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

Hold (HOLD#)

The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). The hold function can be useful when multiple devices are sharing the same SPI signals. The HOLD# function is only available for standard SPI and Dual SPI operation, when during Quad SPI, this pin is the Serial Data IO (DQ_3) for Quad I/O operation.

Write Protect (WP#)

The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1, BP2 and BP3) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. The WP# function is only available for standard SPI and Dual SPI operation, when during Quad SPI, this pin is the Serial Data IO (DQ_2) for Quad I/O operation.

MEMORY ORGANIZATION

The memory is organized as:

- 33,554,432 bytes
- Uniform Sector Architecture
  512 blocks of 64-Kbyte
  8,192 sectors of 4-Kbyte
  131,072 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

Table 2. Uniform Block Sector Architecture (1/8)

Block	Sector	Address range	
511	8191	1FFF000h	1FFFFFFh
	⋮	⋮	⋮
	8176	1FF0000h	1FF0FFFh
510	8175	1FEF000h	1FEFFFFh
	⋮	⋮	⋮
	8160	1FE0000h	1FE0FFFh
509	8159	1FDF000h	1FDFFFFh
	⋮	⋮	⋮
	8144	1FD0000h	1FD0FFFh
⋮	⋮	⋮	⋮
498	7983	1F2F000h	1F2FFFFh
	⋮	⋮	⋮
	7968	1F20000h	1F20FFFh
497	7967	1F1F000h	1F1FFFFh
	⋮	⋮	⋮
	7952	1F10000h	1F10FFFh
496	7951	1F0F000h	1F0FFFFh
	⋮	⋮	⋮
	7936	1F00000h	1F00FFFh

Block	Sector	Address range	
495	7935	1EFF000h	1EFFFFFh
	⋮	⋮	⋮
	7920	1EF0000h	1EF0FFFh
494	7919	1EEF000h	1EEFFFFh
	⋮	⋮	⋮
	7904	1EE0000h	1EE0FFFh
493	7903	1EDF000h	1EDFFFFh
	⋮	⋮	⋮
	7888	1ED0000h	1ED0FFFh
⋮	⋮	⋮	⋮
482	7727	1E2F000h	1E2FFFFh
	⋮	⋮	⋮
	7712	1E20000h	1E20FFFh
481	7711	1E1F000h	1E1FFFFh
	⋮	⋮	⋮
	7696	1E10000h	1E10FFFh
480	7695	1E0F000h	1E0FFFFh
	⋮	⋮	⋮
	7680	1E00000h	1E00FFFh

Block	Sector	Address range	
479	7679	1DFF000h	1DFFFFFh
	⋮	⋮	⋮
	7664	1DF0000h	1DF0FFFh
478	7663	1DEF000h	1DEFFFFh
	⋮	⋮	⋮
	7648	1DE0000h	1DE0FFFh
477	7647	1DDF000h	1DDFFFFh
	⋮	⋮	⋮
	7632	1DD0000h	1DD0FFFh
⋮	⋮	⋮	⋮
466	7471	1D2F000h	1D2FFFFh
	⋮	⋮	⋮
	7456	1D20000h	1D20FFFh
465	7455	1D1F000h	1D1FFFFh
	⋮	⋮	⋮
	7440	1D10000h	1D10FFFh
464	7439	1D0F000h	1D0FFFFh
	⋮	⋮	⋮
	7424	1D00000h	1D00FFFh

Block	Sector	Address range	
463	7423	1CFF000h	1CFFFFFh
	⋮	⋮	⋮
	7408	1CF0000h	1CF0FFFh
462	7407	1CEF000h	1CEFFFFh
	⋮	⋮	⋮
	7392	1CE0000h	1CE0FFFh
461	7391	1CDF000h	1CDFFFFh
	⋮	⋮	⋮
	7376	1CD0000h	1CD0FFFh
⋮	⋮	⋮	⋮
450	7215	1C2F000h	1C2FFFFh
	⋮	⋮	⋮
	7200	1C20000h	1C20FFFh
449	7199	1C1F000h	1C1FFFFh
	⋮	⋮	⋮
	7184	1C10000h	1C10FFFh
448	7183	1C0F000h	1C0FFFFh
	⋮	⋮	⋮
	7168	1C00000h	1C00FFFh

Table 2. Uniform Block Sector Architecture (2/8)

Block	Sector	Address range	
447	7167	1BFF000h	1BFFFFFh
	⋮	⋮	⋮
	7152	1BF0000h	1BF0FFFh
446	7151	1BEF000h	1BEFFFFh
	⋮	⋮	⋮
	7136	1BE0000h	1BE0FFFh
445	7135	1BDF000h	1BDFFFFh
	⋮	⋮	⋮
	7120	1BD0000h	1BD0FFFh
⋮	⋮	⋮	⋮
434	6959	1B2F000h	1B2FFFFh
	⋮	⋮	⋮
	6944	1B20000h	1B20FFFh
433	6943	1B1F000h	1B1FFFFh
	⋮	⋮	⋮
	6928	1B10000h	1B10FFFh
432	6927	1B0F000h	1B0FFFFh
	⋮	⋮	⋮
	6912	1B00000h	1B00FFFh

Block	Sector	Address range	
431	6911	1AFF000h	1AFFFFFh
	⋮	⋮	⋮
	6896	1AF0000h	1AF0FFFh
430	6895	1AEF000h	1AEFFFFh
	⋮	⋮	⋮
	6880	1AE0000h	1AE0FFFh
429	6879	1ADF000h	1ADFFFFh
	⋮	⋮	⋮
	6864	1AD0000h	1AD0FFFh
⋮	⋮	⋮	⋮
418	6703	1A2F000h	1A2FFFFh
	⋮	⋮	⋮
	6688	1A20000h	1A20FFFh
417	6687	1A1F000h	1A1FFFFh
	⋮	⋮	⋮
	6672	1A10000h	1A10FFFh
416	6671	1A0F000h	1A0FFFFh
	⋮	⋮	⋮
	6656	1A00000h	1A00FFFh

Block	Sector	Address range	
415	6655	19FF000h	19FFFFFh
	⋮	⋮	⋮
	6640	19F0000h	19F0FFFh
414	6639	19EF000h	19EFFFFh
	⋮	⋮	⋮
	6624	19E0000h	19E0FFFh
413	6623	19DF000h	19DFFFFh
	⋮	⋮	⋮
	6608	19D0000h	19D0FFFh
⋮	⋮	⋮	⋮
402	6447	192F000h	192FFFFh
	⋮	⋮	⋮
	6432	1920000h	1920FFFh
401	6431	191F000h	191FFFFh
	⋮	⋮	⋮
	6416	1910000h	1910FFFh
400	6415	190F000h	190FFFFh
	⋮	⋮	⋮
	6400	1900000h	1900FFFh

Block	Sector	Address range	
399	6399	18FF000h	18FFFFFh
	⋮	⋮	⋮
	6384	18F0000h	18F0FFFh
398	6383	18EF000h	18EFFFFh
	⋮	⋮	⋮
	6368	18E0000h	18E0FFFh
397	6367	18DF000h	18DFFFFh
	⋮	⋮	⋮
	6352	18D0000h	18D0FFFh
⋮	⋮	⋮	⋮
386	6191	182F000h	182FFFFh
	⋮	⋮	⋮
	6176	1820000h	1820FFFh
385	6175	181F000h	181FFFFh
	⋮	⋮	⋮
	6160	1810000h	1810FFFh
384	6159	180F000h	180FFFFh
	⋮	⋮	⋮
	6144	1800000h	1800FFFh

Table 2. Uniform Block Sector Architecture (3/8)

Block	Sector	Address range	
383	6143	17FF000h	17FFFFFh
	⋮	⋮	⋮
	6128	17F0000h	17F0FFFh
382	6127	17EF000h	17EFFFFh
	⋮	⋮	⋮
	6112	17E0000h	17E0FFFh
381	6111	17DF000h	17DFFFFh
	⋮	⋮	⋮
	6096	17D0000h	17D0FFFh
⋮	⋮	⋮	⋮
370	5935	172F000h	172FFFFh
	⋮	⋮	⋮
	5920	1720000h	1720FFFh
369	5919	171F000h	171FFFFh
	⋮	⋮	⋮
	5904	1710000h	1710FFFh
368	5903	170F000h	170FFFFh
	....	....	....
	5888	1700000h	1700FFFh

Block	Sector	Address range	
367	5887	16FF000h	16FFFFFh
	⋮	⋮	⋮
	5872	16F0000h	16F0FFFh
366	5871	16EF000h	16EFFFFh
	⋮	⋮	⋮
	5856	16E0000h	16E0FFFh
365	5855	16DF000h	16DFFFFh
	⋮	⋮	⋮
	5840	16D0000h	16D0FFFh
⋮	⋮	⋮	⋮
354	5679	162F000h	162FFFFh
	⋮	⋮	⋮
	5664	1620000h	1620FFFh
353	5663	161F000h	161FFFFh
	⋮	⋮	⋮
	5648	1610000h	1610FFFh
352	5647	160F000h	160FFFFh
	....	....	....
	5632	1600000h	1600FFFh

Block	Sector	Address range	
351	5631	15FF000h	15FFFFFh
	⋮	⋮	⋮
	5616	15F0000h	15F0FFFh
350	5615	15EF000h	15EFFFFh
	⋮	⋮	⋮
	5600	15E0000h	15E0FFFh
349	5599	15DF000h	15DFFFFh
	⋮	⋮	⋮
	5584	15D0000h	15D0FFFh
⋮	⋮	⋮	⋮
338	5423	152F000h	152FFFFh
	⋮	⋮	⋮
	5408	1520000h	1520FFFh
337	5407	151F000h	151FFFFh
	⋮	⋮	⋮
	5392	1510000h	1510FFFh
336	5391	150F000h	150FFFFh
	⋮	⋮	⋮
	5376	1500000h	1500FFFh

Block	Sector	Address range	
335	5375	14FF000h	14FFFFFh
	⋮	⋮	⋮
	5360	14F0000h	14F0FFFh
334	5359	14EF000h	14EFFFFh
	⋮	⋮	⋮
	5344	14E0000h	14E0FFFh
333	5343	14DF000h	14DFFFFh
	⋮	⋮	⋮
	5328	14D0000h	14D0FFFh
⋮	⋮	⋮	⋮
322	5167	142F000h	142FFFFh
	⋮	⋮	⋮
	5152	1420000h	1420FFFh
321	5151	141F000h	141FFFFh
	⋮	⋮	⋮
	5136	1410000h	1410FFFh
320	5135	140F000h	140FFFFh
	⋮	⋮	⋮
	5120	1400000h	1400FFFh

Table 2. Uniform Block Sector Architecture (4/8)

Block	Sector	Address range	
319	5119	13FF000h	13FFFFFh
	⋮	⋮	⋮
	5104	13F0000h	13F0FFFh
318	5103	13EF000h	13EFFFFh
	⋮	⋮	⋮
	5088	13E0000h	13E0FFFh
317	5087	13DF000h	13DFFFFh
	⋮	⋮	⋮
	5072	13D0000h	13D0FFFh
⋮	⋮	⋮	⋮
306	4911	132F000h	132FFFFh
	⋮	⋮	⋮
	4896	1320000h	1320FFFh
305	4895	131F000h	131FFFFh
	⋮	⋮	⋮
	4880	1310000h	1310FFFh
304	4879	130F000h	130FFFFh
	⋮	⋮	⋮
	4864	1300000h	1300FFFh

Block	Sector	Address range	
303	4863	12FF000h	12FFFFFh
	⋮	⋮	⋮
	4848	12F0000h	12F0FFFh
302	4847	12EF000h	12EFFFFh
	⋮	⋮	⋮
	4831	12E0000h	12E0FFFh
301	4831	12DF000h	12DFFFFh
	⋮	⋮	⋮
	4816	12D0000h	12D0FFFh
⋮	⋮	⋮	⋮
290	4655	122F000h	122FFFFh
	⋮	⋮	⋮
	4640	1220000h	1220FFFh
289	4639	121F000h	121FFFFh
	⋮	⋮	⋮
	4624	1210000h	1210FFFh
288	4623	120F000h	120FFFFh
	⋮	⋮	⋮
	4608	1200000h	1200FFFh

Block	Sector	Address range	
287	4606	11FF000h	11FFFFFh
	⋮	⋮	⋮
	4592	11F0000h	11F0FFFh
286	4591	11EF000h	11EFFFFh
	⋮	⋮	⋮
	4576	11E0000h	11E0FFFh
285	4575	11DF000h	11DFFFFh
	⋮	⋮	⋮
	4560	11D0000h	11D0FFFh
⋮	⋮	⋮	⋮
274	4399	112F000h	112FFFFh
	⋮	⋮	⋮
	4384	1120000h	1120FFFh
273	4383	111F000h	111FFFFh
	⋮	⋮	⋮
	4368	1110000h	1110FFFh
272	4367	110F000h	110FFFFh
	⋮	⋮	⋮
	4353	1100000h	1100FFFh

Block	Sector	Address range	
271	4351	10FF000h	10FFFFFh
	⋮	⋮	⋮
	4336	10F0000h	10F0FFFh
270	4335	10EF000h	10EFFFFh
	⋮	⋮	⋮
	4320	10E0000h	10E0FFFh
269	4319	10DF000h	10DFFFFh
	⋮	⋮	⋮
	4304	10D0000h	10D0FFFh
⋮	⋮	⋮	⋮
258	4143	102F000h	102FFFFh
	⋮	⋮	⋮
	4128	1020000h	1020FFFh
257	4127	101F000h	101FFFFh
	⋮	⋮	⋮
	4112	1010000h	1010FFFh
256	4111	100F000h	100FFFFh
	⋮	⋮	⋮
	4096	1000000h	1000FFFh

Table 2. Uniform Block Sector Architecture (5/8)

Block	Sector	Address range	
255	4095	0FFF000h	0FFFFFFh
	⋮	⋮	⋮
	4080	0FF0000h	0FF0FFFh
254	4079	0FEF000h	0FEFFFFh
	⋮	⋮	⋮
	4064	0FE0000h	0FE0FFFh
253	4063	0FDF000h	0FDFFFFh
	⋮	⋮	⋮
	4048	0FD0000h	0FD0FFFh
⋮	⋮	⋮	⋮
242	3887	0F2F000h	0F2FFFFh
	⋮	⋮	⋮
	3872	0F20000h	0F20FFFh
241	3871	0F1F000h	0F1FFFFh
	⋮	⋮	⋮
	3856	0F10000h	0F10FFFh
240	3855	0F0F000h	0F0FFFFh
	⋮	⋮	⋮
	3840	0F00000h	0F00FFFh

Block	Sector	Address range	
239	3839	0EFF000h	0EFFFFFh
	⋮	⋮	⋮
	3824	0EF0000h	0EF0FFFh
238	3823	0EEF000h	0EEFFFFh
	⋮	⋮	⋮
	3808	0EE0000h	0EE0FFFh
237	3807	0EDF000h	0EDFFFFh
	⋮	⋮	⋮
	3792	0ED0000h	0ED0FFFh
⋮	⋮	⋮	⋮
226	3631	0E2F000h	0E2FFFFh
	⋮	⋮	⋮
	3616	0E20000h	0E20FFFh
225	3615	0E1F000h	0E1FFFFh
	⋮	⋮	⋮
	3600	0E10000h	0E10FFFh
224	3599	0E0F000h	0E0FFFFh
	⋮	⋮	⋮
	3584	0E00000h	0E00FFFh

Block	Sector	Address range	
223	3583	0DFF000h	0DFFFFFh
	⋮	⋮	⋮
	3568	0DF0000h	0DF0FFFh
222	3567	0DEF000h	0DEFFFFh
	⋮	⋮	⋮
	3552	0DE0000h	0DE0FFFh
221	3551	0DDF000h	0DDFFFFh
	⋮	⋮	⋮
	3536	0DD0000h	0DD0FFFh
⋮	⋮	⋮	⋮
210	3375	0D2F000h	0D2FFFFh
	⋮	⋮	⋮
	3360	0D20000h	0D20FFFh
209	3359	0D1F000h	0D1FFFFh
	⋮	⋮	⋮
	3344	0D10000h	0D10FFFh
208	3343	0D0F000h	0D0FFFFh
	⋮	⋮	⋮
	3328	0D00000h	0D00FFFh

Block	Sector	Address range	
207	3327	0CFF000h	0CFFFFFh
	⋮	⋮	⋮
	3312	0CF0000h	0CF0FFFh
206	3311	0CEF000h	0CEFFFFh
	⋮	⋮	⋮
	3296	0CE0000h	0CE0FFFh
205	3295	0CDF000h	0CDFFFFh
	⋮	⋮	⋮
	3280	0CD0000h	0CD0FFFh
⋮	⋮	⋮	⋮
194	3119	0C2F000h	0C2FFFFh
	⋮	⋮	⋮
	3014	0C20000h	0C20FFFh
193	3103	0C1F000h	0C1FFFFh
	⋮	⋮	⋮
	3088	0C10000h	0C10FFFh
192	3087	0C0F000h	0C0FFFFh
	⋮	⋮	⋮
	3072	0C00000h	0C00FFFh

Table 2. Uniform Block Sector Architecture (6/8)

Block	Sector	Address range	
191	3071	0BFF000h	0BFFFFFh
	⋮	⋮	⋮
	3056	0BF0000h	0BF0FFFh
190	3055	0BEF000h	0BEFFFFh
	⋮	⋮	⋮
	3040	0BE0000h	0BE0FFFh
189	3039	0BDF000h	0BDFFFFh
	⋮	⋮	⋮
	3024	0BD0000h	0BD0FFFh
⋮	⋮	⋮	⋮
178	2863	0B2F000h	0B2FFFFh
	⋮	⋮	⋮
	2848	0B20000h	0B20FFFh
177	2847	0B1F000h	0B1FFFFh
	⋮	⋮	⋮
	2832	0B10000h	0B10FFFh
176	2831	0B0F000h	0B0FFFFh
	⋮	⋮	⋮
	2816	0B00000h	0B00FFFh

Block	Sector	Address range	
175	2815	0AFF000h	0AFFFFFh
	⋮	⋮	⋮
	2800	0AF0000h	0AF0FFFh
174	2799	0AEF000h	0AEFFFFh
	⋮	⋮	⋮
	2784	0AE0000h	0AE0FFFh
173	2783	0ADF000h	0ADFFFFh
	⋮	⋮	⋮
	2768	0AD0000h	0AD0FFFh
⋮	⋮	⋮	⋮
162	2607	0A2F000h	0A2FFFFh
	⋮	⋮	⋮
	2592	0A20000h	0A20FFFh
161	2591	0A1F000h	0A1FFFFh
	⋮	⋮	⋮
	2576	0A10000h	0A10FFFh
160	2575	0A0F000h	0A0FFFFh
	⋮	⋮	⋮
	2560	0A00000h	0A00FFFh

Block	Sector	Address range	
159	2559	09FF000h	09FFFFFh
	⋮	⋮	⋮
	2544	09F0000h	09F0FFFh
158	2543	09EF000h	09EFFFFh
	⋮	⋮	⋮
	2528	09E0000h	09E0FFFh
157	2527	09DF000h	09DFFFFh
	⋮	⋮	⋮
	2512	09D0000h	09D0FFFh
⋮	⋮	⋮	⋮
146	2351	092F000h	092FFFFh
	⋮	⋮	⋮
	2336	0920000h	0920FFFh
145	2335	091F000h	091FFFFh
	⋮	⋮	⋮
	2320	0910000h	0910FFFh
144	2319	090F000h	090FFFFh
	⋮	⋮	⋮
	2304	0900000h	0900FFFh

Block	Sector	Address range	
143	2303	08FF000h	08FFFFFh
	⋮	⋮	⋮
	2288	08F0000h	08F0FFFh
142	2287	08EF000h	08EFFFFh
	⋮	⋮	⋮
	2272	08E0000h	08E0FFFh
141	2271	08DF000h	08DFFFFh
	⋮	⋮	⋮
	2256	08D0000h	08D0FFFh
⋮	⋮	⋮	⋮
130	2095	082F000h	082FFFFh
	⋮	⋮	⋮
	2080	0820000h	0820FFFh
129	2079	081F000h	081FFFFh
	⋮	⋮	⋮
	2064	0810000h	0810FFFh
128	2063	080F000h	080FFFFh
	⋮	⋮	⋮
	2048	0800000h	0800FFFh

Table 2. Uniform Block Sector Architecture (7/8)

Block	Sector	Address range	
127	2047	07FF000h	07FFFFFh
	⋮	⋮	⋮
	2032	07F0000h	07F0FFFh
126	2031	07EF000h	07EFFFFh
	⋮	⋮	⋮
	2016	07E0000h	07E0FFFh
125	2015	07DF000h	07DFFFFh
	⋮	⋮	⋮
	2000	07D0000h	07D0FFFh
⋮	⋮	⋮	⋮
114	1839	072F000h	072FFFFh
	⋮	⋮	⋮
	1824	0720000h	0720FFFh
113	1823	071F000h	071FFFFh
	⋮	⋮	⋮
	1808	0710000h	0710FFFh
112	1807	070F000h	070FFFFh
	⋮	⋮	⋮
	1972	0700000h	0700FFFh

Block	Sector	Address range	
111	1791	06FF000h	06FFFFFh
	⋮	⋮	⋮
	1776	06F0000h	06F0FFFh
110	1775	06EF000h	06EFFFFh
	⋮	⋮	⋮
	1760	06E0000h	06E0FFFh
109	1759	06DF000h	06DFFFFh
	⋮	⋮	⋮
	1744	06D0000h	06D0FFFh
⋮	⋮	⋮	⋮
98	1583	062F000h	062FFFFh
	⋮	⋮	⋮
	1568	0620000h	0620FFFh
97	1567	061F000h	061FFFFh
	⋮	⋮	⋮
	1552	0610000h	0610FFFh
96	1551	060F000h	060FFFFh
	⋮	⋮	⋮
	1536	0600000h	0600FFFh

Block	Sector	Address range	
95	1535	05FF000h	05FFFFFh
	⋮	⋮	⋮
	1520	05F0000h	05F0FFFh
94	1519	05EF000h	05EFFFFh
	⋮	⋮	⋮
	1504	05E0000h	05E0FFFh
93	1503	05DF000h	05DFFFFh
	⋮	⋮	⋮
	1488	05D0000h	05D0FFFh
⋮	⋮	⋮	⋮
82	1327	052F000h	052FFFFh
	⋮	⋮	⋮
	1312	0520000h	0520FFFh
81	1311	051F000h	051FFFFh
	⋮	⋮	⋮
	1296	0510000h	0510FFFh
80	1295	050F000h	050FFFFh
	⋮	⋮	⋮
	1280	0500000h	0500FFFh

Block	Sector	Address range	
79	1279	04FF000h	04FFFFFh
	⋮	⋮	⋮
	1264	04F0000h	04F0FFFh
78	1263	04EF000h	04EFFFFh
	⋮	⋮	⋮
	1248	04E0000h	04E0FFFh
77	1247	04DF000h	04DFFFFh
	⋮	⋮	⋮
	1232	04D0000h	04D0FFFh
⋮	⋮	⋮	⋮
66	1071	042F000h	042FFFFh
	⋮	⋮	⋮
	1056	0420000h	0420FFFh
65	1055	041F000h	041FFFFh
	⋮	⋮	⋮
	1040	0410000h	0410FFFh
64	1039	040F000h	040FFFFh
	⋮	⋮	⋮
	1024	0400000h	0400FFFh

Table 2. Uniform Block Sector Architecture (8/8)

Block	Sector	Address range	
63	1023	03FF000h	03FFFFFh
	⋮	⋮	⋮
	1008	03F0000h	03F0FFFh
62	1007	03EF000h	03EFFFFh
	⋮	⋮	⋮
	992	03E0000h	03E0FFFh
61	991	03DF000h	03DFFFFh
	⋮	⋮	⋮
	976	03D0000h	03D0FFFh
⋮	⋮	⋮	⋮
50	815	032F000h	032FFFFh
	⋮	⋮	⋮
	800	0320000h	0320FFFh
49	799	031F000h	031FFFFh
	⋮	⋮	⋮
	784	0310000h	0310FFFh
48	783	030F000h	030FFFFh
	⋮	⋮	⋮
	768	0300000h	0300FFFh

Block	Sector	Address range	
47	767	02FF000h	02FFFFFh
	⋮	⋮	⋮
	752	02F0000h	02F0FFFh
46	751	02EF000h	02EFFFFh
	⋮	⋮	⋮
	736	02E0000h	02E0FFFh
45	735	02DF000h	02DFFFFh
	⋮	⋮	⋮
	720	02D0000h	02D0FFFh
⋮	⋮	⋮	⋮
34	559	022F000h	022FFFFh
	⋮	⋮	⋮
	544	0220000h	0220FFFh
33	543	021F000h	021FFFFh
	⋮	⋮	⋮
	528	0210000h	0210FFFh
32	527	020F000h	020FFFFh
	⋮	⋮	⋮
	512	0200000h	0200FFFh

Block	Sector	Address range	
31	511	01FF000h	01FFFFFh
	⋮	⋮	⋮
	496	01F0000h	01F0FFFh
30	495	01EF000h	01EFFFFh
	⋮	⋮	⋮
	480	01E0000h	01E0FFFh
29	479	01DF000h	01DFFFFh
	⋮	⋮	⋮
	464	01D0000h	01D0FFFh
⋮	⋮	⋮	⋮
18	303	012F000h	012FFFFh
	⋮	⋮	⋮
	288	0120000h	0120FFFh
17	287	011F000h	011FFFFh
	⋮	⋮	⋮
	272	0110000h	0110FFFh
16	271	010F000h	010FFFFh
	⋮	⋮	⋮
	256	0100000h	0100FFFh

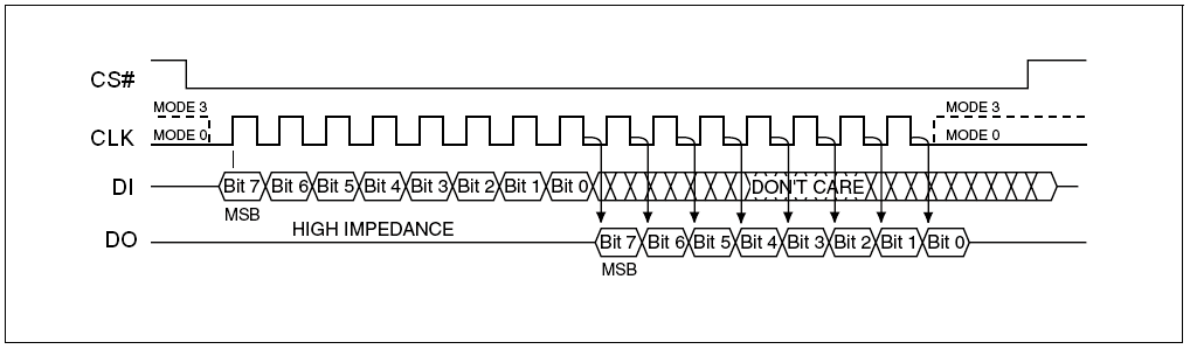
Block	Sector	Address range	
15	255	00FF000h	00FFFFFh
	⋮	⋮	⋮
	240	00F0000h	00F0FFFh
14	239	00EF000h	00EFFFFh
	⋮	⋮	⋮
	224	00E0000h	00E0FFFh
13	223	00DF000h	00DFFFFh
	⋮	⋮	⋮
	208	00D0000h	00D0FFFh
⋮	⋮	⋮	⋮
2	47	002F000h	002FFFFh
	⋮	⋮	⋮
	32	0020000h	0020FFFh
1	31	001F000h	001FFFFh
	⋮	⋮	⋮
	16	0010000h	0010FFFh
0	15	000F000h	000FFFFh
	⋮	⋮	⋮
	4	0004000h	0004FFFh
	3	0003000h	0003FFFh
	2	0002000h	0002FFFh
	1	0001000h	0001FFFh
	0	0000000h	0000FFFh

OPERATING FEATURES

Standard SPI Modes

The EN25QH256 is accessed through a SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3, as shown in Figure 3, concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of the CLK. Data output on the DO pin is clocked out on the falling edge of CLK.

Figure 3. SPI Modes



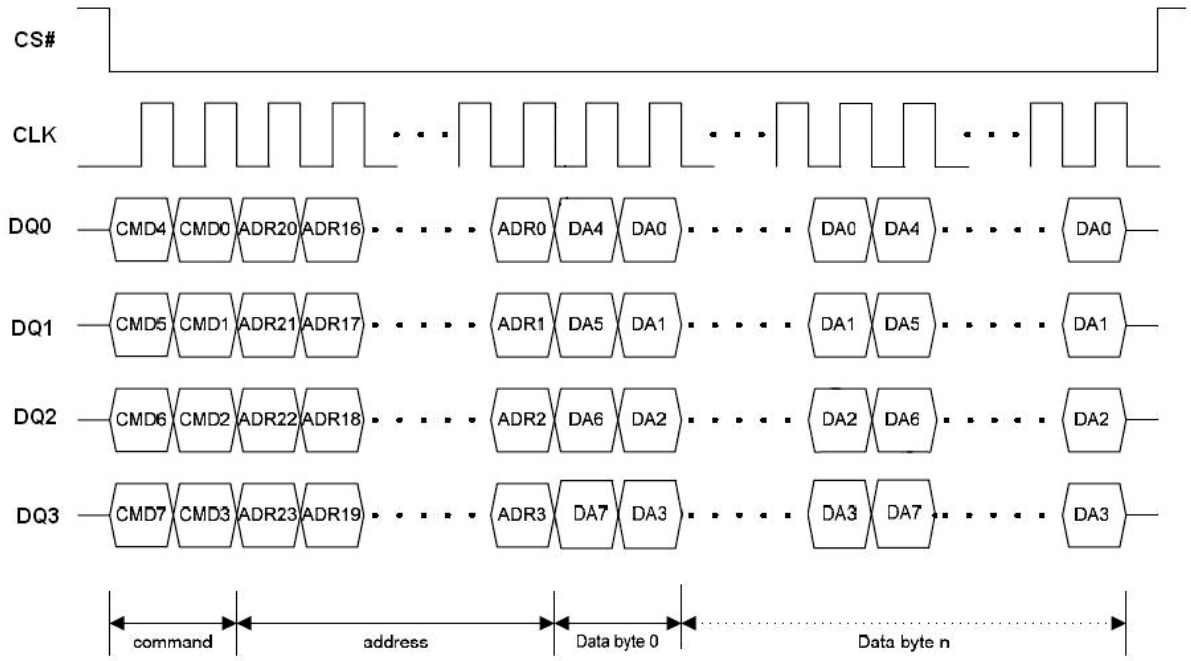
Dual SPI Instruction

The EN25QH256 supports Dual SPI operation when using the “Dual Output Fast Read and Dual I/O Fast Read “ (3Bh and BBh) instructions. These instructions allow data to be transferred to or from the Serial Flash memory at two to three times the rate possible with the standard SPI. The Dual Read instructions are ideal for quickly downloading code from Flash to RAM upon power-up (code-shadowing) or for application that cache code-segments to RAM for execution. The Dual output feature simply allows the SPI input pin to also serve as an output during this instruction. When using Dual SPI instructions the DI and DO pins become bidirectional I/O pins; DQ_0 and DQ_1. All other operations use the standard SPI interface with single output signal.

Quad SPI Instruction

The EN25QH256 supports Quad output operation when using the Quad I/O Fast Read (EBh).This instruction allows data to be transferred to or from the Serial Flash memory at four to six times the rate possible with the standard SPI. The Quad Read instruction offer a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or for application that cache code-segments to RAM for execution. The EN25QH256 also supports full Quad Mode function while using the Enable Quad Peripheral Interface mode (EQPI) (38h). When using Quad SPI instruction the DI and DO pins become bidirectional I/O pins; DQ_0 and DQ_1, and the WP# and HOLD# pins become DQ_2 and DQ_3 respectively.

Figure 4. Quad SPI Modes



Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).

To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0) provided that they lie in consecutive addresses on the same page of memory.

Sector Erase, Block Erase and Chip Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved a sector at a time, using the Sector Erase (SE) instruction, a block at a time using the Block Erase (BE) instruction or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration t_{SE} t_{BE} or t_{CE}). The Erase instruction must be preceded by a Write Enable (WREN) instruction.

Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE, BE or CE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, t_{BE} or t_{CE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, and Write Status Register). The device then goes into the Stand-by Power mode. The device consumption drops to I_{CC1}.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Device ID (RDI) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

Status Register and Information Register

The Status Register and Information Register contain a number of status and control bits that can be read or set (as appropriate) by specific instructions.

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions.

WHDIS bit. The WP# and Hold# Disable bit (WHDIS bit), non-volatile bit, it indicates the WP# and HOLD# are enabled or not. When it is “0” (factory default), the WP# and HOLD# are enabled. On the other hand, while WHDIS bit is “1”, the WP# and HOLD# are disabled. If the system executes Quad Input/Output FAST_READ (EBh) or EQPI (38h) command, this WHDIS bit becomes no affection since WP# and HOLD# function will be disabled by Quad Input/Output FAST_READ (EBh) or EQPI mode.

SRP bit / OTP_LOCK bit The Status Register Protect (SRP) bit operates in conjunction with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRP, BP3, BP2, BP1, BP0) become read-only bits.

In OTP mode, this bit serves as OTP_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP_LOCK bit value is equal 0, after OTP_LOCK bit is programmed with 1 by WRSR command, the OTP sector is protected from program and erase operation. The OTP_LOCK bit can only be programmed once.

Note : In OTP mode, the WRSR command will ignore any input data and program OTP_LOCK bit to 1, user must clear the protect bits before entering OTP mode and program the OTP code, then execute WRSR command to lock the OTP sector before leaving OTP mode.

4 BYTE Indicator bit. By writing EN4B instruction, the 4 BYTE bit may be set to “1” to access the address length of 32-bit for higher density (larger than 128Mb) memory area. The default state is “0”, which means the mode of 24-bit address. The 4 BYTE bit may be clear by power off or writing EX4B instruction to reset the state to be “0”

Program Fail Flag bit. While a program failure happened, the Program Fail Flag bit would be set. This bit will also be set when the user attempts to program a protected main memory region or a locked OTP region. This bit can indicate whether one or more of program operations fail, and can be reset by Program (PP) or Erase (SE, BE or CE) instructions.

Erase Fail Flag bit. While an erase failure happened, the Erase Fail Flag bit would be set. This bit will also be set when the user attempts to erase a protected main memory region or a locked OTP region. This bit can indicate whether one or more of erase operations fail, and can be reset by Program (PP) or Erase (SE, BE or CE) instructions.

Note : For Program and Erase Flag bits,

1. The flag bits can be reset by power-on or that embedded mode was executed like WRSR, Erase or Program command.
2. If the system is trying to erase a locked block and then program a locked block. The erase fail or program fail flag bit will be high due to no successful Program, Erase or WRSE command.

Write Protection

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the EN25QH256 provides the following data protection mechanisms:

- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion or Write Status Register (WRSR) instruction completion or Page Program (PP) instruction completion or Sector Erase (SE) instruction completion or Block Erase (BE) instruction completion or Chip Erase (CE) instruction completion
- The Block Protect (BP3, BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect (WP#) signal allows the Block Protect (BP3, BP2, BP1, BP0) bits and Status Register Protect (SRP) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Table 3. Protected Area Sizes Sector Organization

Status Register Content				Memory Content			
BP3 Bit	BP2 Bit	BP1 Bit	BP0 Bit	Protect Areas	Addresses	Density(KB)	Portion
0	0	0	0	None	None	None	None
0	0	0	1	Block 511	1FF0000h-1FFFFFFh	64KB	Upper 1/512
0	0	1	0	Block 510 to 511	1FE0000h-1FFFFFFh	128KB	Upper 2/512
0	0	1	1	Block 508 to 511	1FC0000h-1FFFFFFh	256KB	Upper 4/512
0	1	0	0	Block 504 to 511	1F80000h-1FFFFFFh	512KB	Upper 8/512
0	1	0	1	Block 496 to 511	1F00000h-1FFFFFFh	1024KB	Upper 16/512
0	1	1	0	Block 480 to 511	1E00000h-1FFFFFFh	2048KB	Upper 32/512
0	1	1	1	All	0000000h-1FFFFFFh	32768KB	All
1	0	0	0	None	None	None	None
1	0	0	1	Block 0	0000000h-000FFFFh	64KB	Lower 1/512
1	0	1	0	Block 0 to 1	0000000h-001FFFFh	128KB	Lower 2/512
1	0	1	1	Block 0 to 3	0000000h-003FFFFh	256KB	Lower 4/512
1	1	0	0	Block 0 to 7	0000000h-007FFFFh	512KB	Lower 8/512
1	1	0	1	Block 0 to 15	0000000h-00FFFFFh	1024KB	Lower 16/512
1	1	1	0	Block 0 to 31	0000000h-01FFFFFh	2048KB	Lower 32/512
1	1	1	1	All	0000000h-1FFFFFFh	32768KB	All

INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first. Serial Data Input (DI) is sampled on the first rising edge of Serial Clock (CLK) after Chip Select (CS#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (DI), each bit being latched on the rising edges of Serial Clock (CLK).

The instruction set is listed in Table 4. Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. Chip Select (CS#) must be driven High after the last bit of the instruction sequence has been shifted in. In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Dual Output Fast Read (3Bh), Dual I/O Fast Read (BBh), Quad Input/Output FAST_READ (EBh), Read Status Register (RDSR), Read Information Register (RDIFR) or Release from Deep Power-down, and Read Device ID (RDI) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (CS#) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select (CS#) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select (CS#) must driven High when the number of clock pulses after Chip Select (CS#) being driven Low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

In the case of multi-byte commands of Page Program (PP), and Release from Deep Power Down (RES) minimum number of bytes specified has to be given, without which, the command will be ignored.

In the case of Page Program, if the number of byte after the command is less than 4 (at least 1 data byte), it will be ignored too. In the case of SE and BE, exact 24-bit address is a must, any less or more will cause the command to be ignored.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 4A. Instruction Set

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
EQPI	38h						
RSTQIO(2)	FFh						
RSTEN	66h						
RST(1)	99h						
Write Enable	06h						
Write Disable / Exit OTP mode	04h						
Read Status Register	05h	(S7-S0)(3)					continuous(4)
Read Information Register	2Bh	(S7-S0)(3)					continuous(4)
Write Status Register	01h	S7-S0					
Enter 4-byte mode	B7h						
Exit 4-byte mode	E9h						
Enter High Bank Latch Mode	67h						
Exit High Bank Latch Mode	98h						
Page Program	02h (8)	A23-A16	A15-A8	A7-A0	D7-D0	Next byte	continuous
Sector Erase	20h (8)	A23-A16	A15-A8	A7-A0			
Block Erase	D8h (8)	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/ 60h						
Deep Power-down	B9h						
Release from Deep Power-down, and read Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(5)
Release from Deep Power-down							
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(6)
				01h	(ID7-ID0)	(M7-M0)	
Read Identification	9Fh	(M7-M0)	(ID15-ID8)	(ID7-ID0)	(7)		
Enter OTP mode	3Ah						
Read SFDP mode and Unique ID Number	5Ah (8)	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous

Notes:
1. RST command only executed if RSTEN command is executed first. Any intervening command will disable Reset.
2. Device accepts eight-clocks command in Standard SPI mode, or two-clocks command in Quad SPI mode
3. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the DO pin
4. The Status Register contents will repeat continuously until CS# terminate the instruction
5. The Device ID will repeat continuously until CS# terminates the instruction
6. The Manufacturer ID and Device ID bytes will repeat continuously until CS# terminates the instruction. 00h on Byte 4 starts with MID and alternate with DID, 01h on Byte 4 starts with DID and alternate with MID
7. (M7-M0) : Manufacturer, (ID15-ID8) : Memory Type, (ID7-ID0) : Memory Capacity
8. Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Table 4B. Instruction Set (Read Instruction)

Instruction Name	Byte 1 Code	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Read Data	03h (6)	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh (6)	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next Byte) continuous
Dual Output Fast Read	3Bh (6)	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, …) (1)	(one byte per 4 clocks, continuous)
Dual I/O Fast Read	BBh (6)	A23-A8(2)	A7-A0, dummy (2)	(D7-D0, …) (1)			(one byte per 4 clocks, continuous)
Quad I/O Fast Read	EBh (6)	A23-A0, dummy (4)	(dummy, D7-D0) (5)	(D7-D0, …) (3)			(one byte per 2 clocks, continuous)

Notes:

1. Dual Output data
   DQ_0 = (D6, D4, D2, D0)
   DQ_1 = (D7, D5, D3, D1)

2. Dual Input Address
   DQ_0 = A22, A20, A18, A16, A14, A12, A10, A8 ; A6, A4, A2, A0, dummy 6, dummy 4, dummy 2, dummy 0
   DQ_1 = A23, A21, A19, A17, A15, A13, A11, A9 ; A7, A5, A3, A1, dummy 7, dummy 5, dummy 3, dummy 1

3. Quad Data
   DQ_0 = (D4, D0, ……)
   DQ_1 = (D5, D1, ……)
   DQ_2 = (D6, D2, …..)
   DQ_3 = (D7, D3, …..)

4. Quad Input Address
   DQ_0 = A20, A16, A12, A8, A4, A0, dummy 4, dummy 0
   DQ_1 = A21, A17, A13, A9, A5, A1, dummy 5, dummy 1
   DQ_2 = A22, A18, A14, A10, A6, A2, dummy 6, dummy 2
   DQ_3 = A23, A19, A15, A11, A7, A3, dummy 7, dummy 3

5. Quad I/O Fast Read Data
   DQ_0 = (dummy 12, dummy 8, dummy 4, dummy 0, D4, D0)
   DQ_1 = (dummy 13, dummy 9, dummy 5, dummy 1, D5, D1)
   DQ_2 = (dummy 14, dummy 10, dummy 6, dummy 2, D6, D2)
   DQ_3 = (dummy 15, dummy 11, dummy 7, dummy 3, D7, D3)

6. Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Table 5. Manufacturer and Device Identification

OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			18h
90h	1Ch		18h
9Fh	1Ch	7019h	

Enable Quad Peripheral Interface mode (EQPI) (38h)

The Enable Quad Peripheral Interface mode (EQPI) instruction will enable the flash device for Quad SPI bus operation. Upon completion of the instruction, all instructions thereafter will be 4-bit multiplexed input/output until a power cycle or " Reset Quad I/O instruction " instruction, as shown in Figure 5. The device did not support the Read Data Bytes (READ) (03h), Dual Output Fast Read (3Bh) and Dual Input/Output FAST_READ (BBh) modes while the Enable Quad Peripheral Interface mode (EQPI) (38h) turns on.

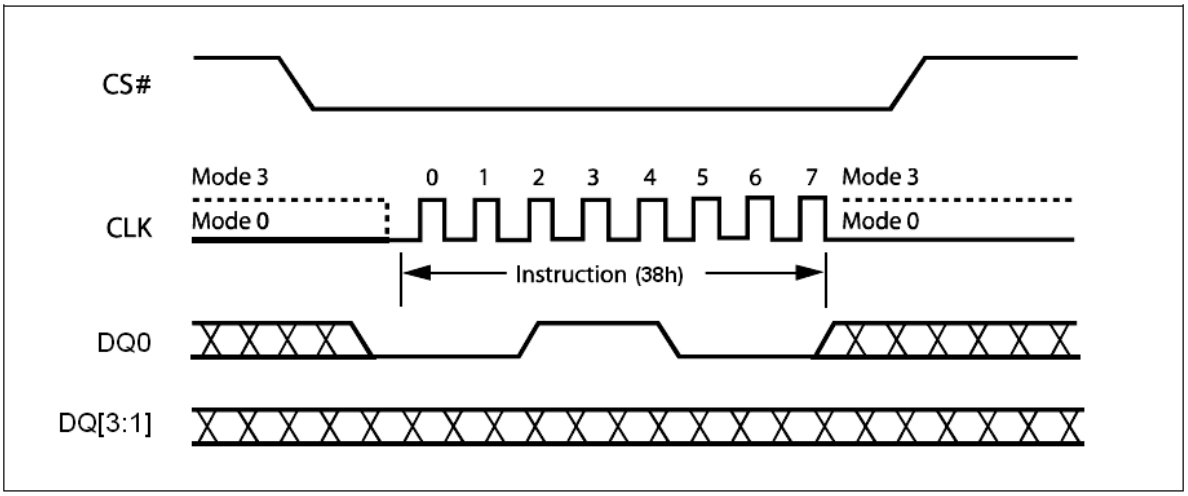


Figure 5. Enable Quad Peripheral Interface mode Sequence Diagram

Reset Quad I/O (RSTQIO) (FFh)

The Reset Quad I/O instruction resets the device to 1-bit Standard SPI operation. To execute a Reset Quad I/O operation, the host drives CS# low, sends the Reset Quad I/O command cycle (FFh) then, drives CS# high. This command can't be used in Standard SPI mode.

Reset-Enable (RSTEN) (66h) and Reset (RST) (99h)

The Reset operation is used as a system (software) reset that puts the device in normal operating Ready mode. This operation consists of two commands: Reset-Enable (RSTEN) and Reset (RST).

To reset the EN25QH256 the host drives CS# low, sends the Reset-Enable command (66h), and drives CS# high. Next, the host drives CS# low again, sends the Reset command (99h), and drives CS# high. The Reset operation requires the Reset-Enable command followed by the Reset command. Any command other than the Reset command after the Reset-Enable command will disable the Reset-Enable.

A successful command execution will reset the Status register and the Information register to data = 00h, see Figure 6 for SPI Mode and Figure 6.1 for EQPI Mode. A device reset during an active Program or Erase operation aborts the operation, which can cause the data of the targeted address range to be corrupted or lost. Depending on the prior operation, the reset timing may vary. Recovery from a Write operation requires more software latency time (t_{SR}) than recovery from other operations.

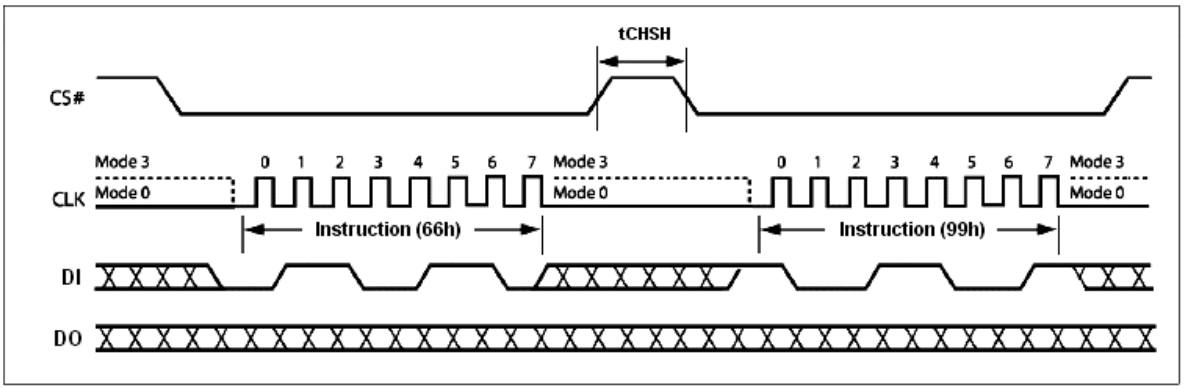


Figure 6. Reset-Enable and Reset Sequence Diagram

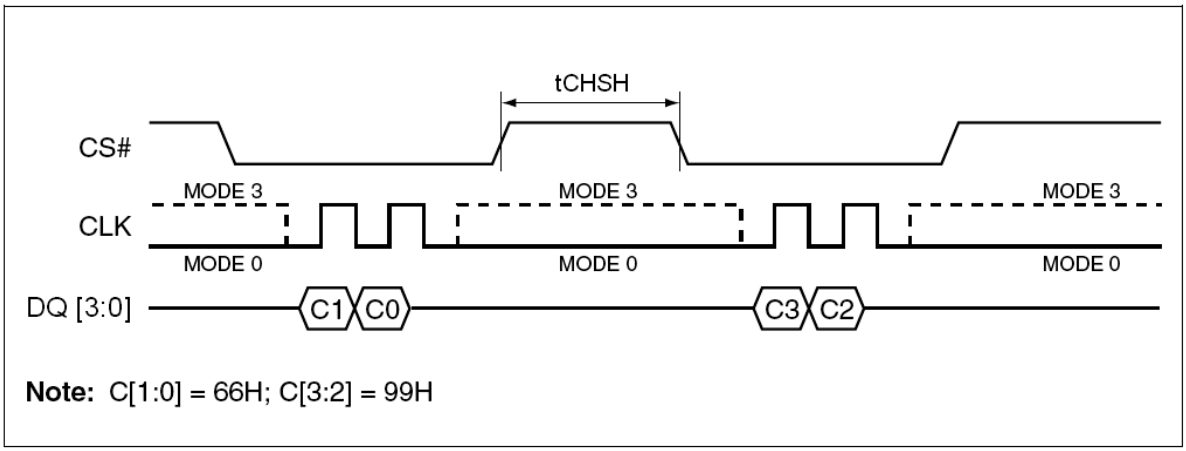
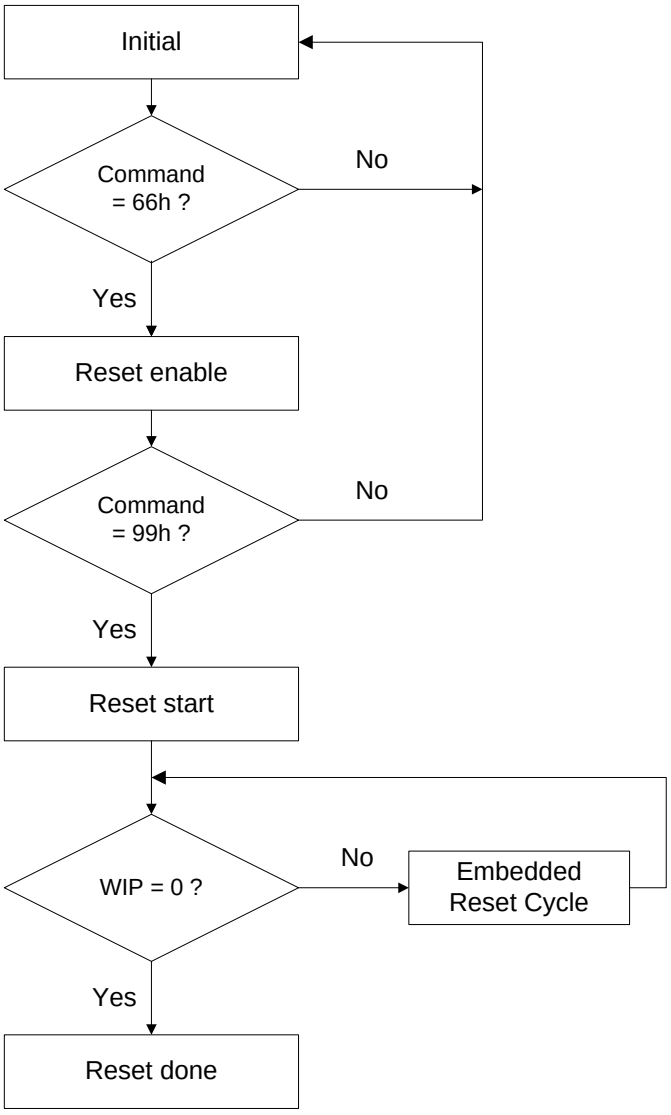


Figure 6.1 Reset-Enable and Reset Sequence Diagram under EQPI Mode

Software Reset Flow



Note:

1. Reset-Enable (RSTEN) (66h) and Reset (RST) (99h) commands need to match standard SPI or EQPI (Quad) mode.
2. Continue (Enhance) EB mode need to use quad Reset-Enable (RSTEN) (66h) and quad Reset (RST) (99h) commands.
3. If user is not sure it is in SPI or Quad mode, we suggest to execute sequence as follows:
   Quad Reset-Enable (RSTEN) (66h) -> Quad Reset (RST) (99h) -> SPI Reset-Enable (RSTEN) (66h) -> SPI Reset (RST) (99h) to reset.
4. The reset command could be executed during embedded program and erase process, EQPI mode and Continue EB mode to back to SPI mode.
5. This flow cannot release the device from Deep power down mode.
6. The Status Register Bit and Information register Bit will reset to default value after reset done.
7. If user reset device during erase, the embedded reset cycle software reset latency will take about 28us in worst case.

Write Enable (WREN) (06h)

The Write Enable (WREN) instruction (Figure 7) sets the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) instruction.
The Write Enable (WREN) instruction is entered by driving Chip Select (CS#) Low, sending the instruction code, and then driving Chip Select (CS#) High.

The instruction sequence is shown in Figure 8.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

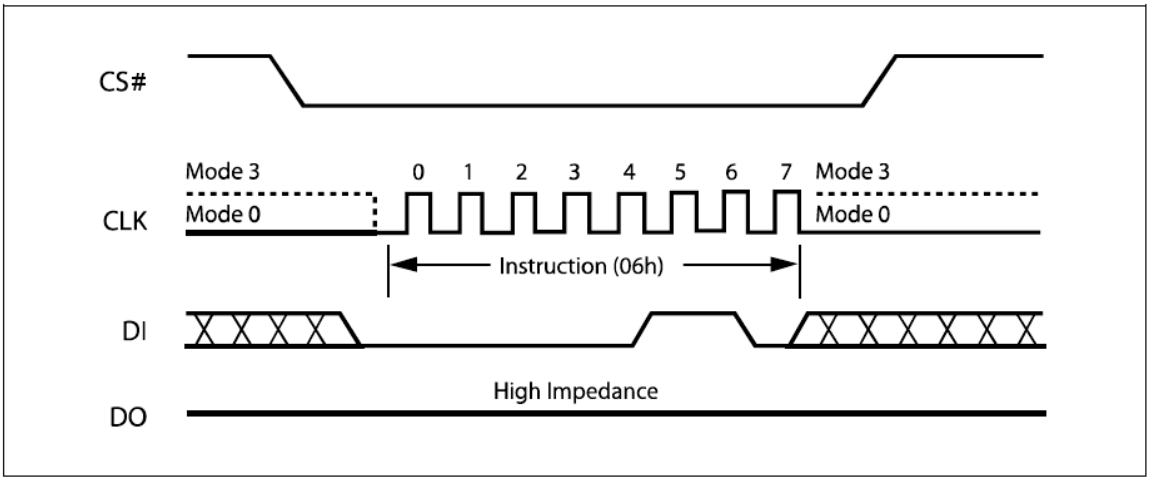


Figure 7. Write Enable Instruction Sequence Diagram

Write Disable (WRDI) (04h)

The Write Disable instruction (Figure 8) resets the Write Enable Latch (WEL) bit in the Status Register to a 0 or exit from OTP mode to normal mode. The Write Disable instruction is entered by driving Chip Select (CS#) low, shifting the instruction code “04h” into the DI pin and then driving Chip Select (CS#) high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase (BE) and Chip Erase instructions.

The instruction sequence is shown in Figure 8.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

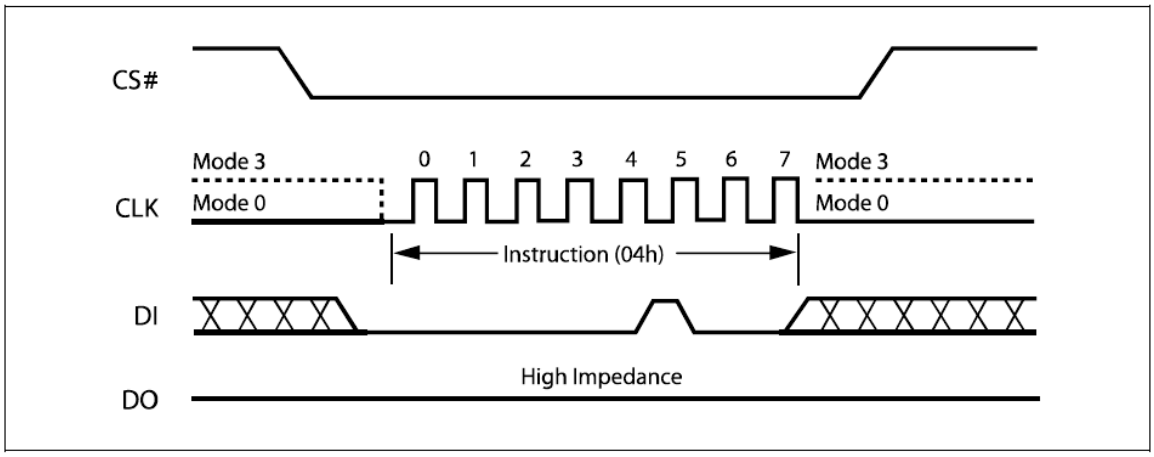


Figure 8. Write Disable Instruction Sequence Diagram

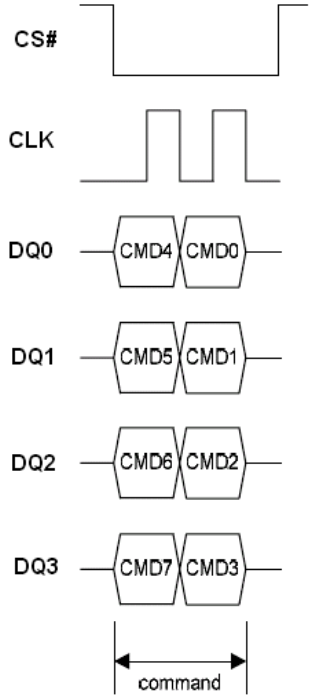


Figure 8.1 Write Enable/Disable Instruction Sequence under EQPI Mode

Read Status Register (RDSR) (05h)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 9.

The instruction sequence is shown in Figure 9.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

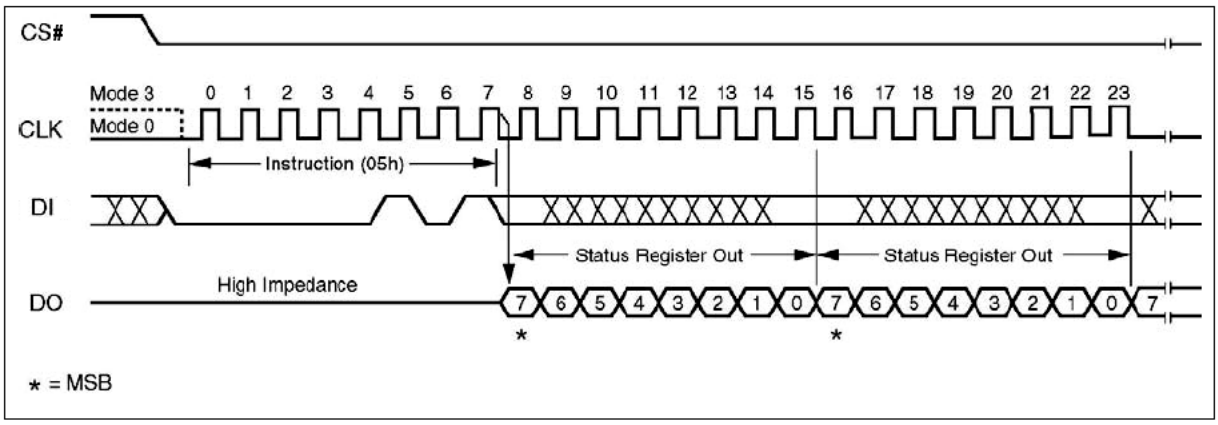


Figure 9. Read Status Register Instruction Sequence Diagram

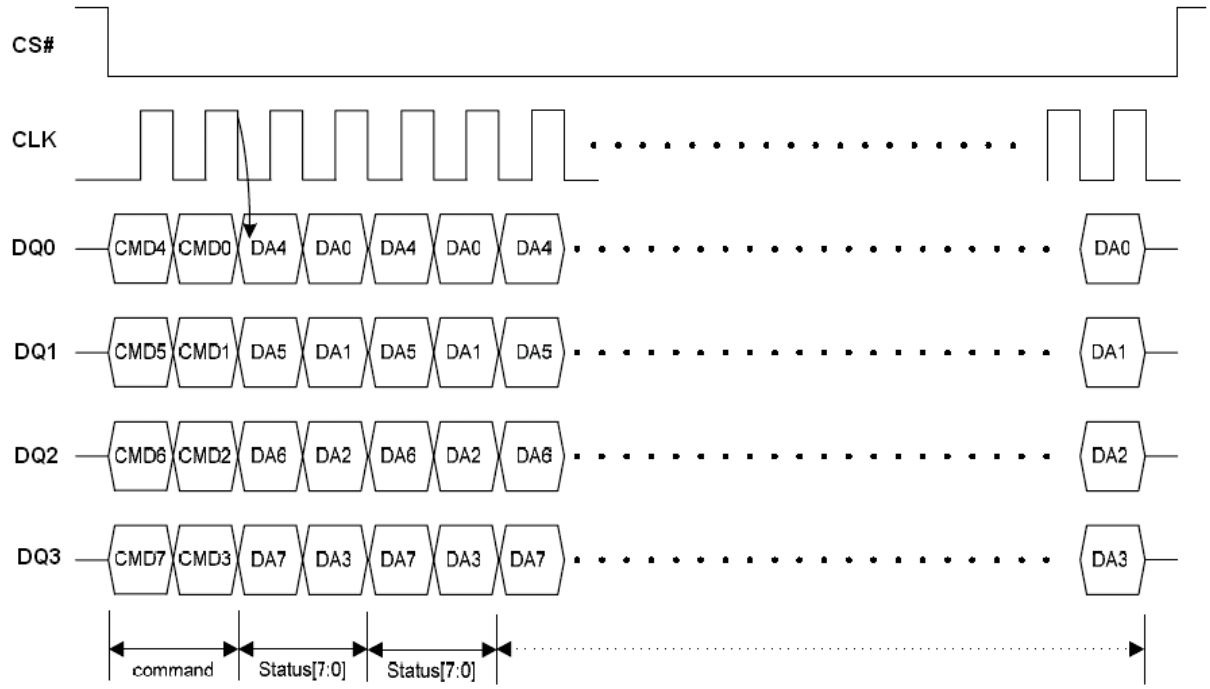


Figure 9.1 Read Status Register Instruction Sequence under EQPI Mode

Table 6. Status Register Bit Locations

S7		S6	S5	S4	S3	S2	S1	S0
SRP Status Register Protect	OTP_LOCK bit (note 1)	WHDIS WP# & Hold# Disable bit	BP3 (Block Protected bits)	BP2 (Block Protected bits)	BP1 (Block Protected bits)	BP0 (Block Protected bits)	WEL (Write Enable Latch)	WIP (Write In Progress bit) (Note 3)
1 = status register write disable	1 = OTP sector is protected	1 = WP# and HOLD# disable 0 = WP# and HOLD# enable	(note 2)	(note 2)	(note 2)	(note 2)	1 = write enable 0 = not write enable	1 = write operation 0 = not in write operation
Non-volatile bit		Non-volatile bit	Non-volatile bit.	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note

1. In OTP mode, SRP bit is served as OTP_LOCK bit.
2. See the table "Protected Area Sizes Sector Organization".
3. When executed the (RDSR) (05h) command, the OTP_LOCK bit (S7 / in OTP mode) value is the same as OTP_LOCK bit (S1) in table 7.

The status and control bits of the Status Register are as follows:

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP3, BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 3.) becomes protected against Page Program (PP) Sector Erase (SE) and , Block Erase (BE), instructions. The Block Protect

(BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) instruction is executed if, and only if, all Block Protect (BP3, BP2, BP1, BP0) bits are 0.

WHDIS bit. The WP# and Hold# Disable bit (WHDIS bit), non-volatile bit, it indicates the WP# and HOLD# are enabled or not. When it is "0" (factory default), the WP# and HOLD# are enabled. On the other hand, while WHDIS bit is "1", the WP# and HOLD# are disabled. If the system executes Quad Input/Output FAST_READ (EBh) or EQPI (38h) command, this WHDIS bit becomes no affection since WP# and HOLD# function will be disabled by Quad Input/Output FAST_READ (EBh) or EQPI mode.

SRP bit / OTP_LOCK bit. The Status Register Protect (SRP) bit operates in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected mode (when the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low). In this mode, the non-volatile bits of the Status Register (SRP, BP3, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

In OTP mode, this bit serves as OTP_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP_LOCK bit value is equal 0, after OTP_LOCK bit is programmed with 1 by WRSR command, the OTP sector is protected from program and erase operation. The OTP_LOCK bit can only be programmed once.

Note : In OTP mode, the WRSR command will ignore any input data and program OTP_LOCK bit to 1, user must clear the protect bits before enter OTP mode and program the OTP code, then execute WRSR command to lock the OTP sector before leaving OTP mode.

Read Information Register (RDIFR) (2Bh)

The Read Information Register (RDIFR) instruction is for reading the value of Information Register. The Read Information Register can be read at any time (even in program/erase/write status register condition) and continuously, as shown in Figure 10.

The sequence of issuing RDIFR instruction is: CS# goes low -> sending RDIFR instruction -> Information Register data out on DO -> CS# goes high.

The instruction sequence is shown in Figure 10.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

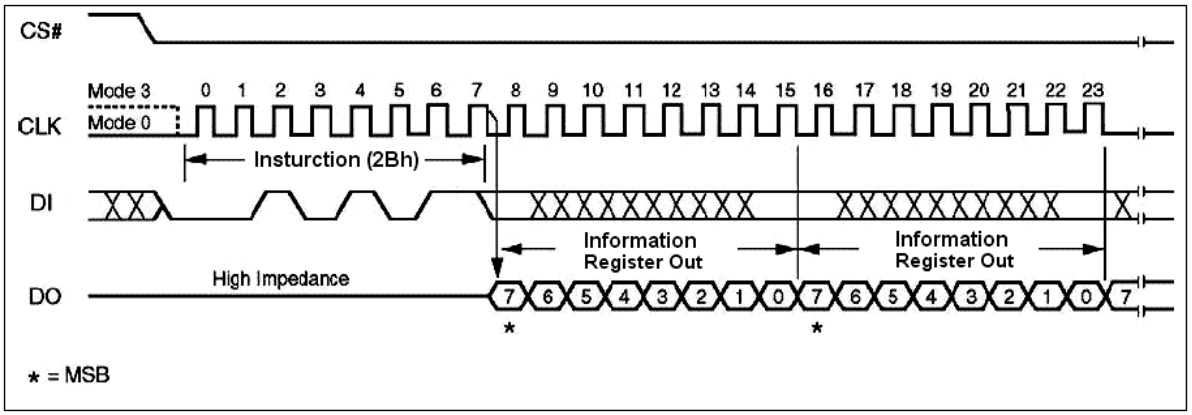


Figure 10. Read Information register Instruction Sequence Diagram

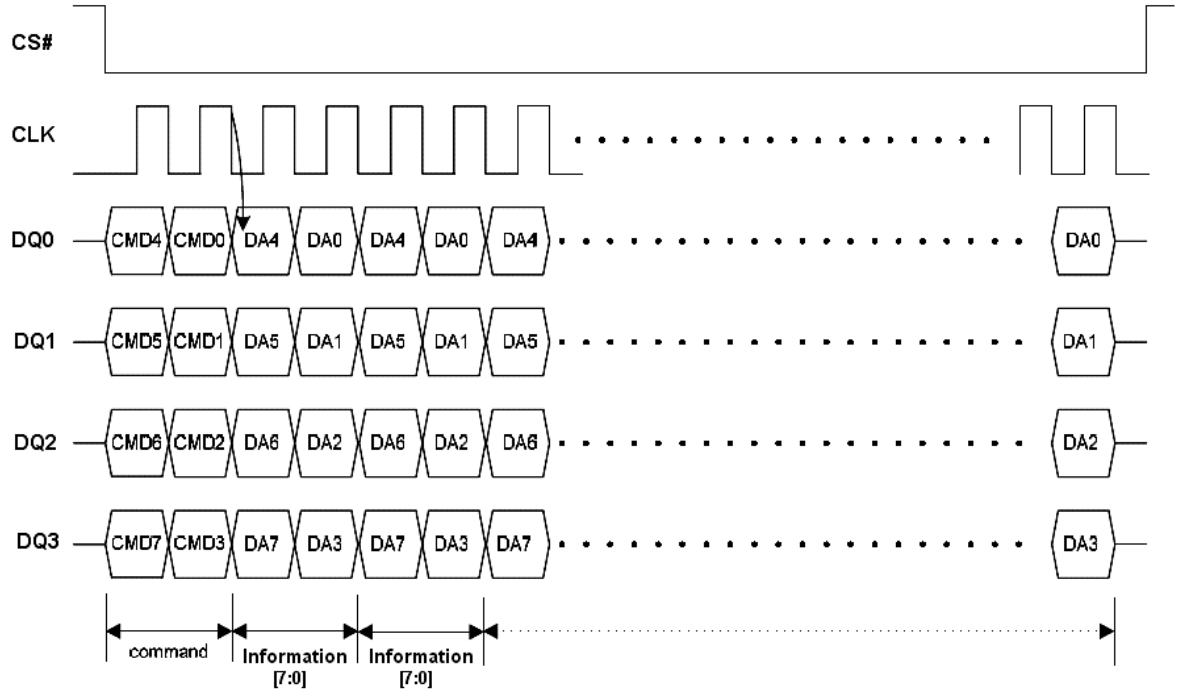


Figure 10.1 Read Information register Instruction Sequence under EQPI Mode

Table 7. Information Register Bit Locations

S7	S6	S5	S4	S3	S2	S1	S0
HBL (High Bank Latch bit)	Erase Fail Flag	Program Fail Flag	Reserved bit	Reserved bit	4 BYTE	OTP_LOCK bit	Reserved bit
1 = access larger than 128Mb 0 = access smaller than 128Mb (default = 0)	1 = indicate Erase failed 0 = normal Erase succeed (default = 0)	1 = indicate Program failed 0 = normal Program succeed (default = 0)			1 = 4-byte address mode 0 = 3-byte address mode (default = 0)	1 = OTP sector is protected	
volatile bit	volatile bit	volatile bit			volatile bit	non-volatile bit	
Read Only	Read Only	Read Only			Read Only	Read Only	

Note:

1. When executed the (RDIFR) (2Bh) command, the OTP_LOCK bit (S1) value is the same as OTP_LOCK bit (S7 / in OTP mode) in table 6.
2. Default at Power-up is “0”

The status and control bits of the Secured Register are as follows:

Reserved bit. Information register bit locations 0, 3 and 4 are reserved for future use. Current devices will read 0 for these bit locations. It is recommended to mask out the reserved bit when testing the Suspend Status Register. Doing this will ensure compatibility with future devices.

OTP_LOCK bit. The OTP_LOCK bit, user can read/program/erase OTP sector as normal sector while OTP_LOCK bit value is equal 0, after OTP_LOCK bit is programmed with 1 by WRSR command, the OTP sector is protected from program and erase operation. The OTP_LOCK bit can only be programmed once.

4 BYTE Indicator bit. By writing EN4B instruction, the 4 BYTE bit may be set to "1" to access the address length of 32-bit for higher density (large than 128Mb) memory area. The default state is "0", which means the mode of 24-bit address. The 4 BYTE bit may be clear by power off or writing EX4B instruction to reset the state to be "0"

Program Fail Flag bit. While a program failure happened, the Program Fail Flag bit would be set. This bit will also be set when the user attempts to program a protected main memory region or a locked OTP region. This bit can indicate whether one or more of program operations fail, and can be reset by Program (PP) or Erase (SE, BE or CE) instructions.

Erase Fail Flag bit. While an erase failure happened, the Erase Fail Flag bit would be set. This bit will also be set when the user attempts to erase a protected main memory region or a locked OTP region. This bit can indicate whether one or more of erase operations fail, and can be reset by Program (PP) or Erase (SE, BE or CE) instructions.

Note : For Program and Erase Flag bits,

1. The flag bits can be reset by power-on or that embedded mode was executed like WRSR, Erase or Program command.
2. If the system is trying to erase a locked block and then program a locked block. The erase fail or program fail flag bit will be high due to no successful Program, Erase or WRSE command.

HBL bit. The High Bank Latch (HBL) bit indicates the status of the internal High Bank Latch. By writing ENHB instruction, the HBL bit may be set to "1" to access the memory area of higher bank (larger than 128M). The default state is "0", which mean if execute read / program / erase command, then the first byte addresses will be accessed at the memory area of lower density (smaller than 128M). The HBL bit may be clear by power off or writing EXHBL instruction to reset the state to be "0"

Write Status Register (WRSR) (01h)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code and the data byte on Serial Data Input (DI).

The instruction sequence is shown in Figure 11. The Write Status Register (WRSR) instruction has no effect on S1 and S0 of the Status Register. Chip Select (CS#) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 3. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

The instruction sequence is shown in Figure 11.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

NOTE : In the OTP mode, WRSR command will ignore input data and program OTP_LOCK bit to 1.

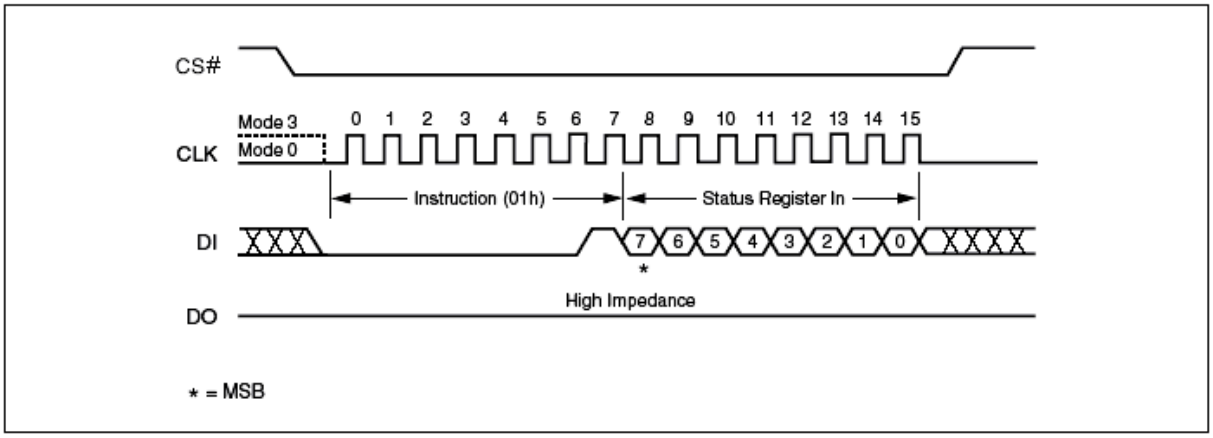


Figure 11. Write Status Register Instruction Sequence Diagram

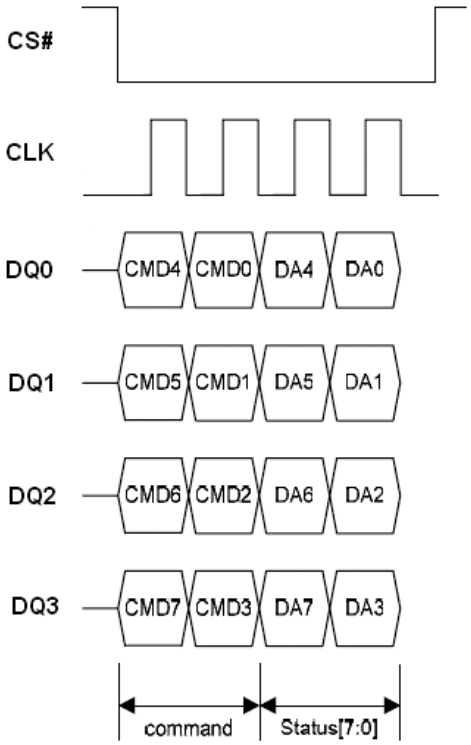


Figure 11.1 Write Status Register Instruction Sequence under EQPI Mode

Enter 4-byte mode (EN4B) (B7h)

The EN4B instruction enables accessing the address length of 32-bit for the memory area of higher density (larger than 128Mb). The device default is in 24-bit address mode; after sending out the EN4B instruction, the bit 2 (4 BYTE bit) of Information register will be automatically set to "1" to indicate the 4-byte address mode has been enabled. Once the 4-byte address mode is enable, the address length becomes 32-bit instead of the default 24-bit. There are two methods to exit the 4-byte mode: power-off or writing exit 4-byte mode (EX4B) instruction.

All instructions are accepted normally, and just the address bit is changed form 24-bit to 32-bit.

The sequence of issuing EN4B instruction is: CS# goes low -> sending EN4B instruction to enter 4-byte mode (automatically set 4 BYTE bit as "1") -> CS# goes high, as shown in Figure 12.

The instruction sequence is shown in Figure 13.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

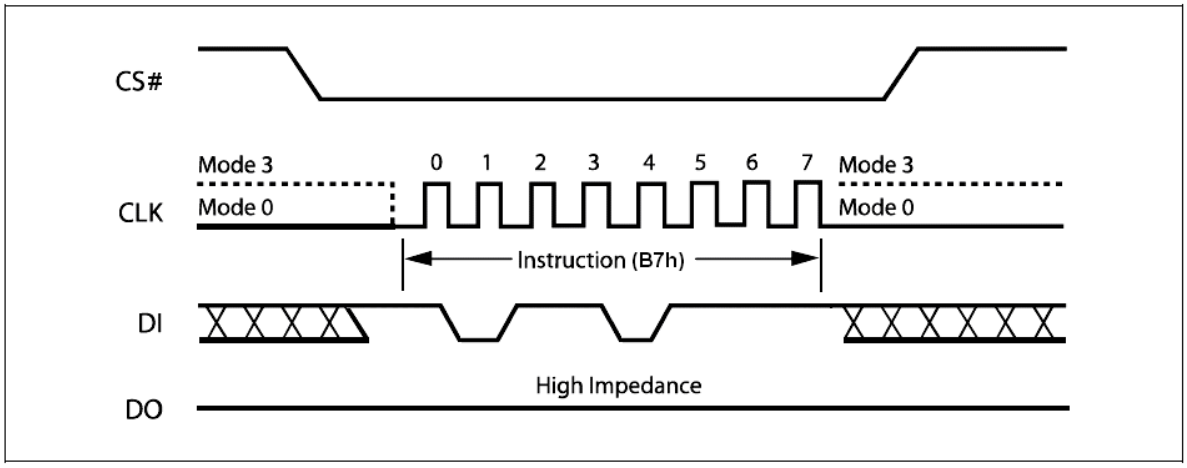


Figure 12. Enter 4-byte mode Instruction Sequence Diagram

Exit 4-byte mode (EX4B) (E9h)

The EX4B instruction is executed to exit the 4-byte address mode and return to the default 3-bytes address mode. After sending out the EX4B instruction, the bit 2 (4 BYTE bit) of Information register will be cleared to be ”0” to indicate the exit of the 4-byte address mode. Once exiting the 4-byte address mode, the address length will return to 24-bit.

The sequence of issuing EX4B instruction is: CS# goes low -> sending EX4B instruction to exit 4-byte mode (automatically clear the 4 BYTE bit to be “0”) -> CS# goes high, as shown in Figure 13.

The instruction sequence is shown in Figure 13.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

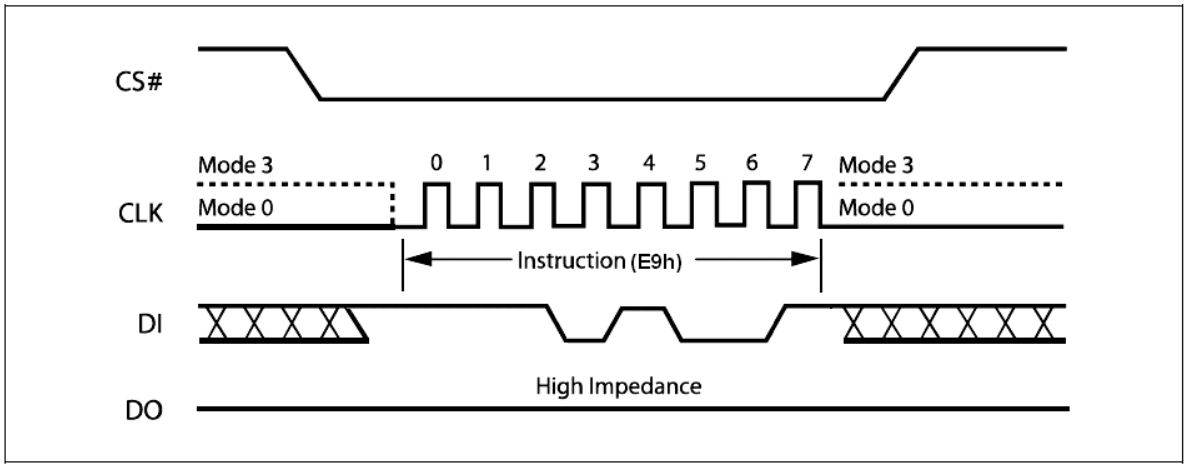


Figure 13. Exit 4-byte mode Instruction Sequence Diagram

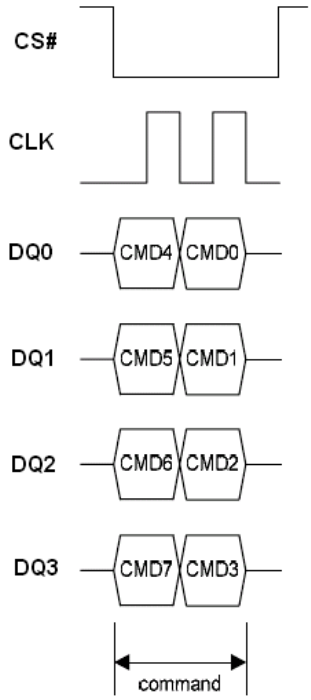


Figure 13.1 Enter / Exit 4-byte mode Instruction Sequence under EQPI Mode

Enter High Bank Latch mode (ENHBL) (67h)

The High Bank Latch mode (ENHBL) instruction enables the first byte addresses was accessed at the memory area of higher bank (larger than 128Mb) while execute the read / program / erase command, that means the address 24-bit was asserted high after entering this mode. In other words, for read / program / erase command the Host system can also access the addresses from 1000000h to 1FFFFFF even if without inputting 4 byte address. The device default is in the memory area of lower bank (smaller than 128M); after sending out the ENHBL instruction, the bit 7 (HBL bit) of Information register will be automatically set to "1" to indicate the High Bank Latch has been enabled. Once the High Bank Latch mode is enable, if execute read / program / erase command, then the first byte addresses will be accessed at memory area of the higher bank (larger than 128Mb) instead of the default the memory area lower bank (smaller than 128M).

There are some methods that can exit the High Bank Latch mode: power-off, or by writing Reset Quad I/O (RSTQIO), Enter 4-byte mode (EN4B) and Exit High Bank Latch mode (EXHBL) instructions.

The sequence of issuing ENHBL instruction is: CS# goes low -> sending ENHBL instruction to enter High Bank Latch mode (automatically set HBL bit as "1") -> CS# goes high, as shown in Figure 14.

The instruction sequence is shown in Figure 15.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

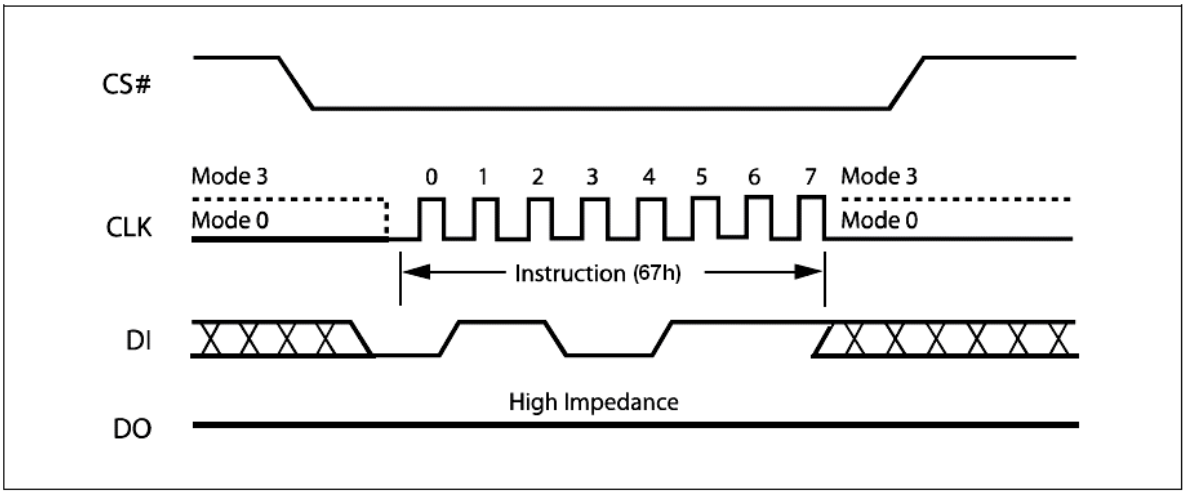


Figure 14. Enter High Bank Latch mode Instruction Sequence Diagram

Exit High Bank Latch mode (EXHBL) (98h)

The Exit High Bank Latch Mode (EXHBL) instruction is executed to exit the High Bank Latch mode and then return to the default state: the first byte addresses was accessed at memory area of lower bank (smaller than 128M) while execute the read / program / erase command. After sending out the EXHBL instruction, the bit 7 (HBL bit) of Information register will be cleared to be ”0” to indicate the exit of the High Bank Latch mode. Once the exit the High Bank Latch mode is enable, if executed the read / program / erase command then the first byte addresses will be accessed at memory area of lower bank (smaller than 128M).

The sequence of issuing EXHBL instruction is: CS# goes low -> sending EXHBL instruction to Exit High Bank Latch mode (automatically clear the HBL bit to be “0”) -> CS# goes high, as shown in Figure 15.

The instruction sequence is shown in Figure 15.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

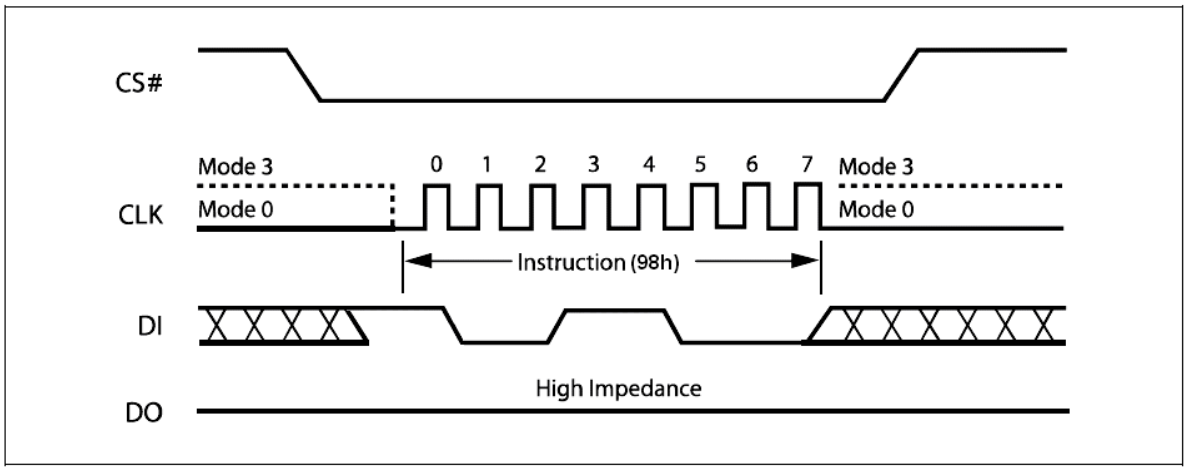


Figure 15. Exit High Bank Latch mode Instruction Sequence Diagram

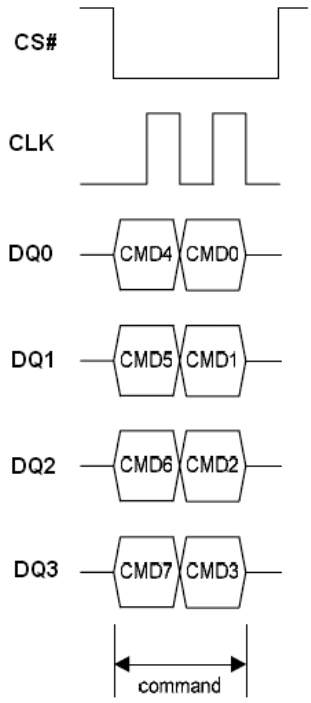


Figure 15.1 Enter / Exit High Bank Latch mode Instruction Sequence under EQPI Mode

Read Data Bytes (READ) (03h)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte or 4-byte address (depending on mode state), each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 16. The first byte addresses can be at any location. To access higher address (larger than 128Mb), there are two methods. One is the Enter 4-byte mode (B7h) command and the other is the Enter High Bank Latch Mode (67h) command. For these methods, the address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

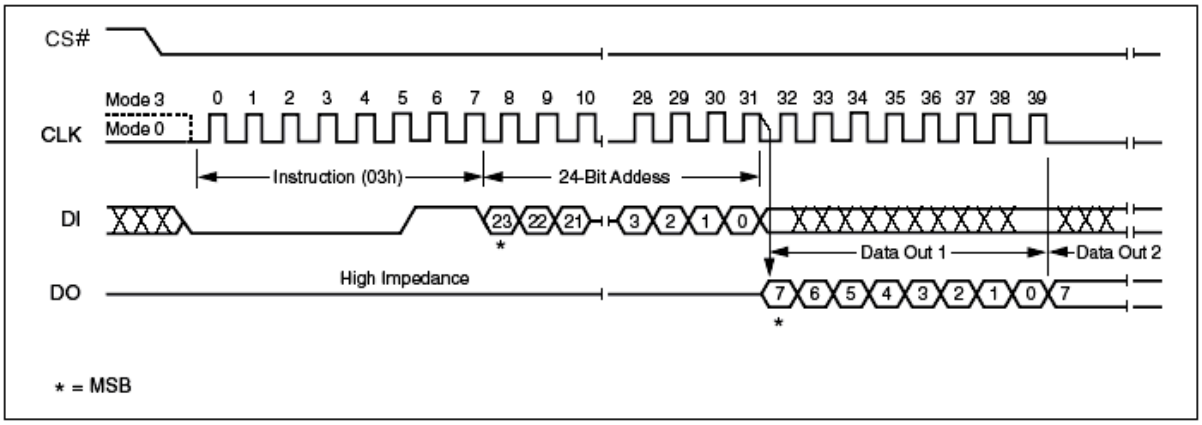


Figure 16. Read Data Instruction Sequence Diagram

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Read Data Bytes at Higher Speed (FAST_READ) (0Bh)

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte or 4-byte address (depending on mode state) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency F_R, during the falling edge of Serial Clock (CLK).

The instruction sequence is shown in Figure 17. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

The instruction sequence is shown in Figure 17.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

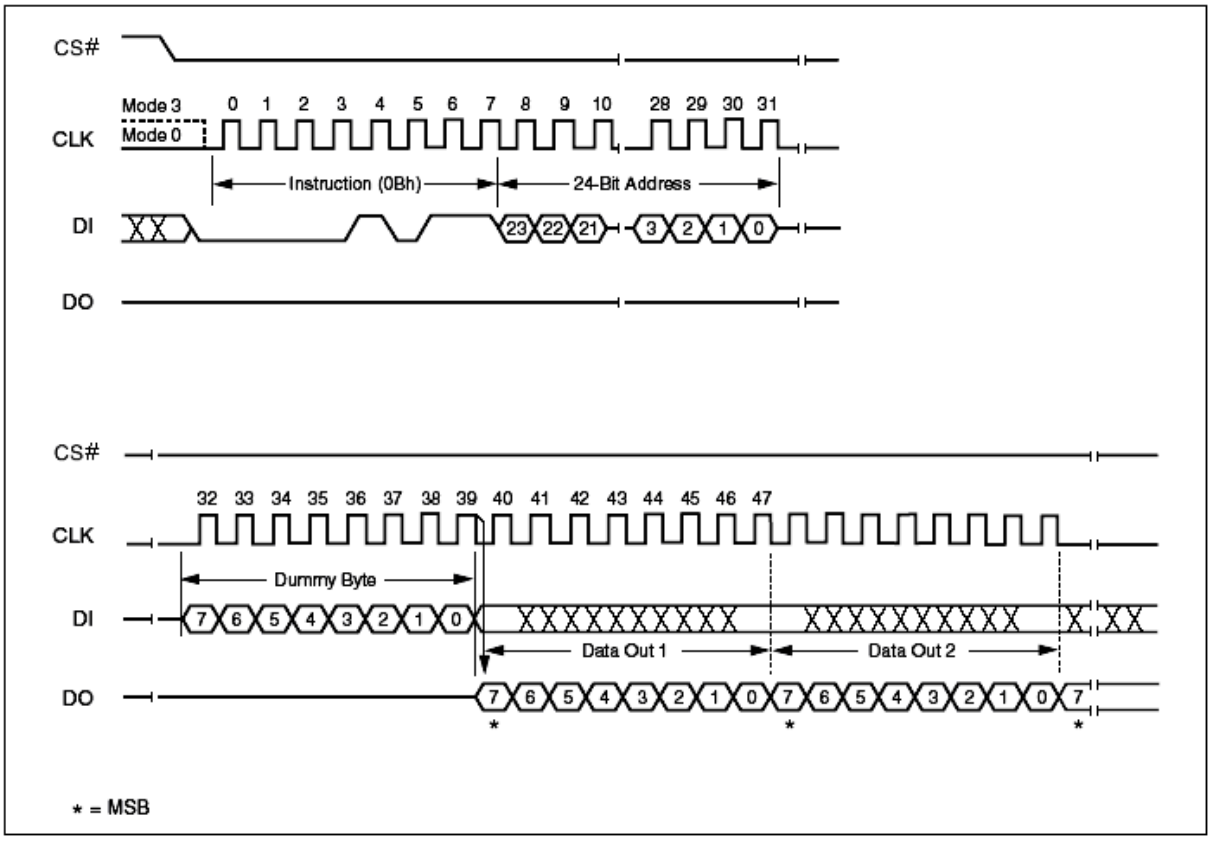


Figure 17. Fast Read Instruction Sequence Diagram

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

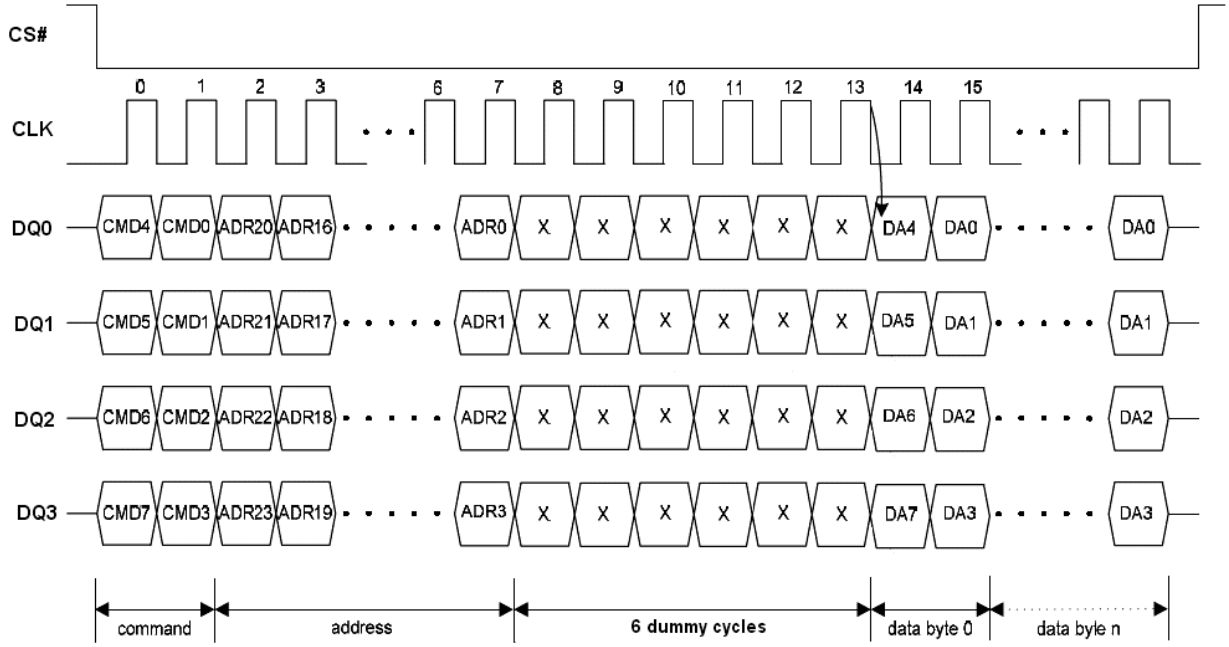


Figure 17.1 Fast Read Instruction Sequence under EQPI Mode

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Dual Output Fast Read (3Bh)

The Dual Output Fast Read (3Bh) is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins, DQ_0 and DQ_1, instead of just DQ_0. This allows data to be transferred from the EN25QH256 at twice the rate of standard SPI devices. The Dual Output Fast Read instruction is ideal for quickly downloading code from to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Dual Output Fast Read instruction can operation at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding eight "dummy clocks after the 3-byte or 4-byte address (depending on mode state) as shown in Figure 18. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clock is "don't care". However, the DI pin should be high-impedance prior to the falling edge of the first data out clock.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

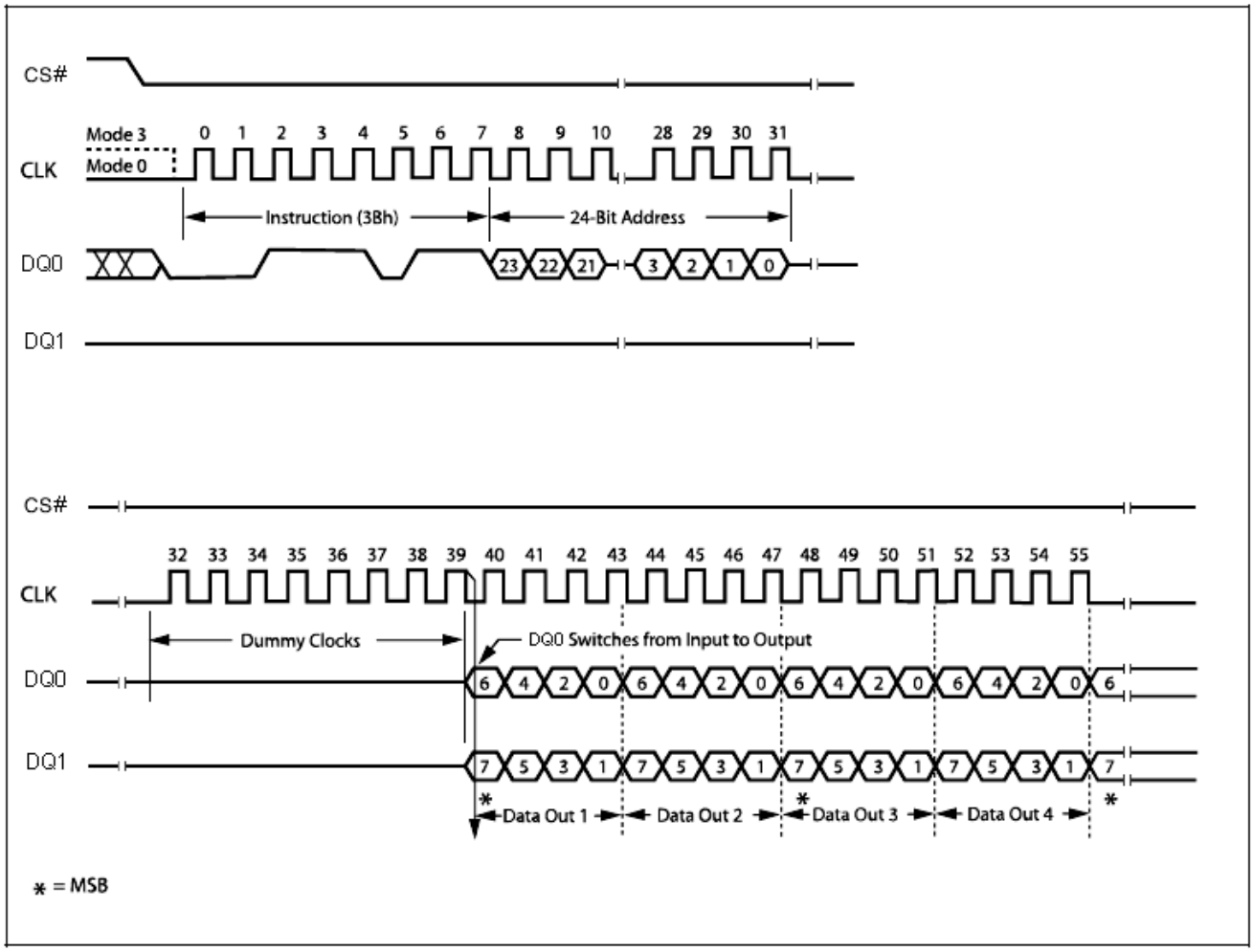


Figure 18. Dual Output Fast Read Instruction Sequence Diagram

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Dual Input / Output FAST_READ (BBh)

The Dual I/O Fast Read (BBh) instruction allows for improved random access while maintaining two IO pins, DQ_0 and DQ_1. It is similar to the Dual Output Fast Read (3Bh) instruction but with the capability to input the Address bits (3-byte or 4-byte, depending on mode state) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The Dual I/O Fast Read instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of CLK, and data of every two bits (interleave 2 I/O pins) shift out on the falling edge of CLK at a maximum frequency. The first address can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Dual I/O Fast Read instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing Dual I/O Fast Read instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit, as shown in Figure 19.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

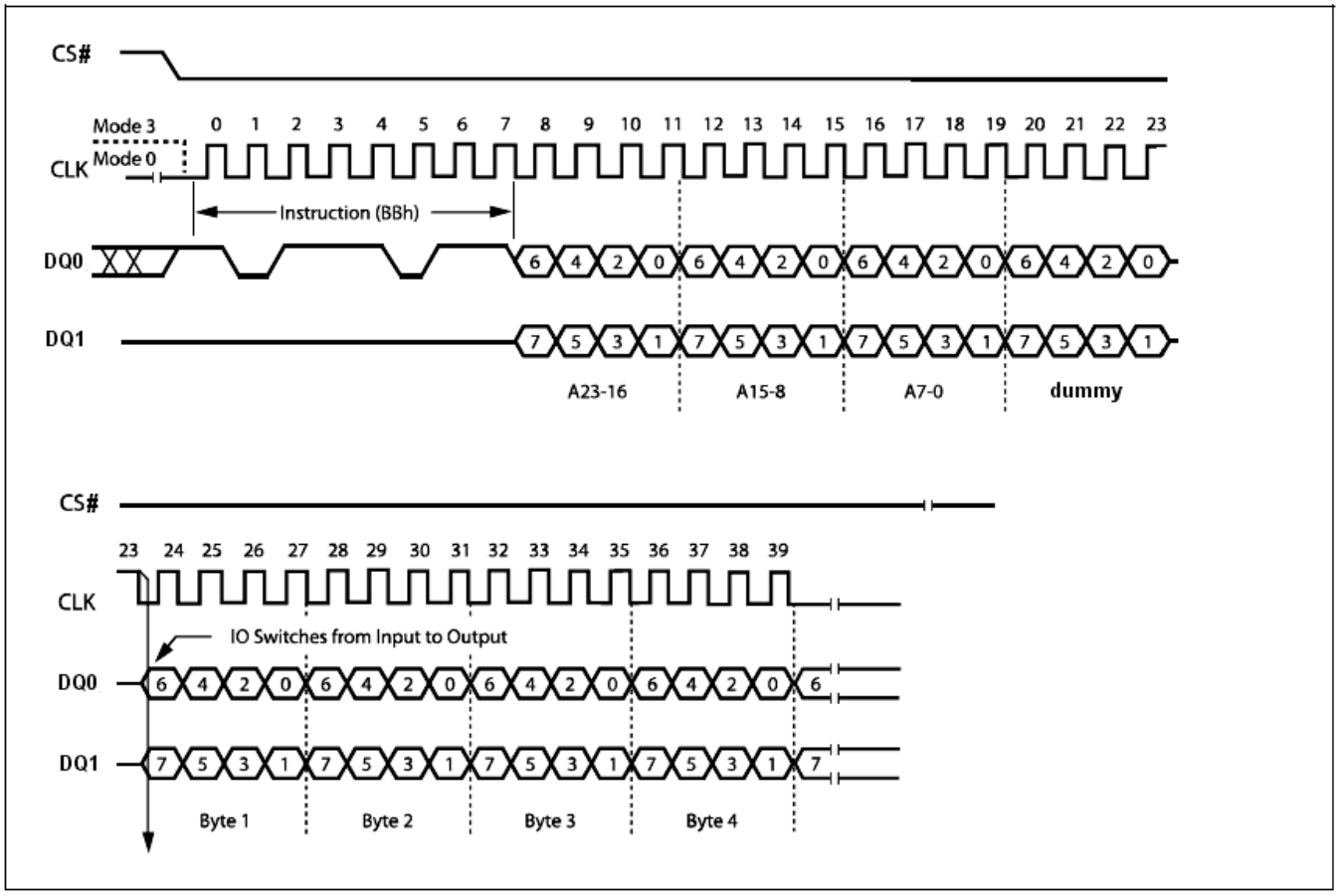


Figure 19. Dual Input / Output Fast Read Instruction Sequence Diagram

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Quad Input / Output FAST_READ (EBh)

The Quad Input/Output FAST_READ (EBh) instruction is similar to the Dual I/O Fast Read (BBh) instruction except that address (3-byte or 4-byte, depending on mode state) and data bits are input and output through four pins, DQ_0, DQ_1, DQ_2 and DQ_3 and six dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The Quad Input/Output FAST_READ (EBh) instruction enable quad throughput of Serial Flash in read mode.

The address is latching on rising edge of CLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of CLK at a maximum frequency F_R. The first address can be any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single Quad Input/Output FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing Quad Input/Output FAST_READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The default read mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The sequence of issuing Quad Input/Output FAST_READ (EBh) instruction is: CS# goes low -> sending Quad Input/Output FAST_READ (EBh) instruction -> 24-bit or 32-bit address (depending on mode state) interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> 6 dummy cycles -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> to end Quad Input/Output FAST_READ (EBh) operation can use CS# to high at any time during data out, as shown in Figure 20.

The instruction sequence is shown in Figure 20.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

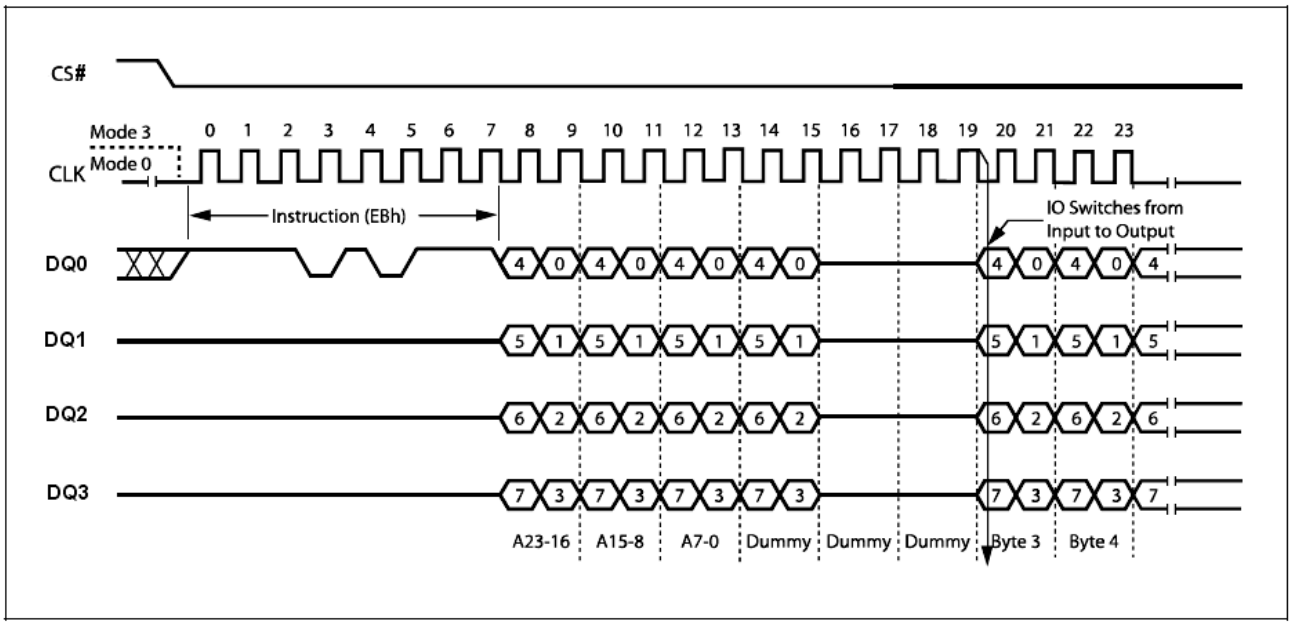


Figure 20. Quad Input / Output Fast Read Instruction Sequence Diagram

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

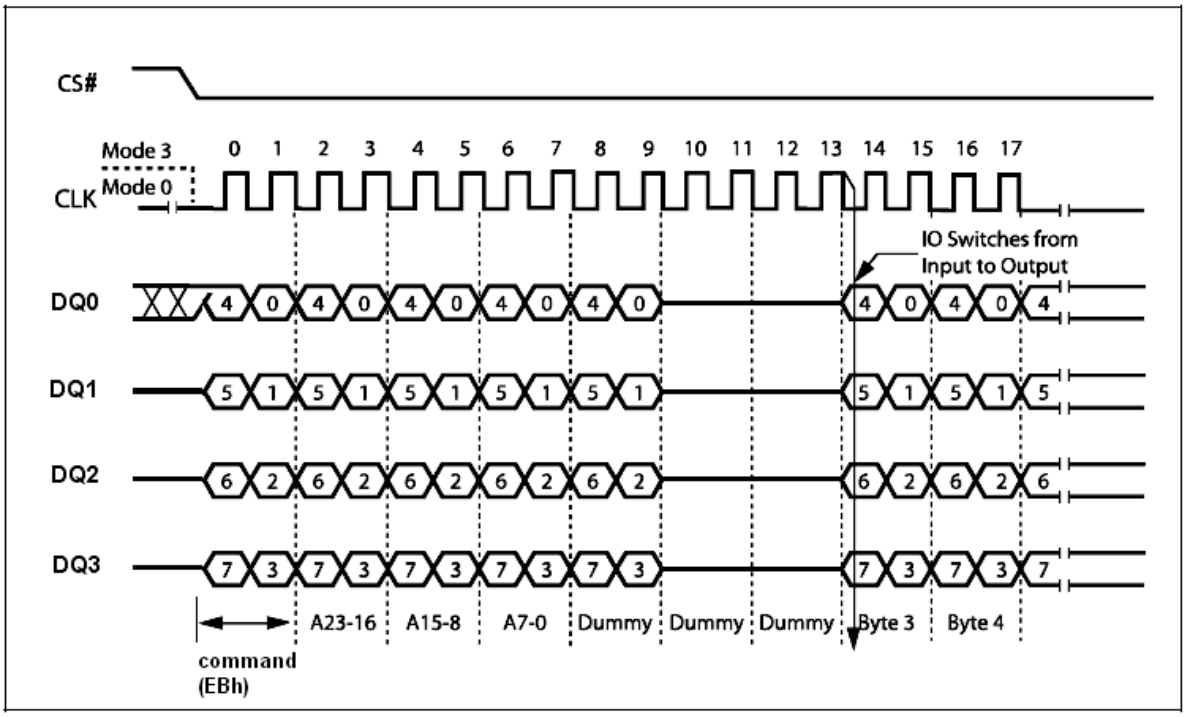


Figure 20.1. Quad Input / Output Fast Read Instruction Sequence under EQPI Mode

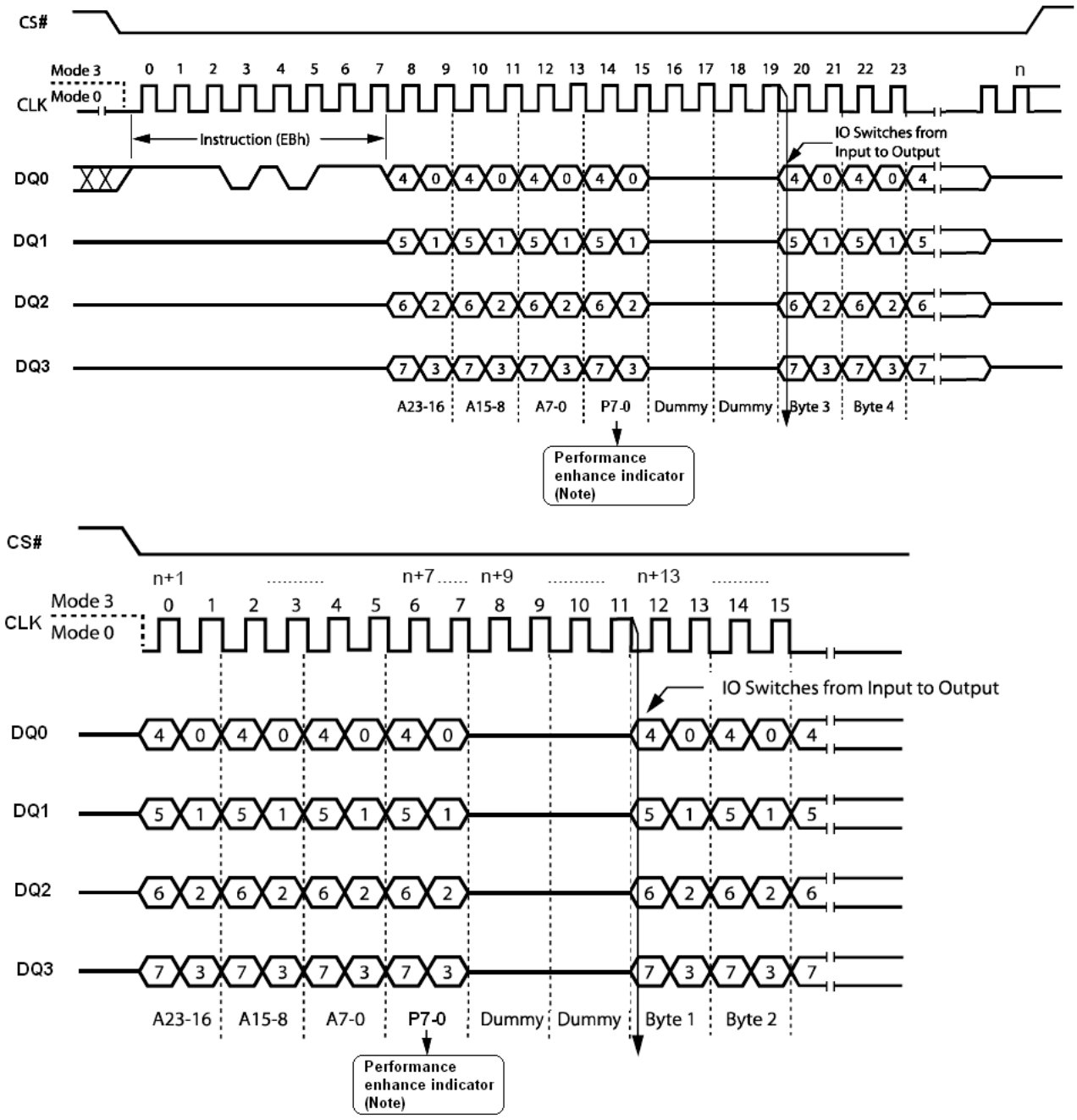
Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Another sequence of issuing Quad Input/Output FAST_READ (EBh) instruction especially useful in random access is : CS# goes low -> sending Quad Input/Output FAST_READ (EBh) instruction -> 24-bit address interleave on DQ_3, DQ_2, DQ_1 and DQ_0 -> performance enhance toggling bit P[7:0] -> 4 dummy cycles -> data out interleave on DQ_3, DQ_2, DQ_1 and DQ_0 till CS# goes high -> CS# goes low (reduce Quad Input/Output FAST_READ (EBh) instruction) -> 24-bit or 32-bit random access address (depending on mode state), as shown in Figure 21.

In the performance – enhancing mode, P[7:4] must be toggling with P[3:0] ; likewise P[7:0] = A5h, 5Ah, F0h or 0Fh can make this mode continue and reduce the next Quad Input/Output FAST_READ (EBh) instruction. Once P[7:4] is no longer toggling with P[3:0] ; likewise P[7:0] = FFh, 00h, AAh or 55h. And afterwards CS# is raised, the system then will escape from performance enhance mode and return to normal operation.

While Program/ Erase/ Write Status Register is in progress, Quad Input/Output FAST_READ (EBh) instruction is rejected without impact on the Program/ Erase/ Write Status Register current cycle.

The instruction sequence is shown in Figure 21.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.



Note: Performance enhance mode, if P7 ≠ P3 & P6 ≠ P2 & P5 ≠ P1 & P4 ≠ P0 (Toggling), ex: A5, 5A, 0F
Reset the performance enhance mode, if P7 = P3 or P6 = P2 or P5 = P1 or P4 = P0, ex: AA, 00, FF

Figure 21. Quad Input/Output Fast Read Enhance Performance Mode Sequence Diagram

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

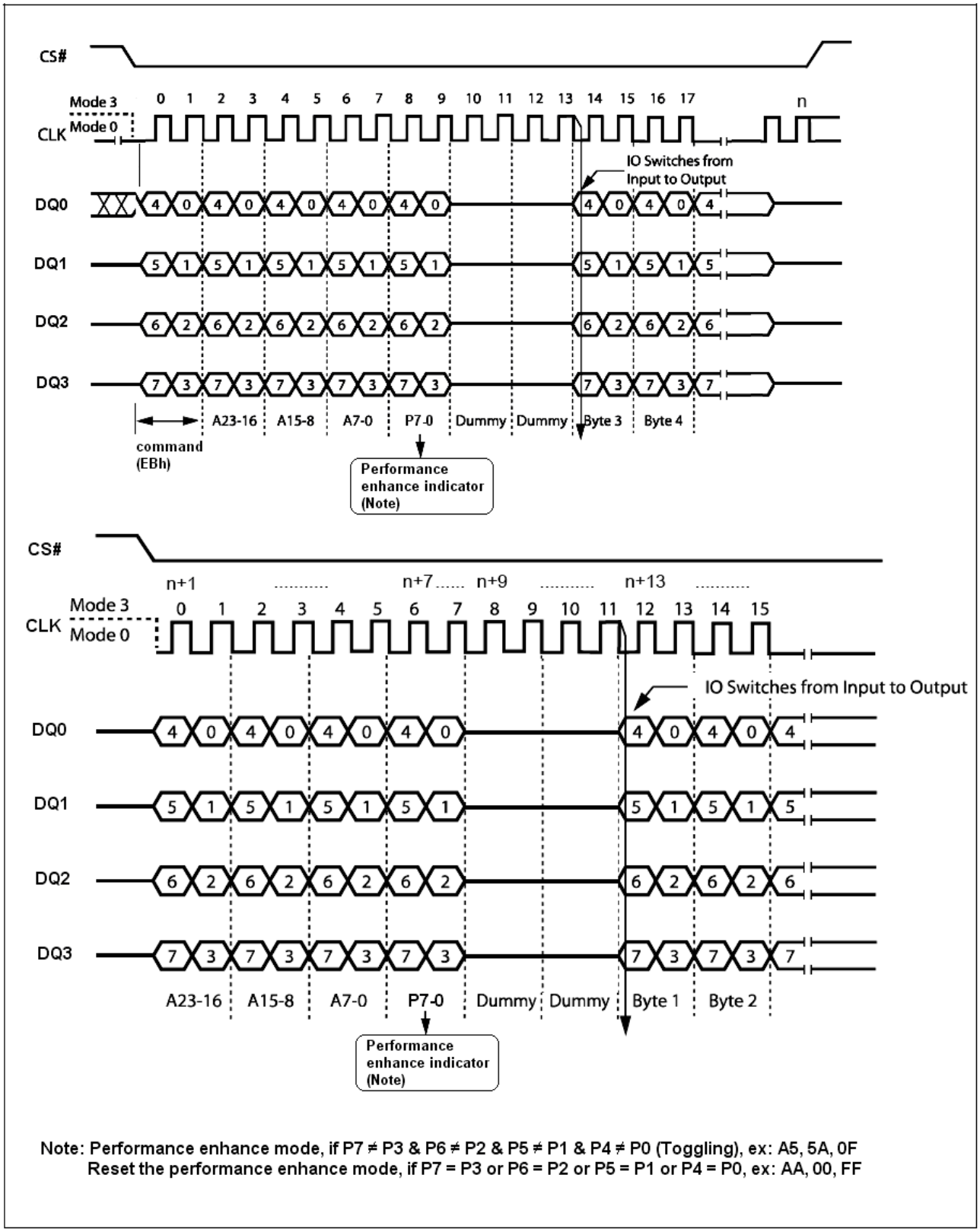


Figure 21.1 Quad Input/Output Fast Read Enhance Performance Mode Sequence under EQPI Mode

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Page Program (PP) (02h)

The Page Program (PP) instruction allows bytes to be programmed in the memory. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, three or four address bytes (depending on mode state) and at least one data byte on Serial Data Input (DI). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select (CS#) must be driven Low for the entire duration of the sequence.
The instruction sequence is shown in Figure 22. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

The default mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

Chip Select (CS#) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select (CS#) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (BP3, BP2, BP1, BP0) bits (see Table 3) is not executed.

The instruction sequence is shown in Figure 22.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

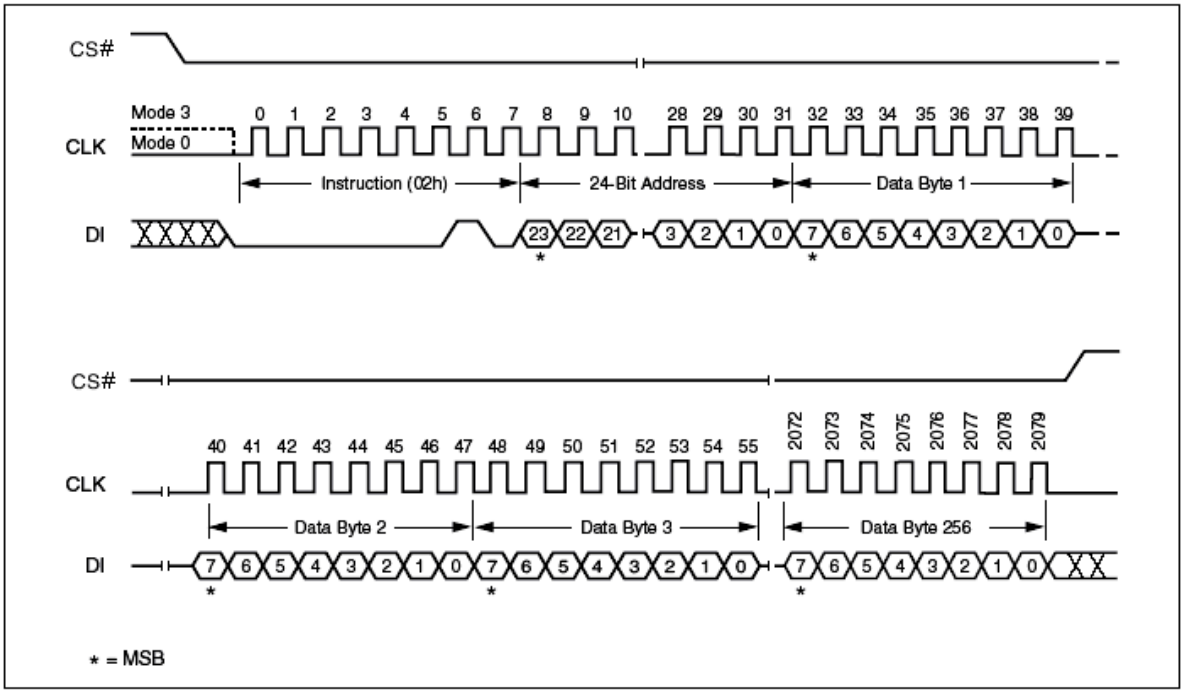


Figure 22. Page Program Instruction Sequence Diagram

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

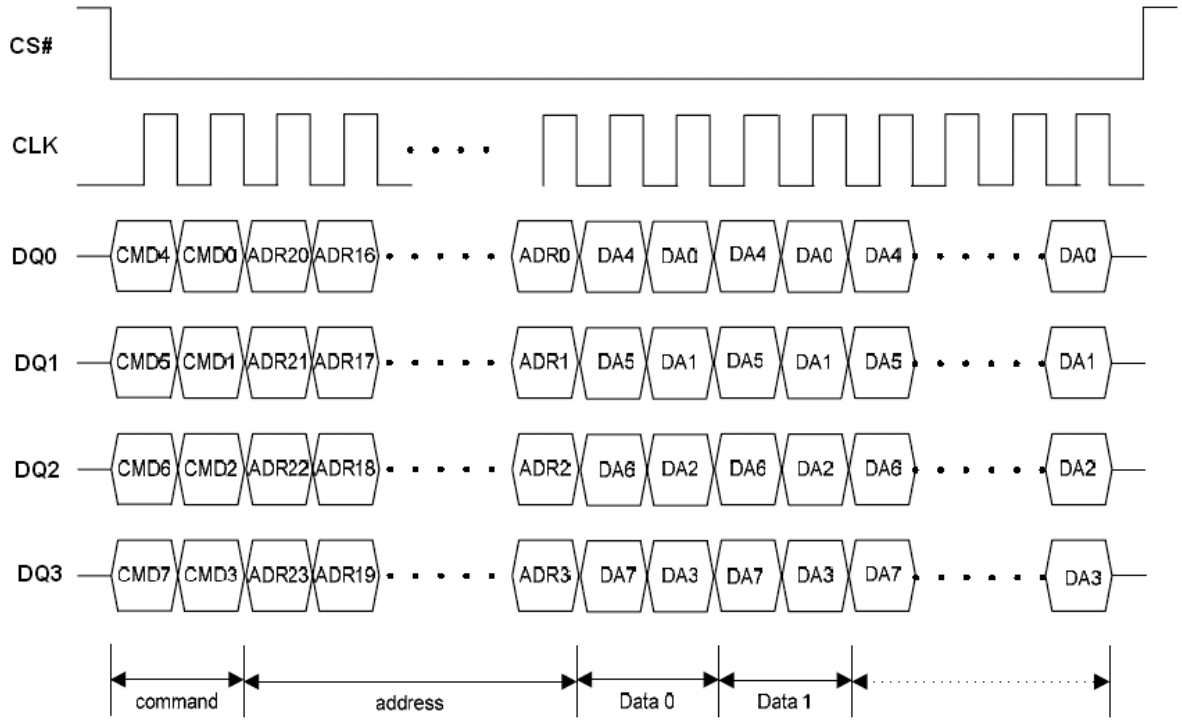


Figure 22.1 Program Instruction Sequence under EQPI Mode

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Sector Erase (SE) (20h)

The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three or four address bytes (depending on mode state) on Serial Data Input (DI). Any address inside the Sector (see Table 2) is a valid address for the Sector Erase (SE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The default mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The instruction sequence is shown in Figure 23. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Sector Erase (SE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A Sector Erase (SE) instruction applied to a sector which is protected by the Block Protect (BP3, BP2, BP1, BP0) bits (see Table 3) is not executed.

The instruction sequence is shown in Figure 24.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

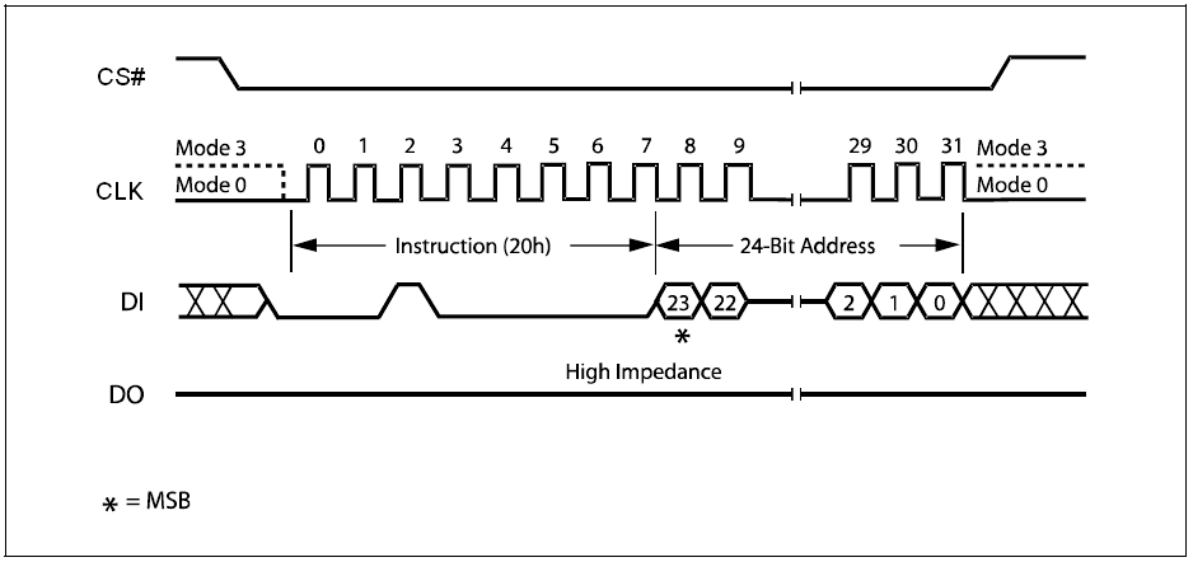


Figure 23. Sector Erase Instruction Sequence Diagram

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Block Erase (BE) (D8h)

The Block Erase (BE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Block Erase (BE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code, and three or four address bytes (depending on mode state) on Serial Data Input (DI). Any address inside the Block (see Table 2) is a valid address for the Block Erase (BE) instruction. Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The default mode is 3-byte address, to access higher address (4-byte address) which requires to enter the 4-byte address read mode. To enter the 4-byte mode, please refer to the enter 4-byte mode (EN4B) Mode section.

The instruction sequence is shown in Figure 24. Chip Select (CS#) must be driven High after the eighth bit of the last address byte has been latched in, otherwise the Block Erase (BE) instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A Block Erase (BE) instruction applied to a block which is protected by the Block Protect (BP3, BP2, BP1, BP0) bits (see Table 3) is not executed.

The instruction sequence is shown in Figure 24.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

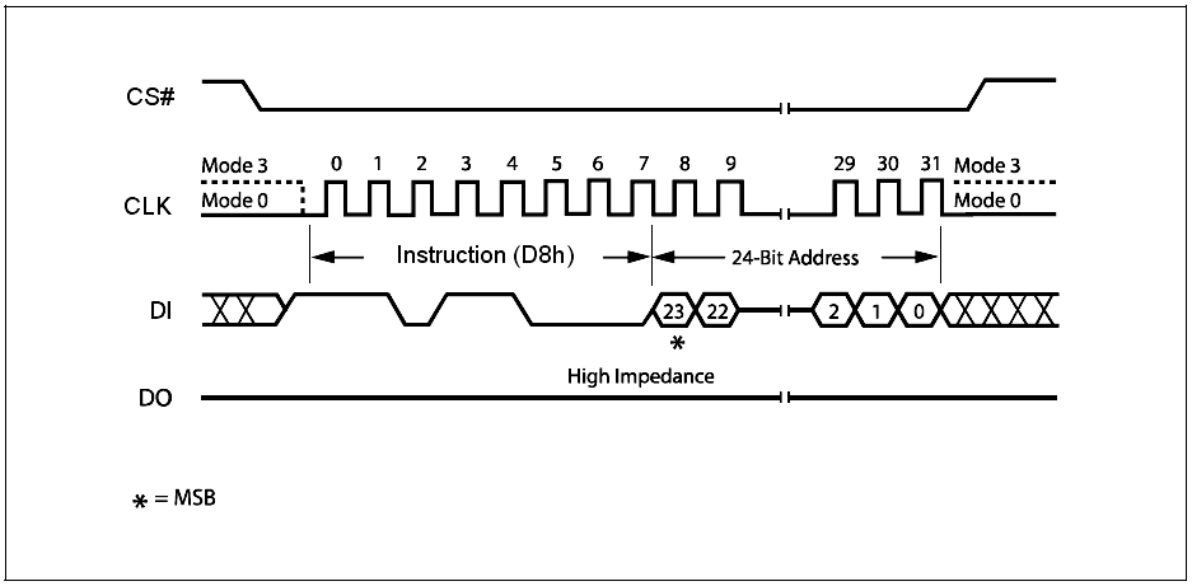


Figure 24. Block Erase Instruction Sequence Diagram

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

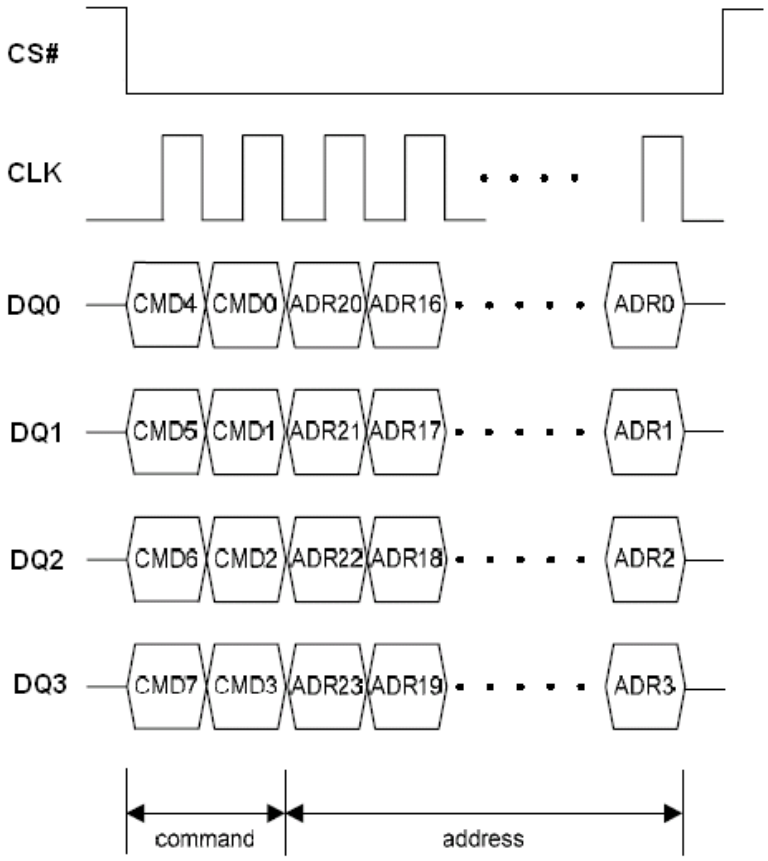


Figure 24.1 Block/Sector Erase Instruction Sequence under EQPI Mode

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Chip Erase (CE) (C7h/60h)

The Chip Erase (CE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Chip Erase (CE) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 25. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Chip Erase instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Chip Erase (CE) instruction is executed only if all Block Protect (BP3, BP2, BP1, BP0) bits are 0. The Chip Erase (CE) instruction is ignored if one, or more blocks are protected.

The instruction sequence is shown in Figure 25.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

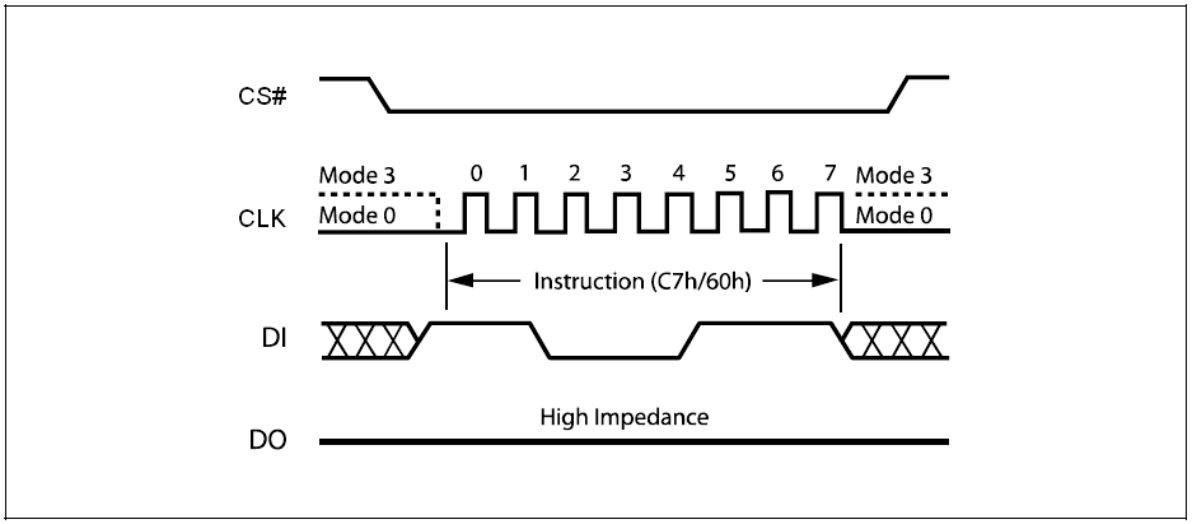


Figure 25. Chip Erase Instruction Sequence Diagram

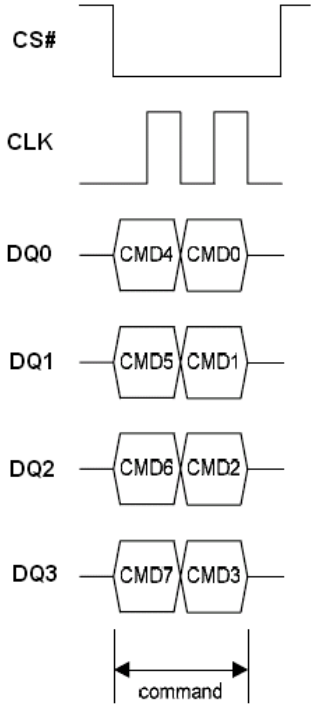


Figure 25.1 Chip Erase Sequence under EQPI Mode

Deep Power-down (DP) (B9h)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select (CS#) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in Table 13.)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Device ID (RDI) instruction also allows the Device ID of the device to be output on Serial Data Output (DO).

The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode. The Deep Power-down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (DI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 26. Chip Select (CS#) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select (CS#) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

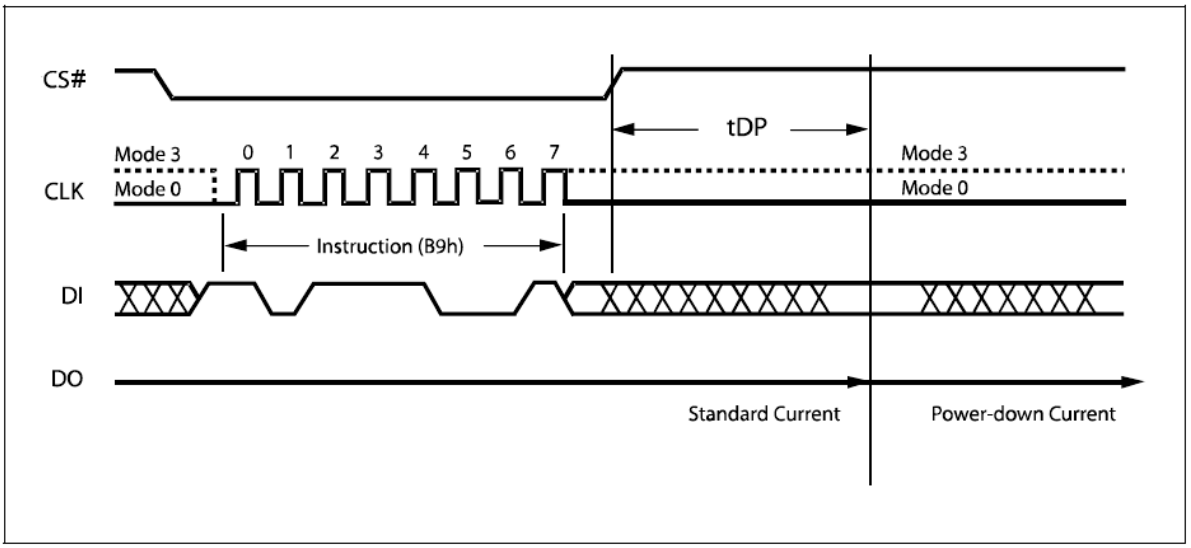


Figure 26. Deep Power-down Instruction Sequence Diagram

Release from Deep Power-down and Read Device ID (RDI)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Device ID (RDI) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

Please note that this is not the same as, or even a subset of, the JEDEC 16-bit Electronic Signature that is read by the Read Identifier (RDID) instruction. The old-style Electronic Signature is supported for reasons of backward compatibility, only, and should not be used for new designs. New designs should, instead, make use of the JEDEC 16-bit Electronic Signature, and the Read Identifier (RDID) instruction.

When used only to release the device from the power-down state, the instruction is issued by driving the CS# pin low, shifting the instruction code “ABh” and driving CS# high as shown in Figure 27. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the CS# pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 28. The Device ID value for the EN25QH256 are listed in Table 5. The Device ID can be read continuously. The instruction is completed by driving CS# high.

When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Standby Power mode is delayed by t_{RES2}, and Chip Select (CS#) must remain High for at least t_{RES2} (max), as specified in Table 15. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Device ID (RDI) instruction always provides access to the 8bit Device ID of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Device ID (RDI) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

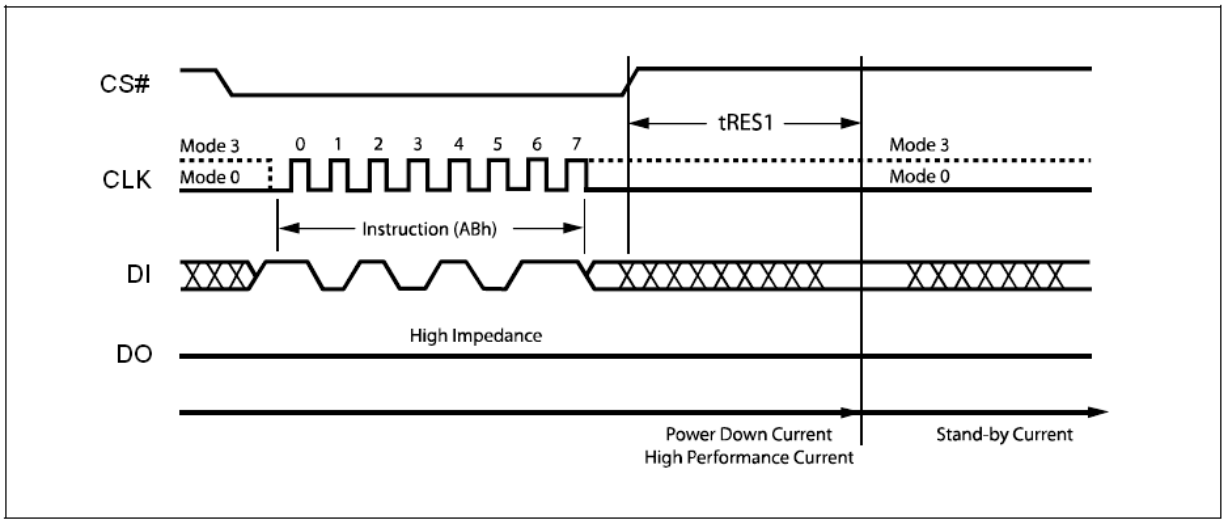


Figure 27. Release Power-down Instruction Sequence Diagram

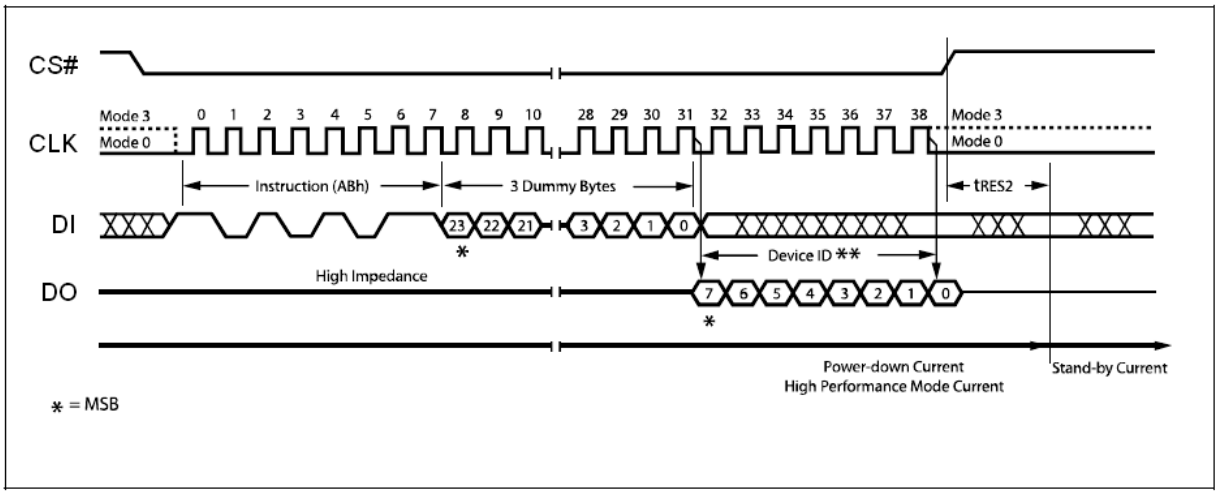


Figure 28. Release Power-down / Device ID Instruction Sequence Diagram

Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the CS# pin low and shifting the instruction code "90h" followed by a 24-bit or 32-bit address (depending on mode state) of 000000h. After which, the Manufacturer ID for Eon (1Ch) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 29. The Device ID values for the EN25QH256 are listed in Table 5. If the 24-bit or 32-bit address (depending on mode state) is initially set to 000001h the Device ID will be read first

The instruction sequence is shown in Figure 29.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

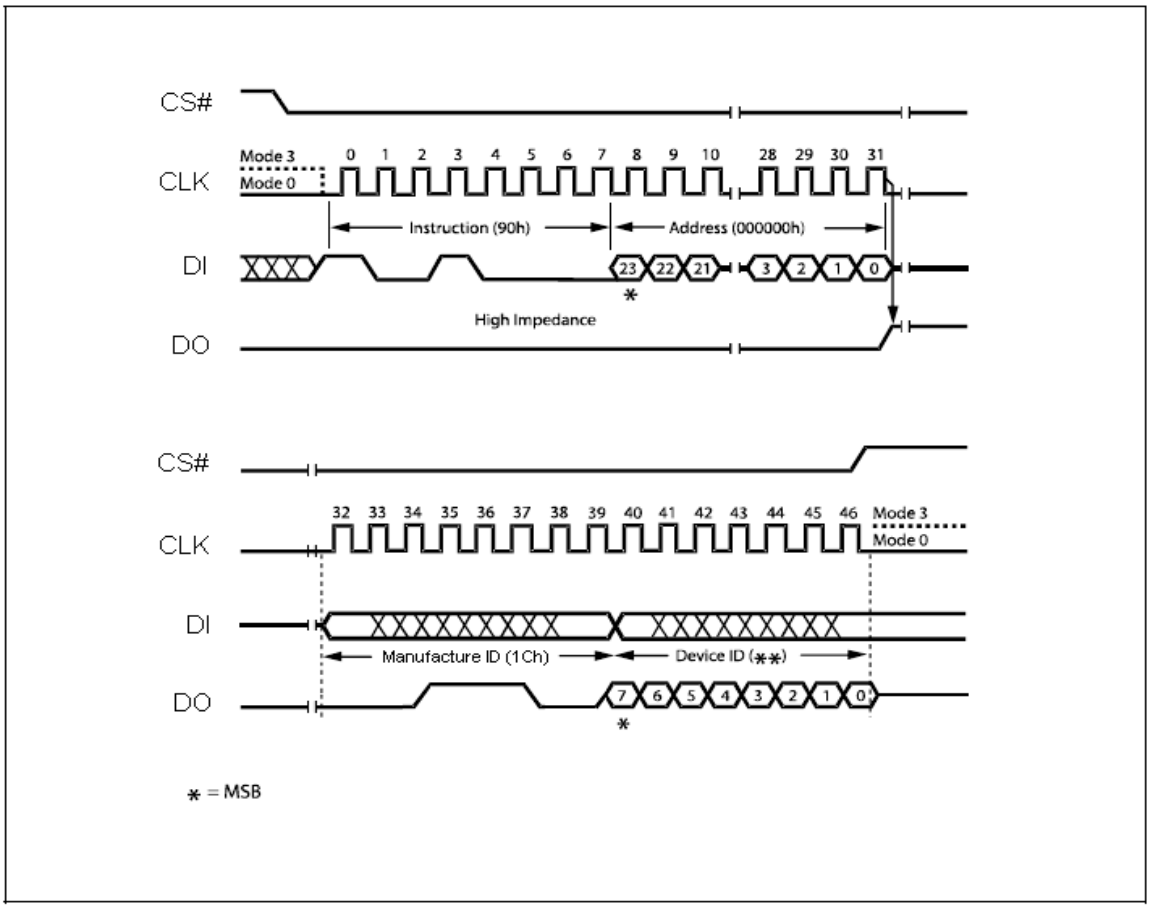


Figure 29. Read Manufacturer / Device ID Diagram

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

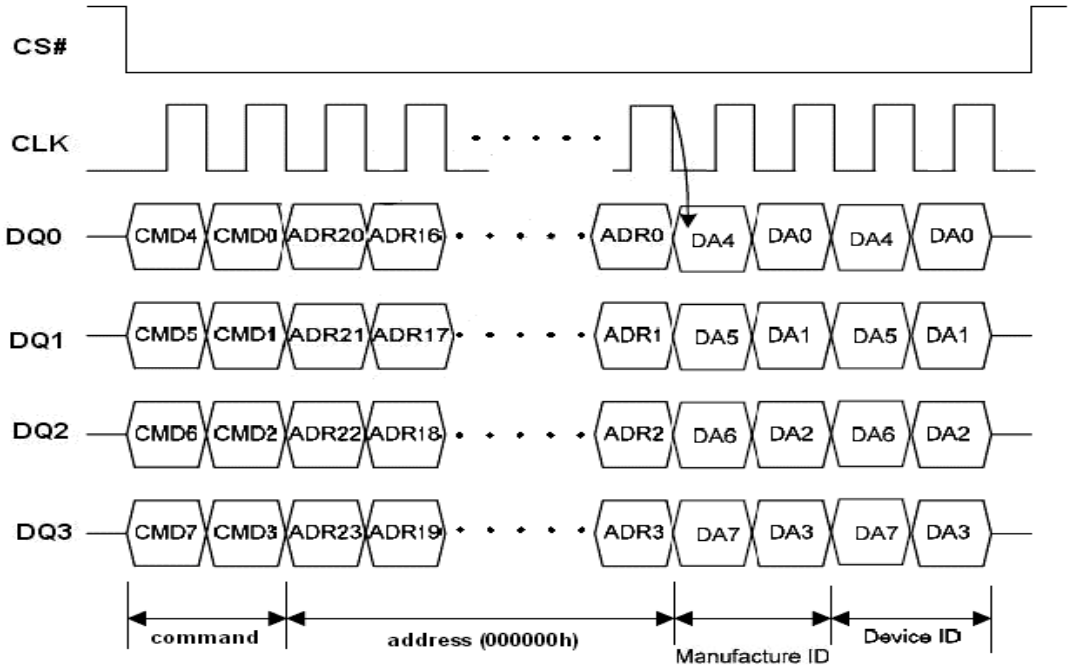


Figure 29.1. Read Manufacturer / Device ID Diagram under EQPI Mode

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Read Identification (RDID) (9Fh)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte , and the memory capacity of the device in the second byte .

Any Read Identification (RDID) instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) instruction should not be issued while the device is in Deep Power down mode.

The device is first selected by driving Chip Select Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The instruction sequence is shown in Figure 30. The Read Identification (RDID) instruction is terminated by driving Chip Select High at any time during data output.

When Chip Select is driven High, the device is put in the Standby Power mode. Once in the Standby Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

The instruction sequence is shown in Figure 30.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

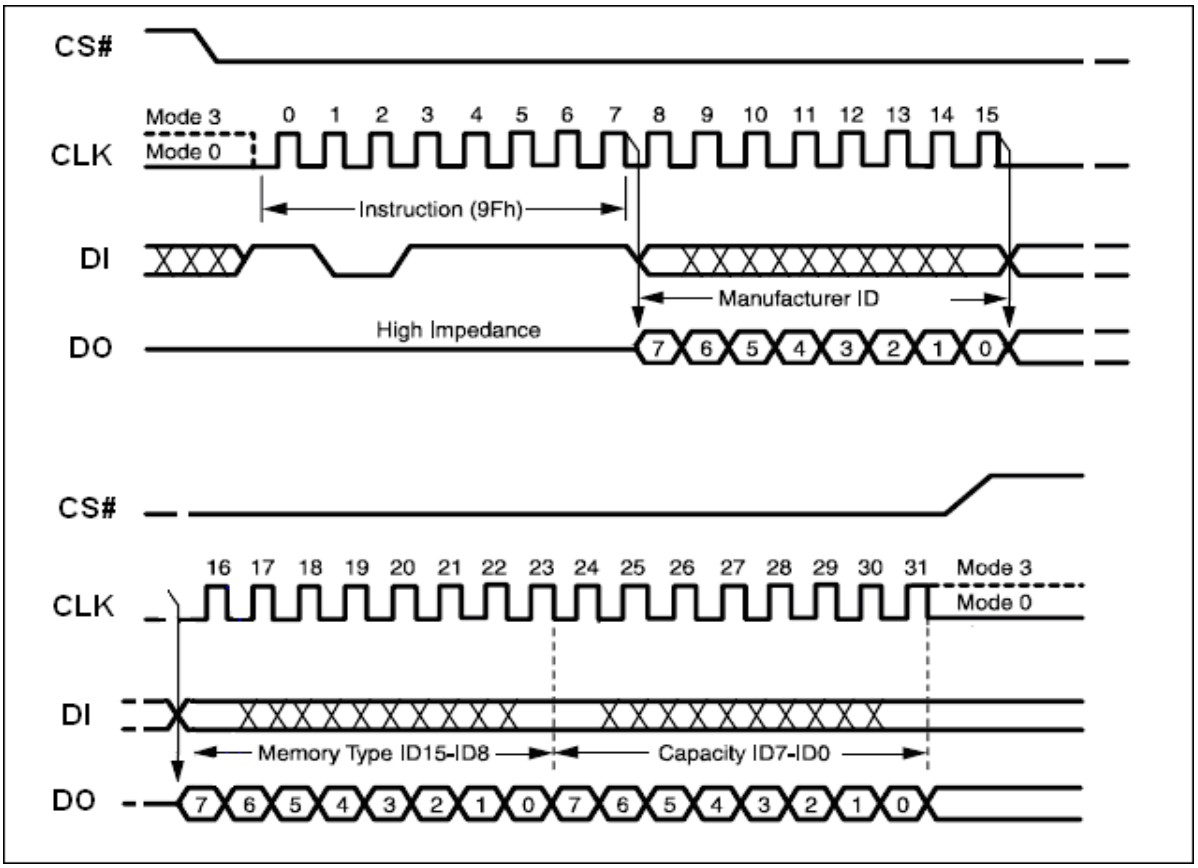


Figure 30. Read Identification (RDID)

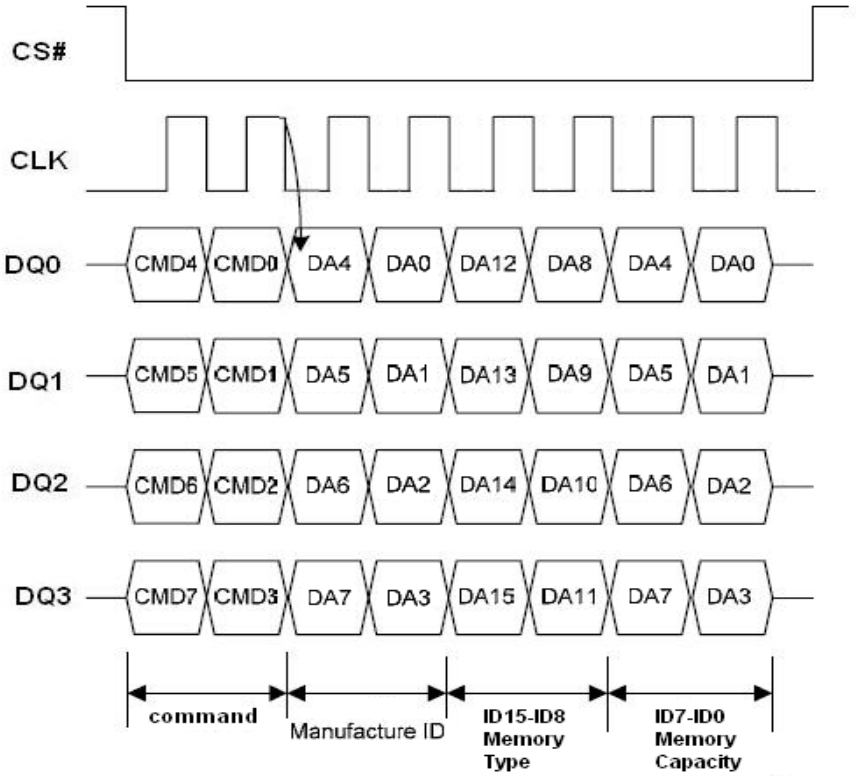


Figure 30.1. Read Identification (RDID) under EQPI Mode

Enter OTP Mode (3Ah)

This Flash has an extra 512 bytes OTP sector, user must issue ENTER OTP MODE command to read, program or erase OTP sector. After entering OTP mode, **SRP bit** becomes OTP_LOCK bit and can be read with RDSR command. Program / Erase command will be disabled when OTP_LOCK bit is '1'

WRSR command will ignore the input data and program OTP_LOCK bit to 1. User must clear the protect bits before enter OTP mode.

OTP sector can only be program and erase before OTP_LOCK bit is set to '1' and BP [3:0] = '0000'. While in OTP mode, array access is not allowed.

User can use WRDI (04h) command to exit OTP mode.

While in OTP mode, user can use Sector Erase (20h) command only to erase OTP data.

The instruction sequence is shown in Figure 31.1 while using the Enable Quad Peripheral Interface mode (EQPI) (38h) command.

Table 8. OTP Sector Address

Sector Size	Address Range
512 byte	xxx000h – xxx1FFh

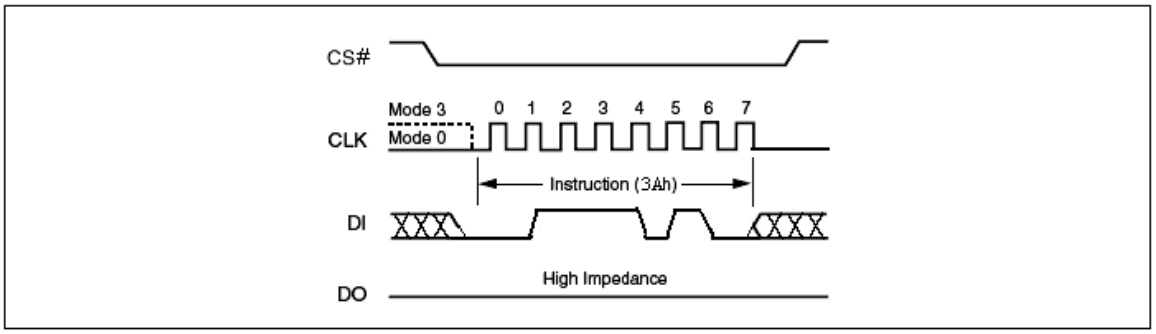


Figure 31. Enter OTP Mode Sequence

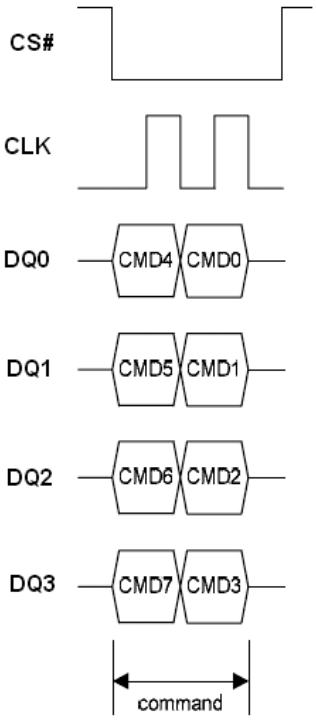


Figure 31.1 Enter OTP Mode Sequence under EQPI Mode

Read SFDP Mode and Unique ID Number (5Ah)

Read SFDP Mode

EN25QH256 features Serial Flash Discoverable Parameters (SFDP) mode. Host system can retrieve the operating characteristics, structure and vendor specified information such as identifying information, memory size, operating voltage and timing information of this device by SFDP mode.
The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read SFDP Mode is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (CLK). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency FR, during the falling edge of Serial Clock (CLK).
The instruction sequence is shown in Figure 32. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Serial Flash Discoverable Parameters (SFDP) instruction. When the highest address is reached, the address counter rolls over to 0x00h, allowing the read sequence to be continued indefinitely. The Serial Flash Discoverable Parameters (SFDP) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output. Any Read Data Bytes at Serial Flash Discoverable Parameters (SFDP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

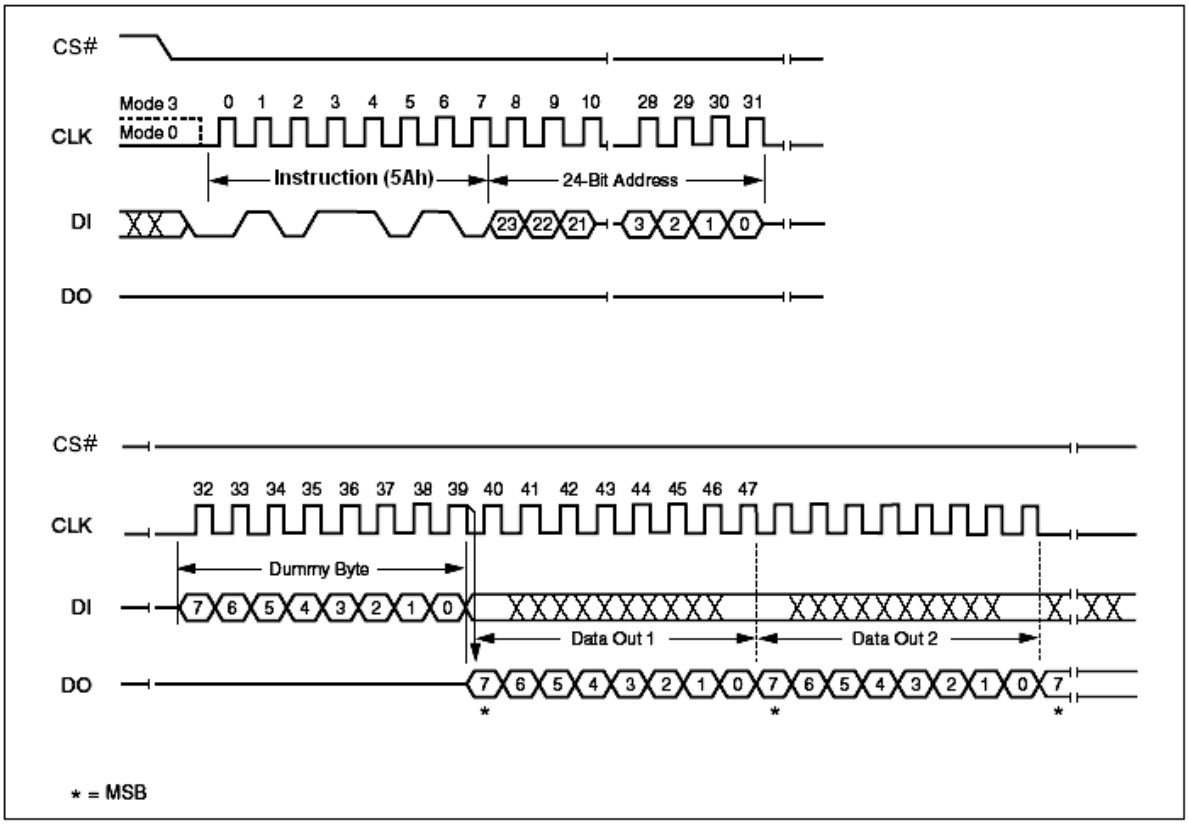


Figure 32. Read SFDP Mode Instruction Sequence Diagram

Note: Please note the above address cycles are base on 3-byte address mode, for 4-byte address mode, the address cycles will be increased.

Table 9. Serial Flash Discoverable Parameters (SFDP) Signature and Parameter Identification Data Value (Advanced Information)

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
SFDP Signature	00h	07 : 00	53h	Signature [31:0]: Hex: 50444653
	01h	15 : 08	46h	
	02h	23 : 16	44h	
	03h	31 : 24	50h	
SFDP Minor Revision Number	04h	07 : 00	00h	Star from 0x00
SFDP Major Revision Number	05h	15 : 08	01h	Star from 0x01
Number of Parameter Headers (NPH)	06h	23 : 16	00h	1 parameter header
Unused	07h	31 : 24	FFh	Reserved
ID Number	08h	07 : 00	00h	JEDEC ID
Parameter Table Minor Revision Number	09h	15 : 08	00h	Star from 0x00
Parameter Table Major Revision Number	0Ah	23 : 16	01h	Star from 0x01
Parameter Table Length (in DW)	0Bh	31 : 24	09h	9 DWORDs
Parameter Table Pointer (PTP)	0Ch	07 : 00	30h	000030h
	0Dh	15 : 08	00h	
	0Eh	23 : 16	00h	
Unused	0Fh	31 : 24	FFh	Reserved

Table 10. Parameter ID (0) (Advanced Information) 1/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Block / Sector Erase sizes Identifies the erase granularity for all Flash Components	30h	00	01b	00 = reserved 01 = 4KB erase 10 = reserved 11 = 64KB erase
		01		
Write Granularity		02	1b	0 = No, 1 = Yes
Write Enable Instruction Required for Writing to Volatile Status Register		03	00b	00 = N/A 01 = use 50h opcode 11 = use 06h opcode
Write Enable Opcode Select for Writing to Volatile Status Register		04		
Unused		05	111b	Reserved
		06		
		07		
4 Kilo-Byte Erase Opcode	31h	08	20h	4 KB Erase Support (FFh = not supported)
		09		
		10		
		11		
		12		
		13		
		14		
		15		
Supports (1-1-2) Fast Read Device supports single input opcode & address and quad output data Fast Read	32h	16	1b	0 = not supported 1 = supported
Address Byte Number of bytes used in addressing for flash arra write and erase.		17	01b	00 = 3-Byte 01 = 3- or 4-Byte (e.g. defaults to 3-Byte mode; enters 4-Byte mode on command) 10 = 4-Byte 11 = reserved
		18		
Supports Double Transfer Rate (DTR) Clocking Indicates the device supports some type of double transfer rate clocking.		19	0b	0 = not supported 1 = supported
Supports (1-2-2) Fast Read Device supports single input opcode, dual input address, and quad output data Fast Read		20	1b	0 = not supported 1 = supported
Supports (1-4-4) Fast Read Device supports single input opcode, quad input address, and quad output data Fast Read		21	1b	0 = not supported 1 = supported
Supports (1-1-4) Fast Read Device supports single input opcode & address and quad output data Fast Read		22	0b	0 = not supported 1 = supported
Unused		23	1b	Reserved
Unused	33h	24	FFh	Reserved
		25		
		26		
		27		
		28		
		29		
		30		
		31		

Table 10. Parameter ID (0) (Advanced Information) 2/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Flash Memory Density	37h : 34h	31 : 00	0FFFFFFFh	256 Mbits

Table 10. Parameter ID (0) (Advanced Information) 3/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
(1-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output	38h	00 01 02 03 04	00100b	4 dummy clocks
Quad Input Address Quad Output (1-4-4) Fast Read Number of Mode Bits		05 06 07	010b	8 mode bits
(1-4-4) Fast Read Opcode Opcode for single input opcode, quad input address, and quad output data Fast Read.	39h	08 09 10 11 12 13 14 15	EBh	
(1-1-4) Fast Read Number of Wait states (dummy clocks) needed before valid output	3Ah	16 17 18 19 20	00000b	Not Supported
(1-1-4) Fast Read Number of Mode Bits		21 22 23	000b	Not Supported
(1-1-4) Fast Read Opcode Opcode for single input opcode & address and quad output data Fast Read.	3Bh	31 : 24	FFh	Not Supported

Table 10. Parameter ID (0) (Advanced Information) 4/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
(1-1-2) Fast Read Number of Wait states (dummy clocks) needed before valid output	3Ch	00 01 02 03 04	01000b	8 dummy clocks
(1-1-2) Fast Read Number of Mode Bits		05 06 07	000b	Not Supported
(1-1-2) Fast Read Opcode Opcode for single input opcode & address and dual output data Fast Read.	3Dh	15 : 08	3Bh	
(1-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output	3Eh	16 17 18 19 20	00100b	4 dummy clocks
(1-2-2) Fast Read Number of Mode Bits		21 22 23	000b	Not Supported
(1-2-2) Fast Read Opcode Opcode for single input opcode, dual input address, and dual output data Fast Read.	3Fh	31 : 24	BBh	

Table 10. Parameter ID (0) (Advanced Information) 5/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Supports (2-2-2) Fast Read Device supports dual input opcode & address and dual output data Fast Read.	40h	00	0b	0 = not supported 1 = supported
Reserved. These bits default to all 1's		01 02 03	111b	Reserved
Supports (4-4-4) Fast Read Device supports Quad input opcode & address and quad output data Fast Read.		04	1b	0 = not supported 1 = supported (EQPI Mode)
Reserved. These bits default to all 1's		05 06 07	111b	Reserved
Reserved. These bits default to all 1's	43h : 41h	31 : 08	FFh	Reserved

Table 10. Parameter ID (0) (Advanced Information) 6/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Reserved. These bits default to all 1's	45h : 44h	15 : 00	FFh	Reserved
(2-2-2) Fast Read Number of Wait states (dummy clocks) needed before valid output	46h	16	00000b	Not Supported
		17		
		18		
		19		
		20		
(2-2-2) Fast Read Number of Mode Bits		21	000b	Not Supported
		22		
		23		
(2-2-2) Fast Read Opcode Opcode for dual input opcode & address and dual output data Fast Read.	47h	31 : 24	FFh	Not Supported

Table 10. Parameter ID (0) (Advanced Information) 7/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Reserved. These bits default to all 1's	49h : 48h	15 : 00	FFh	Reserved
(4-4-4) Fast Read Number of Wait states (dummy clocks) needed before valid output	4Ah	16	00100b	4 dummy clocks
		17		
		18		
		19		
		20		
(4-4-4) Fast Read Number of Mode Bits		21	010b	8 mode bits
		22		
		23		
(4-4-4) Fast Read Opcode Opcode for quad input opcode/address, quad output data Fast Read.	4Bh	31 : 24	EBh	Must Enter EQPI Mode Firstly

Table 10. Parameter ID (0) (Advanced Information) 8/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Sector Type 1 Size	4Ch	07 : 00	0Ch	4 KB
Sector Type 1 Opcode	4Dh	15 : 08	20h	
Sector Type 2 Size	4Eh	23 : 16	00h	Not Supported
Sector Type 2 Opcode	4Fh	31 : 24	FFh	Not Supported

Table 10. Parameter ID (0) (Advanced Information) 9/9

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Sector Type 3 Size	50h	07 : 00	10h	64 KB
Sector Type 3 Opcode	51h	15 : 08	D8h	
Sector Type 4 Size	52h	23 : 16	00h	Not Supported
Sector Type 4 Opcode	53h	31 : 24	FFh	Not Supported

Read Unique ID Number

The Read Unique ID Number instruction accesses a factory-set read-only 96-bit number that is unique to each EN25QH256 device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the CS# pin low and shifting the instruction code "5Ah" followed by a three bytes of addresses, 0x80h, and one byte of dummy clocks. After which, the 96-bit ID is shifted out on the falling edge of CLK as shown in figure 32.

Table 11. Unique ID Number

Description	Address (h) (Byte Mode)	Address (Bit)	Data	Comment
Unique ID Number	80h : 8Bh	95 : 00	By die	

Power-up Timing

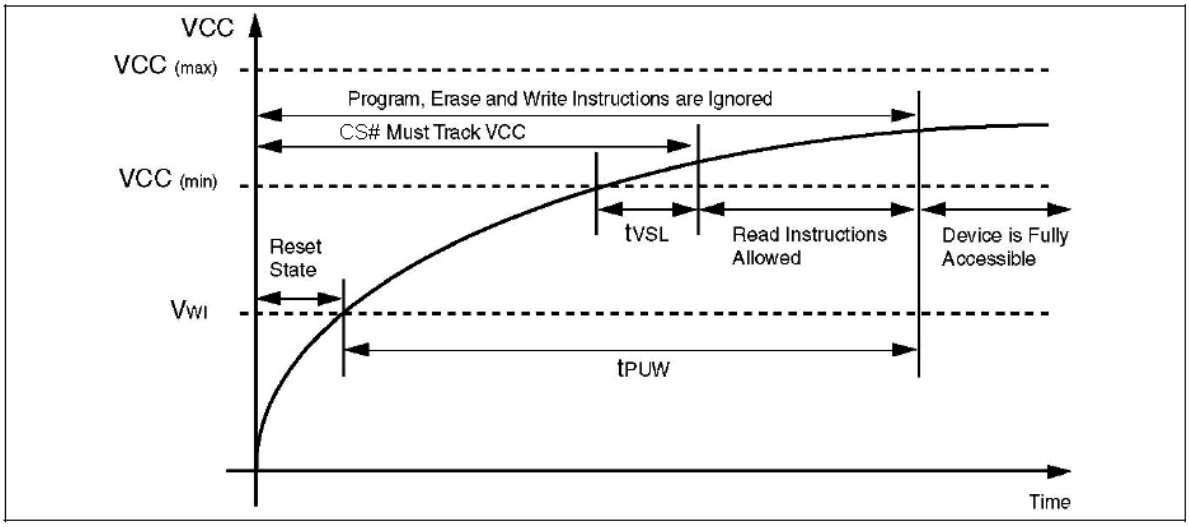


Figure 33. Power-up Timing

Table 12. Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
t_{VSL}(1)	VCC(min) to CS# low	10		µs
t_{PUW}(1)	Time delay to Write instruction	1	10	ms
V_{WI}(1)	Write Inhibit Voltage	1	2.5	V

Note:
1.The parameters are characterized only.
2. VCC (max.) is 3.6V and VCC (min.) is 2.7V

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Table 13. DC Characteristics

(T_a = - 40°C to 85°C; V_{CC} = 2.7-3.6V)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current		-	± 2	µA
I_{LO}	Output Leakage Current		-	± 2	µA
I_{CC1}	Standby Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	20	µA
I_{CC2}	Deep Power-down Current	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	-	20	µA
I_{CC3}	Operating Current (READ)	CLK = 0.1 V_{CC} / 0.9 V_{CC} at 80MHz, DQ = open	-	20	mA
I_{CC4}	Operating Current (PP)	CS# = V_{CC}	-	28	mA
I_{CC5}	Operating Current (WRSR)	CS# = V_{CC}	-	18	mA
I_{CC6}	Operating Current (SE)	CS# = V_{CC}	-	25	mA
I_{CC7}	Operating Current (BE)	CS# = V_{CC}	-	25	mA
V_{IL}	Input Low Voltage		– 0.5	0.2 V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA	-	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA	V_{CC}-0.2	-	V

Table 14. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	20		pF
	Input Rise and Fall Times	5		ns
	Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}		V
	Input Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}		V
	Output Timing Reference Voltages	V_{CC} / 2		V

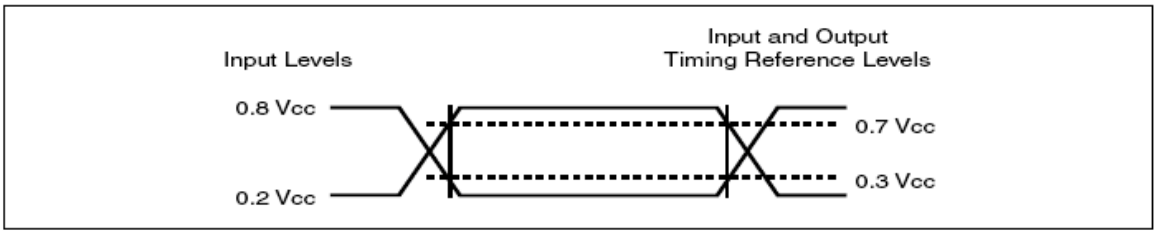


Figure 34. AC Measurement I/O Waveform

Table 15. AC Characteristics

(T_a = - 40°C to 85°C; V_{CC} = 2.7-3.6V)

Symbol	Alt	Parameter		Min	Typ	Max	Unit
F_R	f_C	Serial Clock Frequency for: FAST_READ, PP, SE, BE, DP, RES, WREN, WRDI, WRSR		D.C.	-	80	MHz
		Serial Clock Frequency for: Dual Output Fast Read		D.C.	-	80	MHz
f_R		Serial Clock Frequency for READ, Quad I/O Fast Read, RDSR, RDID,		D.C.	-	50	MHz
t_{CH} [1]		Serial Clock High Time		5	-	-	ns
t_{CL} [1]		Serial Clock Low Time		5	-	-	ns
t_{CLCH} [2]		Serial Clock Rise Time (Slew Rate)		0.1	-	-	V / ns
t_{CHCL} [2]		Serial Clock Fall Time (Slew Rate)		0.1	-	-	V / ns
t_{SLCH}	t_{CSS}	CS# Active Setup Time (Relative to CLK)		5	-	-	ns
t_{CHSH}		CS# Active Hold Time (Relative to CLK)		5	-	-	ns
t_{SHCH}		CS# Not Active Setup Time (Relative to CLK)		5	-	-	ns
t_{CHSL}		CS# Not Active Hold Time (Relative to CLK)		5	-	-	ns
t_{SHSL}	t_{CSH}	CS# High Time for read CS# High Time for program/erase		15 50	-	-	ns ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time		-	-	6	ns
t_{CLQX}	t_{HO}	Output Hold Time		0	-	-	ns
t_{DVCH}	t_{DSU}	Data In Setup Time		2	-	-	ns
t_{CHDX}	t_{DH}	Data In Hold Time		5	-	-	ns
t_{HLCH}		HOLD# Low Setup Time (relative to CLK)		5			ns
t_{HHCH}		HOLD# High Setup Time (relative to CLK)		5			ns
t_{CHHH}		HOLD# Low Hold Time (relative to CLK)		5			ns
t_{CHHL}		HOLD# High Hold Time (relative to CLK)		5			ns
t_{HLQZ} [2]	t_{HZ}	HOLD# Low to High-Z Output				6	ns
t_{HHQX} [2]	t_{LZ}	HOLD# High to Low-Z Output				6	ns
t_{CLQV}	t_V	Output Valid from CLK		-	-	10	ns
t_{WHSL} [3]		Write Protect Setup Time before CS# Low		20	-	-	ns
t_{SHWL} [3]		Write Protect Hold Time after CS# High		100	-	-	ns
t_{DP} [2]		CS# High to Deep Power-down Mode		-	-	3	µs
t_{RES1} [2]		CS# High to Standby Mode without Electronic Signature read		-	-	3	µs
t_{RES2} [2]		CS# High to Standby Mode with Electronic Signature read		-	-	1.8	µs
t_W		Write Status Register Cycle Time		-	10	50	ms
t_{PP}		Page Programming Time		-	0.8	5	ms
t_{SE}		Sector Erase Time		-	50	300	ms
t_{BE}		Block Erase Time		-	0.4	2	s
t_{CE}		Chip Erase Time		-	100	280	s
t_{SR}		Software Reset Latency	WIP = write operation	-	-	28	µs
			WIP = not in write operation	-	-	0	µs

Note: 1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/f_C$
2. Value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write status Register instruction when Status Register Protect Bit is set at 1.

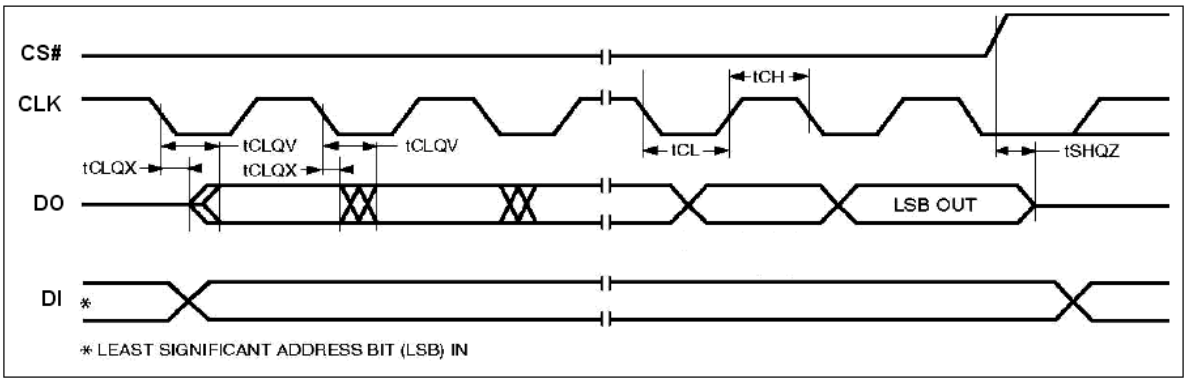


Figure 35. Serial Output Timing

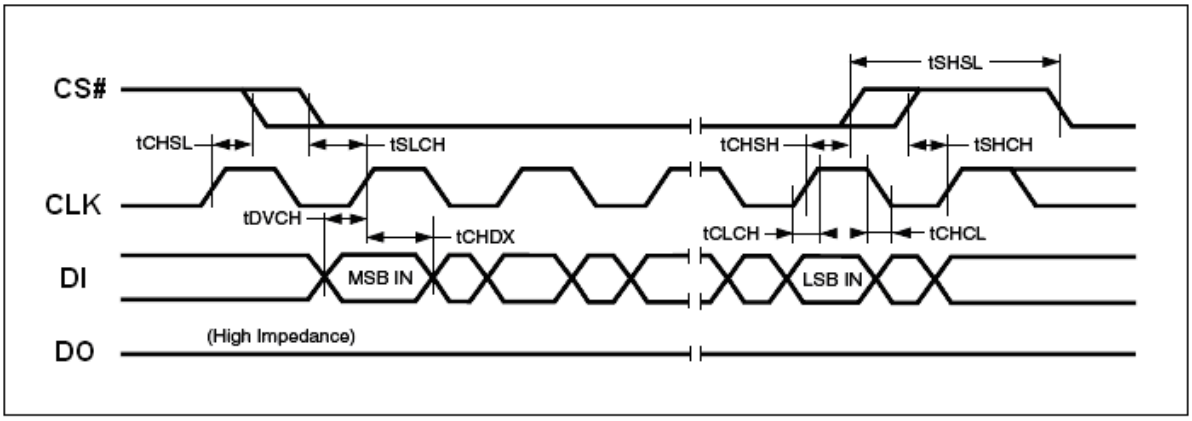


Figure 36. Input Timing

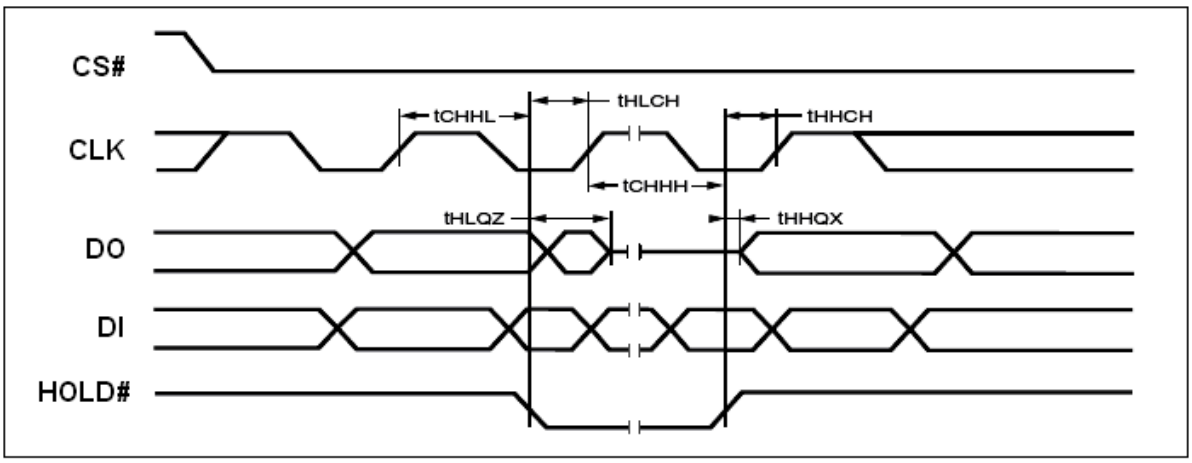


Figure 37. Hold Timing

ABSOLUTE MAXIMUM RATINGS

Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

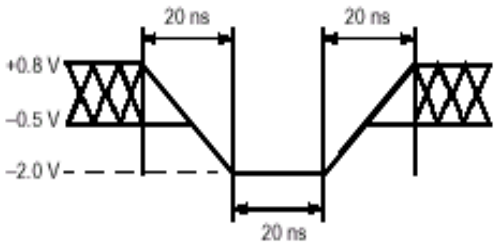
Parameter	Value	Unit
Storage Temperature	-65 to +150	C
Plastic Packages	-65 to +125	C
Output Short Circuit Current[1]	200	mA
Input and Output Voltage (with respect to ground) [2]	-0.5 to +4.0	V
Vcc	-0.5 to +4.0	V

Notes:
1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{ss} to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is V_{cc} + 0.5 V. During voltage transitions, outputs may overshoot to V_{cc} + 1.5 V for periods up to 20ns. See figure below.

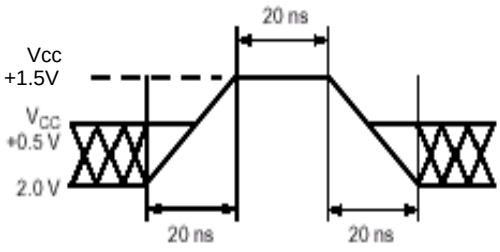
RECOMMENDED OPERATING RANGES [1]

Parameter	Value	Unit
Ambient Operating Temperature Industrial Devices	-40 to 85	C
Operating Supply Voltage Vcc	Full: 2.7 to 3.6	V

Notes:
1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.



Maximum Negative Overshoot Waveform



Maximum Positive Overshoot Waveform

Table 16. DATA RETENTION and ENDURANCE

Parameter Description	Test Conditions	Min	Unit
Data Retention Time	150°C	10	Years
	125°C	20	Years
Erase/Program Endurance	-40 to 85 °C	100k	cycles

Table 17. CAPACITANCE

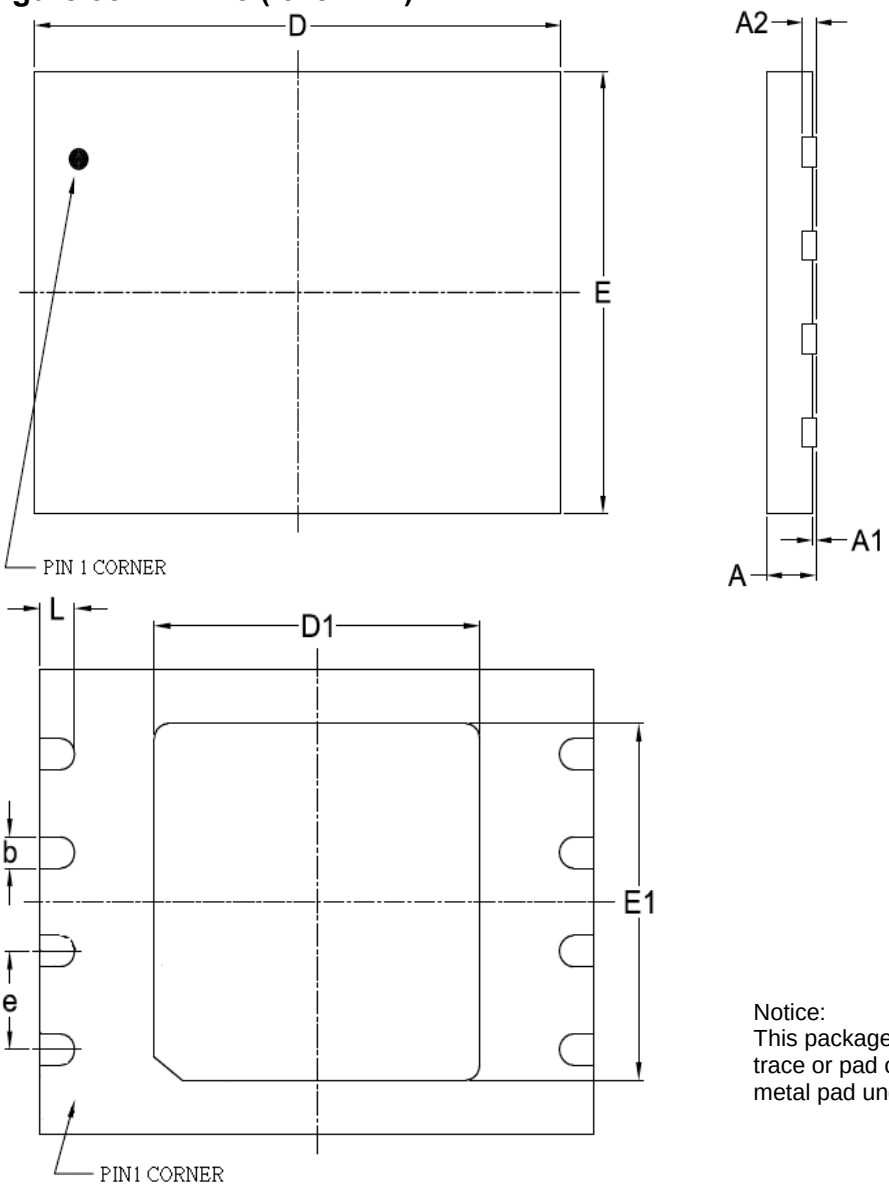
(V_{CC} = 2.7-3.6V)

Parameter Symbol	Parameter Description	Test Setup	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8	pF

Note : Sampled only, not 100% tested, at T_A = 25°C and a frequency of 20MHz.

PACKAGE MECHANICAL

Figure 38. VDFN 8 (6x8 mm)

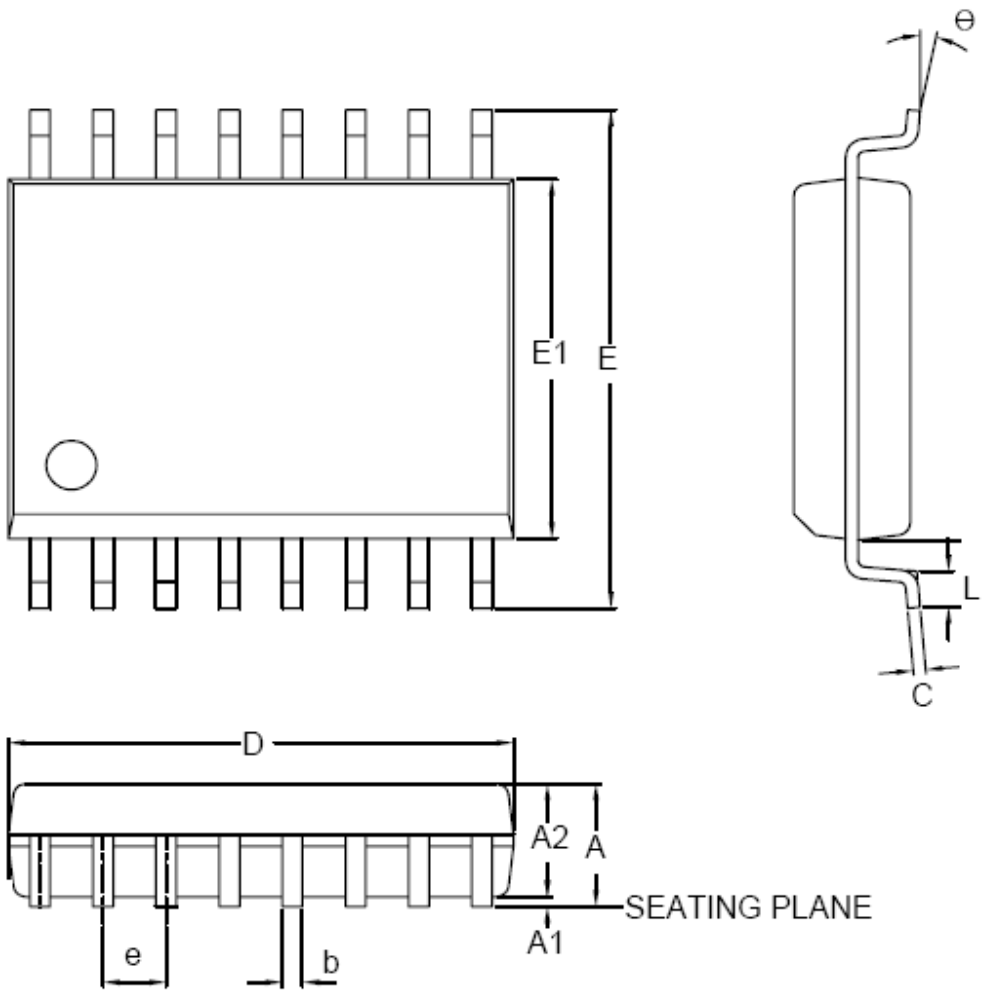


Notice:
This package can't contact to metal trace or pad on board due to expose metal pad underneath the package.

SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	- - -	0.20	- - -
D	7.90	8.00	8.10
E	5.90	6.00	6.10
D1	4.65	4.70	4.75
E1	4.55	4.60	4.65
e	- - -	1.27	- - -
b	0.35	0.40	0.48
L	0.4	0.50	0.60

Note : 1. Coplanarity: 0.1 mm

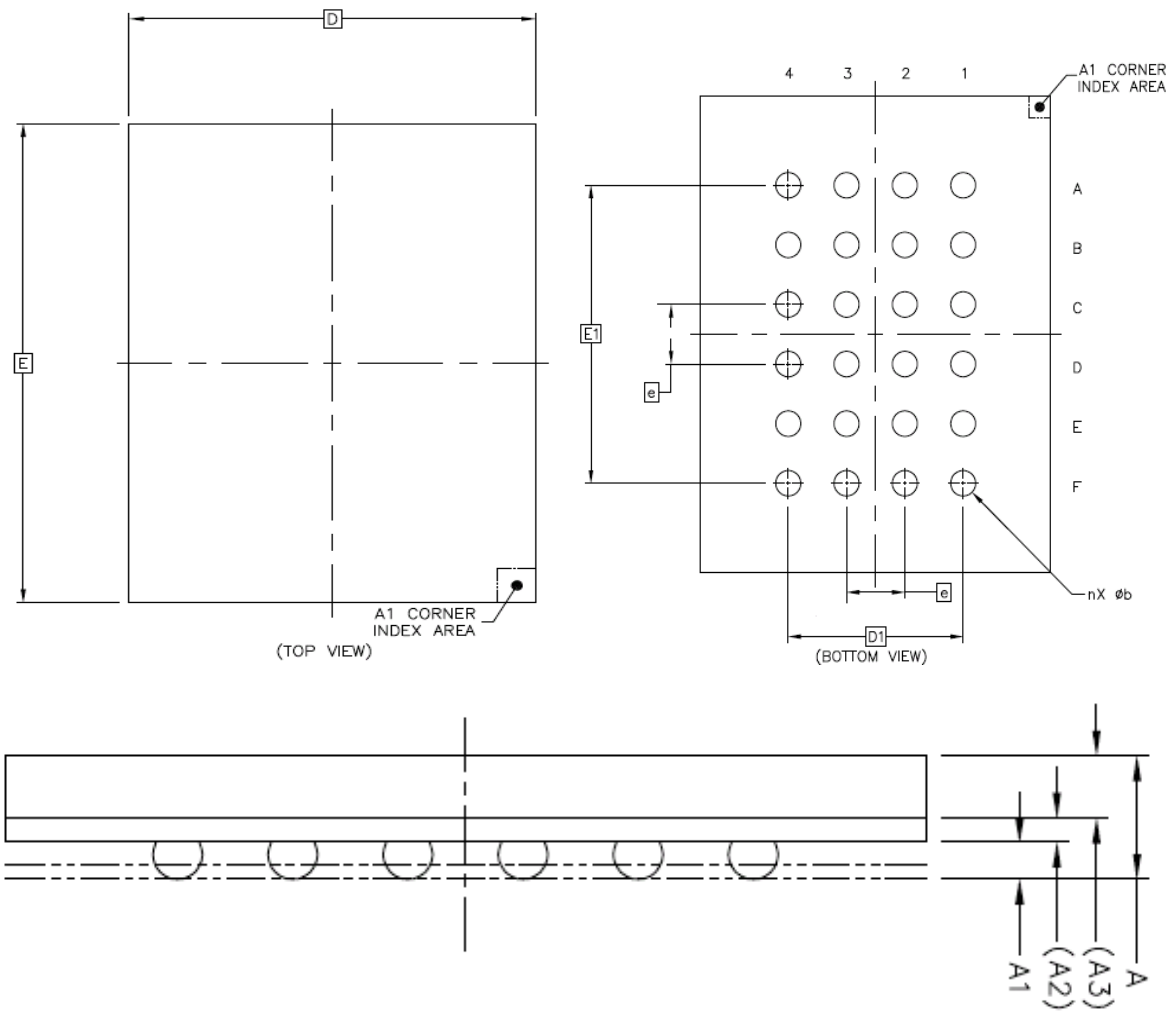
Figure 39. 16 LEAD SOP 300 mil



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	2.65
A1	0.10	0.20	0.30
A2	2.25	- - -	2.40
C	0.20	0.25	0.30
D	10.10	10.30	10.50
E	10.00	- - -	10.65
E1	7.40	7.50	7.60
e	- - -	1.27	- - -
b	0.31	- - -	0.51
L	0.4	- - -	1.27
θ	0^0	5^0	8^0

Note : 1. Coplanarity: 0.1 mm

Figure 40. 24-ball Ball Grid Array (6 x 8 mm) Package



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	---	---	1.20
A1	0.27	---	0.37
A2	0.21 REF		
A3	0.54 REF		
D	6 BSC		
E	8 BSC		
D1	---	3.00	---
E1	---	5.00	---
e	---	1.00	---
b	---	0.40	---

Purpose

Eon Silicon Solution Inc. (hereinafter called “Eon”) is going to provide its products’ top marking on ICs with < cFeon > from January 1st, 2009, and without any change of the part number and the compositions of the Ics. Eon is still keeping the promise of quality for all the products with the same as that of Eon delivered before. Please be advised with the change and appreciate your kindly cooperation and fully support Eon’s product family.

Eon products’ Top Marking

cFeon

cFeon Top Marking Example:

cFeon

Part Number: XXXX-XXX
Lot Number: XXXXX
Date Code: XXXXX

For More Information

Please contact your local sales office for additional information about Eon memory solutions.

ORDERING INFORMATION

EN25QH256 - 80 F I P

PACKAGING CONTENT
P = RoHS compliant

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)

PACKAGE
Y = 8-pin VDFN (6x8mm)
F = 16-pin 300mil SOP
BB = 24-ball Ball Grid Array (6 x 8 mm)

SPEED
80 = 80 MHz

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
25QH = 3V Serial Flash with 4KB Uniform-Sector, Dual and Quad I/O
256 = 256 Megabit (32768K x 8)

Revisions List

Revision No	Description	Date
A	Initial Release	2011/01/10
B	1. Add the note “5. This flow cannot release the device from Deep power down mode.” on page 24. 2. Correct the typo of 6 dummy clocks for EBh command on page 41. 3. Update Read SFDP Mode and add Unique ID Number (5Ah) description on page 57.	2011/06/07
C	1. Update Standard SPI speed from 104MHz to 80MHz. 2. Update Table 16. DC Characteristics on page 63. 3. Update Table 18. AC Characteristics on page 64. 4. Update ORDERING INFORMATION on page 72.	2011/09/01
D	1. Update Figure 2. BLOCK DIAGRAM on page 4. 2. Update the Serial Flash Discoverable Parameters (SFDP) table on page 58, 59, 60, 61 and 62.	2011/11/28
E	Update Unique ID Number from 64 bits to 96 bits on page 63.	2012/01/30
F	1. For the Table 6 Status Register, rename S6 bit from QE to WHDIS and revised its description on page 17, 27 and 28. 2. Update the description for Quad Input/Output FAST_READ (EBh) on page 41. 3. Revise the typo for Table 9. Parameter ID (0) (Advanced Information) 5/9 on page 61.	2012/06/01