# EN29PL032A
## 32 Mbit (2 M x 16-Bit) CMOS 3.0 Volt- only, Simultaneous-Read/Write Flash Memory

## Distinctive Characteristics

### Architectural Advantages

- 32 Mbit Page Mode devices
  - Page size of 4 words: Fast page read access from random locations within the page
- Single power supply operation
  - Voltage range of 2.7V to 3.3V valid for MCP product
  - Single Voltage, 2.7V to 3.6V for Read and Write operations
- Simultaneous Read/Write Operation
  - Data can be continuously read from one bank while executing erase/ program functions in another bank
  - Zero latency switching from write to read operations
- FlexBank Architecture
  - 4 separate banks, with up to two simultaneous operations per device
  - Bank A: 4 Mbit (4 Kw x 8 and 32 Kw x 7)
  - Bank B: 12 Mbit (32 Kw x 24)
  - Bank C: 12 Mbit (32 Kw x 24)
  - Bank D: 4 Mbit (4 Kw x 8 and 32 Kw x 7)
- Secured Silicon Sector region
  - 64 words Secured Silicon Sector region
- Both top and bottom boot blocks in one device
- Cycling Endurance: 100K cycles per sector typical

### Performance Characteristics

- High Performance
  - Page access times as fast as 25 ns
  - Random access times as fast as 70 ns
- Power consumption (typical values at 10 MHz)
  - 45 mA active read current
  - 17 mA program/erase current
  - 0.2 µA typical standby mode current

### Software Features

- Software command-set compatible with JEDEC 42.4 standard
- CFI (Common Flash Interface) compliant
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- Erase Suspend / Erase Resume
  - Suspends an erase operation to allow read or program operations in other sectors of same bank
- Program Suspend / Program Resume
  - Suspends a program operation to allow read operation from sectors other than the one being programmed

### Hardware Features

- Ready/Busy# pin (RY/BY#)
  - Provides a hardware method of detecting program or erase cycle completion
- Hardware reset pin (RESET#)
  - Hardware method to reset the device to reading array data
- WP#/ ACC (Write Protect/Acceleration) input
  - At $V_{IL}$, hardware level protection for the first and last two 4K word sectors.
  - At $V_{IH}$, allows removal of sector protection
  - At $V_{HH}$, provides accelerated programming in a factory setting
- Persistent Sector Protection
  - A command sector protection method to lock combinations of individual sectors and sector groups to prevent program or erase operations within that sector
  - Sectors can be locked and unlocked in-system at $V_{CC}$ level
- Package options
  - 48-pin TSOP-1

## GENERAL DESCRIPTION

The EN29PL032A is a 32 Mega bit, 3.0 volt-only Page Mode and Simultaneous Read/Write Flash memory device organized as 2 Mega words. The devices are offered in the following packages: 48-pin TSOP

The word-wide data (x16) appears on DQ15-DQ0. This device can be programmed in-system or in standard EPROM programmers. An 11.0 volt $V_{PP}$ is not required for write or erase operations.

The device offers fast page access times of 25 ns, with corresponding random access times of 70 ns, respectively, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

# 1. Simultaneous Read/Write Operation with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into 4 banks, which can be considered to be four separate memory arrays as far as certain operations are concerned. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from another bank with zero latency (with two simultaneous operations operating at any one time). This releases the system from waiting for the completion of a program or erase operation, greatly improving system performance.
The device can be organized in both top and bottom sector configurations. The banks are organized as follows:

| Bank | Sectors |
|---|---|
| A | 4 Mbit (4 Kw x 8 and 32 Kw x 7) |
| B | 12 Mbit (32 Kw x 24) |
| C | 12 Mbit (32 Kw x 24) |
| D | 4 Mbit (4 Kw x 8 and 32 Kw x 7) |

## 1.1 Page Mode Features

The page size is 4 words. After initial page access is accomplished, the page mode operation provides fast read access speed of random locations within that page.

## 1.2 Standard Flash Memory Features

The device requires a **single 3.0 volt power supply** (2.7 V to 3.6 V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC 42.4 single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.
Device programming occurs by executing the program command sequence. The Accelerated Program

mode facilitates faster programming times by requiring only two write cycles to program data instead of four. Device erasure occurs by executing the erase command sequence.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

**Hardware data protection** measures include a low $V_{CC}$ detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

**The Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Secured Silicon Sector area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The **Program Suspend/Program Resume** feature enables the user to hold the program operation to read data from any sector that is not selected for programming. If a read is needed from the Secured Silicon Sector area, Persistent Protection area, or the CFI area, after a program suspend, then the user must use the proper command sequence to enter and exit this region.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

## Purpose

Eon Silicon Solution Inc. (hereinafter called “Eon”) is going to provide its products’ top marking on ICs with < cFeon > from January 1st, 2009, and without any change of the part number and the compositions of the ICs. Eon is still keeping the promise of quality for all the products with the same as that of Eon delivered before. Please be advised with the change and appreciate your kindly cooperation and fully support Eon’s product family.

## Eon products’ Top Marking

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**cFeon Top Marking Example:**

| |
|---|
| **cFeon** |
| **Part Number: XXXX-XXX** |
| **Lot Number: XXXXX** |
| **Date Code: XXXXX** |

## For More Information

Please contact your local sales office for additional information about Eon memory solutions.

## 2. Ordering Information

EN29PL032A - 70 T I P

**PACKAGING CONTENT**
P = RoHS compliant

**TEMPERATURE RANGE**
I = Industrial (-40°C to +85°C)

**PACKAGE**
T = 48-pin TSOP

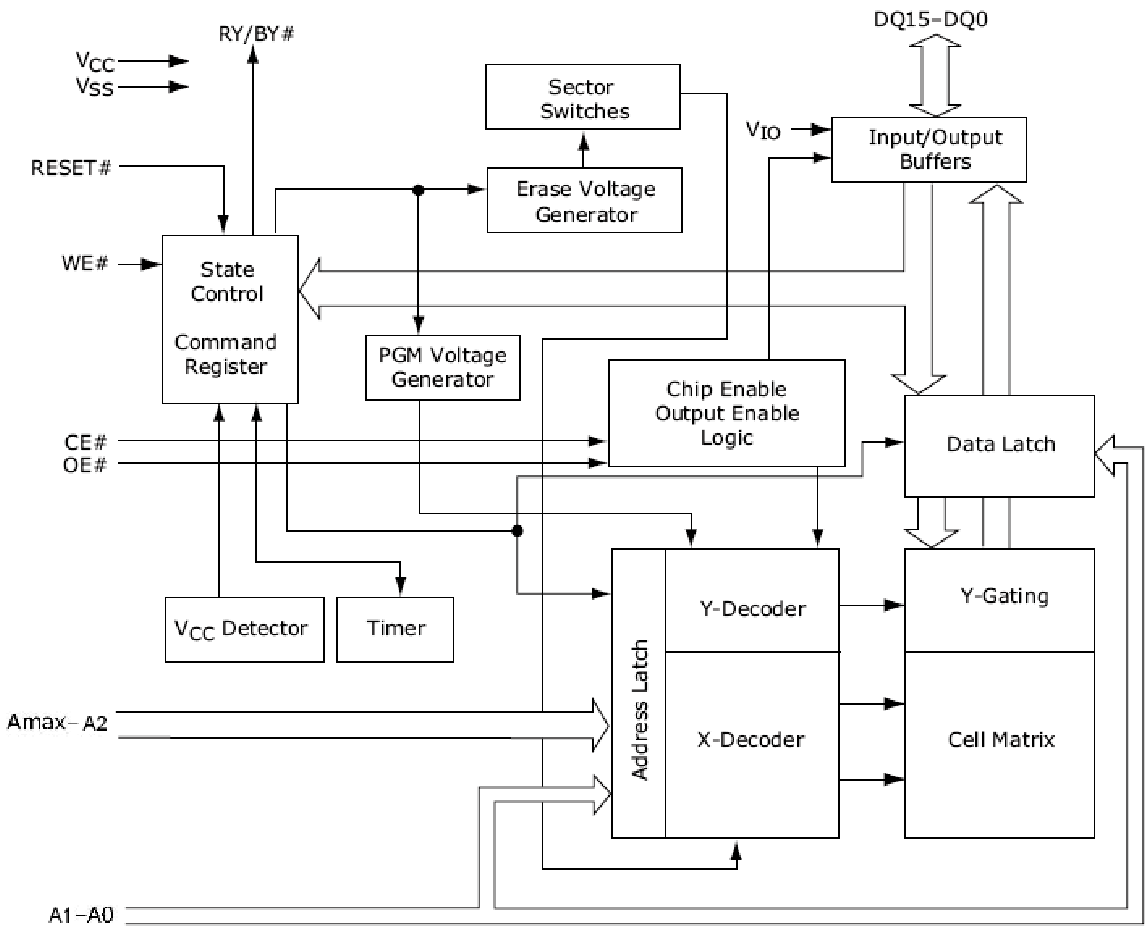
**SPEED**
70 = 70ns

**BASE PART NUMBER**
EN = Eon Silicon Solution Inc.
29PL = FLASH, 3.0V Read Program Erase,
Simultaneous-Read/Write, Page-Mode
032 = 32 Megabit (2 M x 16-Bit)
A = version identifier

## 3. Product Selector Guide

| Part Number | | EN29PL032A |
|---|---|---|
| Speed Option | $V_{CC}$ = 2.7 V – 3.6 V | 70 |
| Max Access Time, ns ($t_{ACC}$) | | 70 |
| Max CE# Access , ns ($t_{CE}$) | | |
| Max Page Access, ns ($t_{PACC}$) | | 25 |
| Max OE# Access, ns ($t_{OE}$) | | |

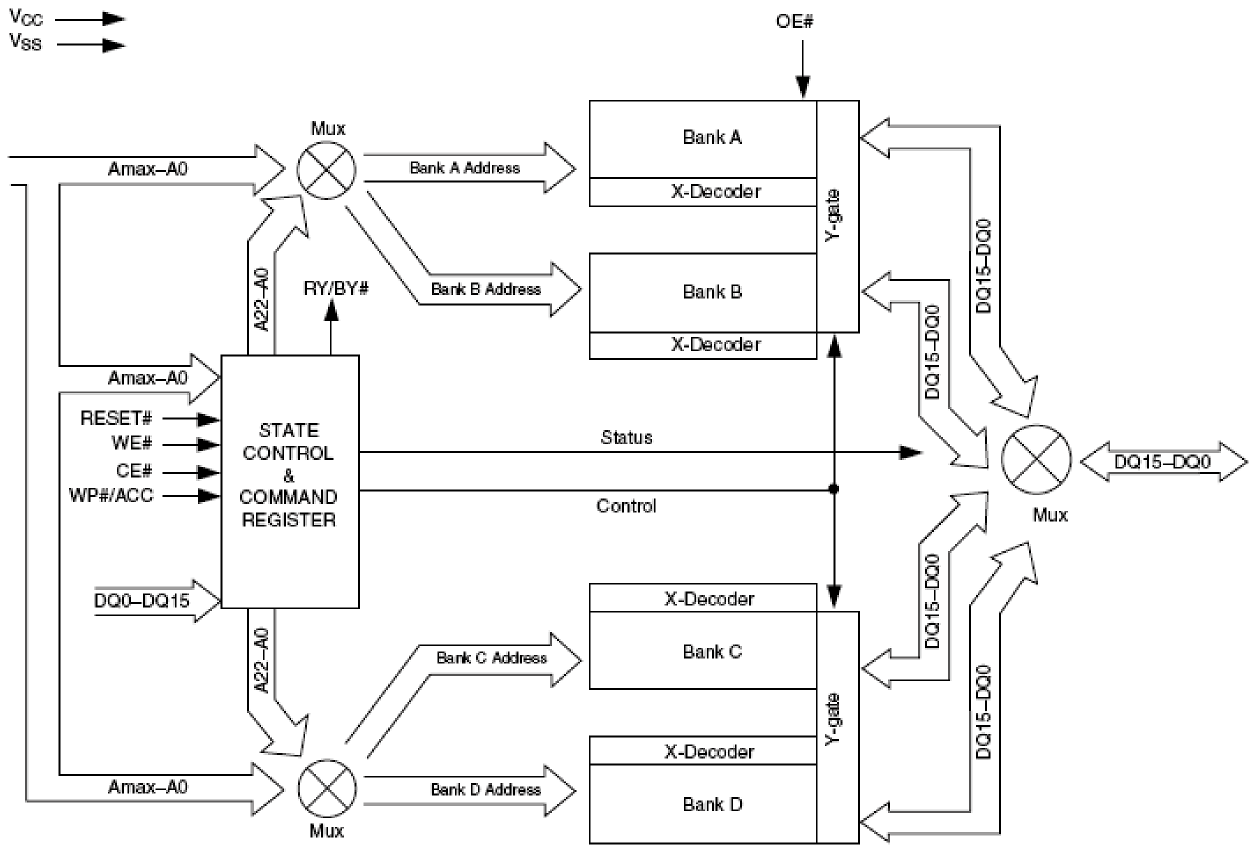
## 4. BLOCK DIAGRAM




**Notes**

1. RY/BY# is an open drain output.
2. Amax = A20

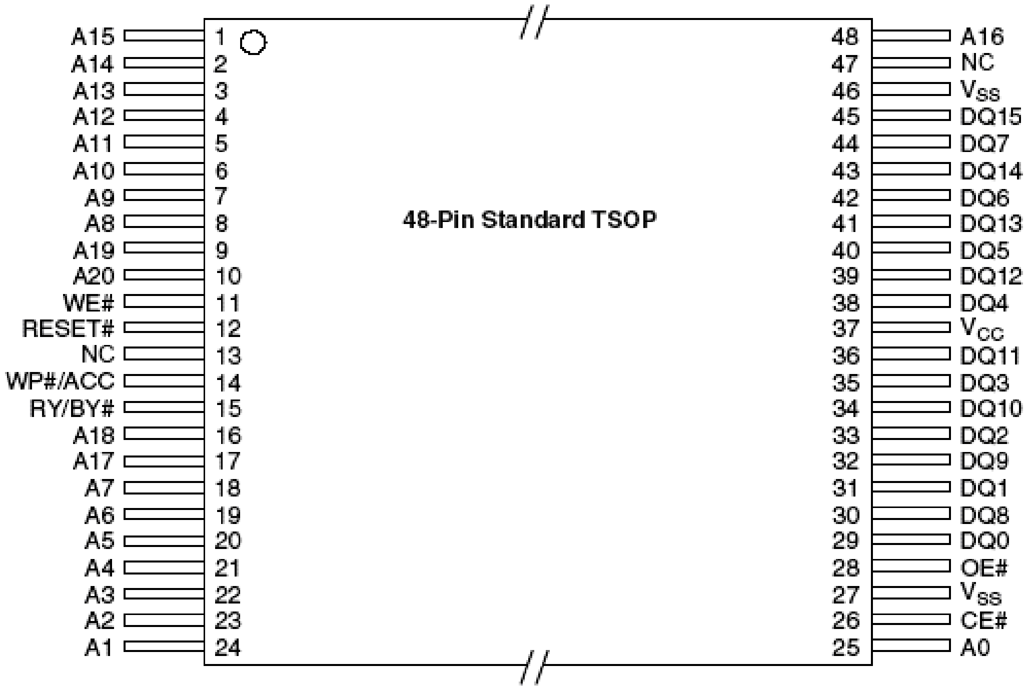
# 5. Simultaneous Read/Write Block Diagram




**Note**
Amax = A20

## 6. Connection Diagrams

**Figure 6.1** 48-pin TSOP

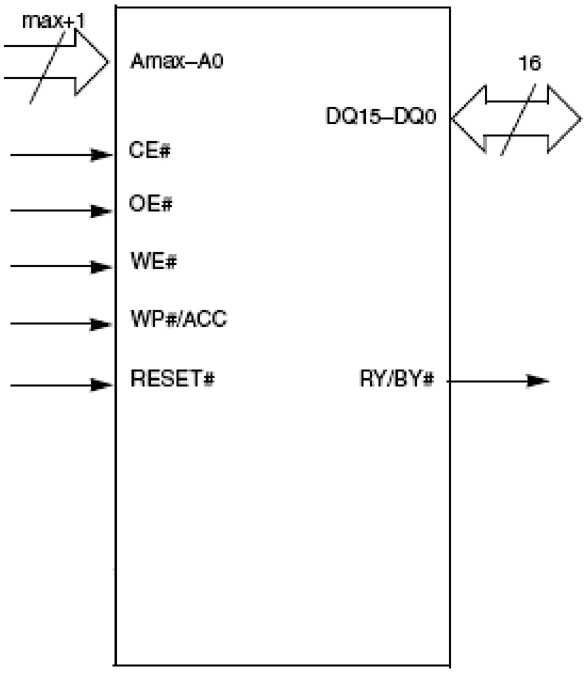



## 7. Pin Description

| | |
|---|---|
| Amax–A0 | Address bus |
| DQ15–DQ0 | 16-bit data inputs/outputs/float |
| CE# | Chip Enable Inputs |
| OE# | Output Enable Input |
| WE# | Write Enable |
| $V_{SS}$ | Device Ground |
| NC | Pin Not Connected Internally |
| RY/BY# | Ready/Busy output and open drain.<br>When RY/BY#= $V_{IH}$, the device is ready to accept read operations and commands. When RY/ BY#= $V_{OL}$, the device is either executing an embedded algorithm or the device is executing a hardware reset operation. |
| WP#/ACC | Write Protect/Acceleration Input.<br>When WP#/ACC= $V_{IL}$, the highest and lowest two 4K-word sectors are write protected regardless of other sector protection configurations. When WP#/ACC= $V_{IH}$, these sector are unprotected unless the PPB is programmed. When WP#/ACC= 9.0V, program and erase operations are accelerated. |
| $V_{CC}$ | Chip Power Supply<br>(2.7 V to 3.6 V) |
| RESET# | Hardware Reset Pin |

**Note**
Amax = A20

## 8. Logic Symbol




**Note:** Amax = A20

## 9. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 9.1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

**Table 9.1** Device Bus Operations

| Operation | CE# | OE# | WE# | RESET# | WP#/ACC | Addresses (Amax–A0) | DQ15–DQ0 |
|---|---|---|---|---|---|---|---|
| Read | L | L | H | H | X | $A_{IN}$ | $D_{OUT}$ |
| Write | L | H | L | H | X (Note 2) | $A_{IN}$ | $D_{IN}$ |
| Standby | Vcc±0.3 V | X | X | Vcc ±0.3 V | X (Note 2) | X | High-Z |
| Output Disable | L | H | H | H | X | X | High-Z |
| Reset | X | X | X | L | X | X | High-Z |
| Temporary Sector Unprotect (High Voltage) | X | X | X | $V_{ID}$ | X | $A_{IN}$ | $D_{IN}$ |

**Legend:**
L = Logic Low = $V_{IL}$, H = Logic High = $V_{IH}$, $V_{ID}$ = $V_{HH}$ = 8.5–9.5 V, X = Don't Care, SA = Sector Address, $A_{IN}$ = Address In, $D_{IN}$ = Data In, $D_{OUT}$ = Data Out

**Notes**
1. The sector protect and sector unprotect functions may also be implemented via programming equipment. See High Voltage Sector Protection
2. WP#/ACC must be high when writing to upper two and lower two sectors.

## 9.1 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the OE# and appropriate CE# pins. CE# is the power control. OE# is the output control and gates array data to the output pins. WE# should remain at $V_{IH}$.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to Table 20.3 for timing specifications and to Figure 20.3 for the timing diagram. $I_{CC1}$ in the DC Characteristics table represents the active current specification for reading array data.

### 9.1.1 Random Read (Non-Page Read)

Address access time ($t_{ACC}$) is equal to the delay from stable addresses to valid output data. The chip enable access time ($t_{CE}$) is the delay from the stable addresses and stable CE# to valid data at the output inputs. The output enable access time is the delay from the falling edge of the OE# to valid data at the output inputs (assuming the addresses have been stable for at least $t_{ACC}–t_{OE}$ time).

### 9.1.2 Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. Address bits Amax–A2 select a 4 word page, and address bits A1–A0 select a specific word within that page. This is an asynchronous operation with the microprocessor supplying the specific word location.

The random or initial page access is $t_{ACC}$ or $t_{CE}$ and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to $t_{PACC}$. When CE# is deasserted (=$V_{IH}$), the reassertion of CE# for subsequent access has access time of $t_{ACC}$ or $t_{CE}$. Here again, CE# selects the device and OE# is the output control and should be used to gate data to the output inputs if the device is selected. Fast page mode accesses are obtained by keeping Amax–A2 constant and changing A1–A0 to select the specific word within that page.

**Table 9.2** Page Select

| Word | A1 | A0 |
|---|---|---|
| Word 0 | 0 | 0 |
| Word 1 | 0 | 1 |
| Word 2 | 1 | 0 |
| Word 3 | 1 | 1 |

## 9.2 Simultaneous Read/Write Operation

In addition to the conventional features (read, program, erase-suspend read, erase-suspend program, and program-suspend read), the device is capable of reading data from one bank of memory while a program or erase operation is in progress in another bank of memory (simultaneous operation). The bank can be selected by bank addresses (A20–A18) with zero latency.

The simultaneous operation can execute multi-function mode in the same bank.

**Table 9.3** Bank Select

| Bank | A20–A18 |
|---|---|
| Bank A | 000 |
| Bank B | 001, 010, 011 |
| Bank C | 100, 101, 110 |
| Bank D | 111 |

## 9.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to $V_{IL}$, and OE# to $V_{IH}$.

The device features an Accelerated Program mode to facilitate faster programming. Once a bank enters the Accelerated Program mode, only two write cycles are required to program a word, instead of four. *Word Program Command Sequence* has details on programming data to the device using both standard and Accelerated Program command sequences.
An erase operation can erase one sector or the entire device. Table 9.4 indicates the set of address space that each sector occupies. A "bank address" is the set of address bits required to uniquely select a bank. Similarly, a "sector address" refers to the address bits required to uniquely select a sector. *Command Definitions* has details on erasing a sector or the entire chip, or suspending / resuming the erase operation.

$I_{CC2}$ in the DC Characteristics table represents the active current specification for the write mode. See the timing specification tables and timing diagrams in section *Reset* for write operations.

### 9.3.1 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts $V_{HH}$ on this pin, the device automatically enters the aforementioned Accelerated Program mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Accelerated Program mode. Removing $V_{HH}$ from the WP#/ACC pin returns the device to normal operation. *Note that $V_{HH}$ must not be asserted on WP#/ACC for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin should be raised to $V_{CC}$ when not in use. That is, the WP#/ACC pin should not be left floating or unconnected; inconsistent behavior of the device may result.*

### 9.3.2 Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to section 9.8 and section 15.3 for more information.

## 9.4 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than $V_{IH}$.) If CE# and RESET# are held at $V_{IH}$, but not within $V_{CC}$ ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time ($t_{CE}$) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

$I_{CC3}$ in *DC Characteristics* represents the CMOS standby current specification.

## 9.5 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for $t_{ACC}$ + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Note that during automatic sleep mode, OE# must be at $V_{IH}$ before the device reduces current to the stated sleep mode specification. $I_{CC5}$ in *DC Characteristics* represents the automatic sleep mode current specification.

## 9.6 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of $t_{RP}$, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS}$±0.3 V, the device draws CMOS standby current ($I_{CC4}$). If RESET# is held at $V_{IL}$ but not within $V_{SS}$±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of $t_{READY}$ (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of $t_{READY}$ (not during Embedded Algorithms). The system can read data $t_{RH}$ after the RESET# pin returns to $V_{IH}$.

Refer to the tables in *AC Characteristic* for RESET# parameters and to Figure 20.5 for the timing diagram.

## 9.7 Output Disable Mode

When the OE# input is at $V_{IH}$, output from the device is disabled. The output pins (except for RY/BY#) are placed in the highest Impedance state

**Table 9.4** Sector Architecture (Sheet 1 of 2)

| Bank | Sector | Sector Address (A20-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank A | SA0 | 000000000 | 4 | 000000h–000FFFh |
| | SA 1 | 000000001 | 4 | 001000h–001FFFh |
| | SA 2 | 000000010 | 4 | 002000h–002FFFh |
| | SA 3 | 000000011 | 4 | 003000h–003FFFh |
| | SA 4 | 000000100 | 4 | 004000h–004FFFh |
| | SA 5 | 000000101 | 4 | 005000h–005FFFh |
| | SA 6 | 000000110 | 4 | 006000h–006FFFh |
| | SA 7 | 000000111 | 4 | 007000h–007FFFh |
| | SA 8 | 000001XXX | 32 | 008000h–00FFFFh |
| | SA 9 | 000010XXX | 32 | 010000h–017FFFh |
| | SA 10 | 000011XXX | 32 | 018000h–01FFFFh |
| | SA 11 | 000100XXX | 32 | 020000h–027FFFh |
| | SA 12 | 000101XXX | 32 | 028000h–02FFFFh |
| | SA 13 | 000110XXX | 32 | 030000h–037FFFh |
| | SA 14 | 000111XXX | 32 | 038000h–03FFFFh |
| Bank B | SA 15 | 001000XXX | 32 | 040000h–047FFFh |
| | SA16 | 001001XXX | 32 | 048000h–04FFFFh |
| | SA 17 | 001010XXX | 32 | 050000h–057FFFh |
| | SA 18 | 001011XXX | 32 | 058000h–05FFFFh |
| | SA 19 | 001100XXX | 32 | 060000h–067FFFh |
| | SA 20 | 001101XXX | 32 | 068000h–06FFFFh |
| | SA 21 | 001110XXX | 32 | 070000h–077FFFh |
| | SA 22 | 001111XXX | 32 | 078000h–07FFFFh |
| | SA 23 | 010000XXX | 32 | 080000h–087FFFh |
| | SA 24 | 010001XXX | 32 | 088000h–08FFFFh |
| | SA25 | 010010XXX | 32 | 090000h–097FFFh |
| | SA 26 | 010011XXX | 32 | 098000h–09FFFFh |
| | SA 27 | 010100XXX | 32 | 0A0000h–0A7FFFh |
| | SA 28 | 010101XXX | 32 | 0A8000h–0AFFFFh |
| | SA 29 | 010110XXX | 32 | 0B0000h–0B7FFFh |
| | SA 30 | 010111XXX | 32 | 0B8000h–0BFFFFh |
| | SA 31 | 011000XXX | 32 | 0C0000h–0C7FFFh |
| | SA 32 | 011001XXX | 32 | 0C8000h–0CFFFFh |
| | SA 33 | 011010XXX | 32 | 0D0000h–0D7FFFh |
| | SA 34 | 011011XXX | 32 | 0D8000h–0DFFFFh |
| | SA 35 | 011100XXX | 32 | 0E0000h–0E7FFFh |
| | SA 36 | 011101XXX | 32 | 0E8000h–0EFFFFh |
| | SA 37 | 011110XXX | 32 | 0F0000h–0F7FFFh |
| | SA 38 | 011111XXX | 32 | 0F8000h–0FFFFFh |

**Table 9.4** Sector Architecture (Sheet 2 of 2)

| Bank | Sector | Sector Address (A20-A12) | Sector Size (Kwords) | Address Range (x16) |
|---|---|---|---|---|
| Bank C | SA39 | 100000XXX | 32 | 100000h–107FFFh |
| | SA40 | 100001XXX | 32 | 108000h–10FFFFh |
| | SA41 | 100010XXX | 32 | 110000h–117FFFh |
| | SA42 | 100011XXX | 32 | 118000h–11FFFFh |
| | SA43 | 100100XXX | 32 | 120000h–127FFFh |
| | SA44 | 100101XXX | 32 | 128000h–12FFFFh |
| | SA45 | 100110XXX | 32 | 130000h–137FFFh |
| | SA46 | 100111XXX | 32 | 138000h–13FFFFh |
| | SA47 | 101000XXX | 32 | 140000h–147FFFh |
| | SA48 | 101001XXX | 32 | 148000h–14FFFFh |
| | SA49 | 101010XXX | 32 | 150000h–157FFFh |
| | SA50 | 101011XXX | 32 | 158000h–15FFFFh |
| | SA51 | 101100XXX | 32 | 160000h–167FFFh |
| | SA52 | 101101XXX | 32 | 168000h–16FFFFh |
| | SA53 | 101110XXX | 32 | 170000h–177FFFh |
| | SA54 | 101111XXX | 32 | 178000h–17FFFFh |
| | SA55 | 110000XXX | 32 | 180000h–187FFFh |
| | SA56 | 110001XXX | 32 | 188000h–18FFFFh |
| | SA57 | 110010XXX | 32 | 190000h–197FFFh |
| | SA58 | 110011XXX | 32 | 198000h–19FFFFh |
| | SA59 | 110100XXX | 32 | 1A0000h–1A7FFFh |
| | SA60 | 110101XXX | 32 | 1A8000h–1AFFFFh |
| | SA61 | 110110XXX | 32 | 1B0000h–1B7FFFh |
| | SA62 | 110111XXX | 32 | 1B8000h–1BFFFFh |
| Bank D | SA63 | 111000XXX | 32 | 1C0000h–1C7FFFh |
| | SA64 | 111001XXX | 32 | 1C8000h–1CFFFFh |
| | SA65 | 111010XXX | 32 | 1D0000h–1D7FFFh |
| | SA66 | 111011XXX | 32 | 1D8000h–1DFFFFh |
| | SA67 | 111100XXX | 32 | 1E0000h–1E7FFFh |
| | SA68 | 111101XXX | 32 | 1E8000h–1EFFFFh |
| | SA69 | 111110XXX | 32 | 1F0000h–1F7FFFh |
| | SA70 | 111111000 | 4 | 1F8000h–1F8FFFh |
| | SA71 | 111111001 | 4 | 1F9000h–1F9FFFh |
| | SA72 | 111111010 | 4 | 1FA000h–1FAFFFh |
| | SA73 | 111111011 | 4 | 1FB000h–1FBFFFh |
| | SA74 | 111111100 | 4 | 1FC000h–1FCFFFh |
| | SA75 | 111111101 | 4 | 1FD000h–1FDFFFh |
| | SA76 | 111111110 | 4 | 1FE000h–1FEFFFh |
| | SA77 | 111111111 | 4 | 1FF000h–1FFFFFh |

**Table 9.5** Secured Silicon Sector Addresses

| | Sector Size | Address Range |
|---|---|---|
| Customer-Lockable Area | 64 words | 000040h-00007Fh |

## 9.8 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires $V_{ID}$ on address pin A9. Address pins must be as shown in Table 9.6. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 9.4). Table 9.6 show the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0. However, the autoselect codes can also be accessed in-system through the command register, for instances when the device is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 15.1. *Note that if a Bank Address (BA) (on address bits A20–A18) is asserted during the third write cycle of the autoselect command, the host system can read autoselect data from that bank and then immediately read array data from the other bank, without exiting the autoselect mode.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 15.1. This method does not require $V_{ID}$. Refer to Section 15.3 *Autoselect Command Sequence* for more information.

**Table 9.6** Autoselect Codes (High Voltage Method)

| Description | | CE# | OE# | WE# | Amax to A12 | A10 | A9 | A8 | A7 | A6 | A5 to A4 | A3 | A2 | A1 | A0 | DQ15 to DQ0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Manufacturer ID: Eon | | L | L | H | BA | X | $V_{ID}$ | H[1] | L | L | X | L | L | L | L | 001Ch |
| | | | | | | | | L | | | | | | | | 007Fh |
| Device ID | Read Cycle 1 | L | | | | | | | | | | L | L | L | H | 227Eh |
| | Read Cycle 2 | L | L | H | BA | X | $V_{ID}$ | X | L | L | L | H | H | H | L | 220Ah |
| | Read Cycle 3 | L | | | | | | | | | | H | H | H | H | 2201h |
| Sector Protection Verification | | L | L | H | SA | X | $V_{ID}$ | X | L | L | L | L | L | H | L | 0001h (protected), 0000h (unprotected) |
| Secured Silicon Indicator Bit (DQ7, DQ6) | | L | L | H | BA (See Note) | X | $V_{ID}$ | X | X | L | X | L | L | H | H | DQ7=1 (Factory locked) DQ6=1 (customer locked) |

L = Logic Low = $V_{IL}$, H = Logic High = $V_{IH}$, BA = Bank Address, SA = Sector Address, X = Don't care.

**Note**

1. A8=H is recommended for Manufacturing ID check. If a manufacturing ID is read with A8=L, the chip will output a configuration code 7Fh.
2. A9 = $V_{ID}$ is for HV A9 Autoselect mode only. A9 must be ≤ Vcc (CMOS logic level) for Command Autoselect Mode.

## 9.9 Selecting a Sector Protection Mode

**Table 9.7** Boot Sector/Sector Block Addresses for Protection/Unprotection

| Sector | A20-A12 | Sector/Sector Block Size |
|---|---|---|
| SA0 | 000000000 | 4 Kwords |
| SA1 | 000000001 | 4 Kwords |
| SA2 | 000000010 | 4 Kwords |
| SA3 | 000000011 | 4 Kwords |
| SA4 | 000000100 | 4 Kwords |
| SA5 | 000000101 | 4 Kwords |
| SA6 | 000000110 | 4 Kwords |
| SA7 | 000000111 | 4 Kwords |
| SA8 | 000001XXX | 32 Kwords |
| SA9 | 000010XXX | 32 Kwords |
| SA10 | 000011XXX | 32 Kwords |
| SA11-SA14 | 0001XXXXX | 128 (4x32) Kwords |
| SA15-SA18 | 0010XXXXX | 128 (4x32) Kwords |
| SA19-SA22 | 0011XXXXX | 128 (4x32) Kwords |
| SA23-SA26 | 0100XXXXX | 128 (4x32) Kwords |
| SA27-SA30 | 0101XXXXX | 128 (4x32) Kwords |
| SA31-SA34 | 0110XXXXX | 128 (4x32) Kwords |
| SA35-SA38 | 0111XXXXX | 128 (4x32) Kwords |
| SA39-SA42 | 1000XXXXX | 128 (4x32) Kwords |
| SA43-SA46 | 1001XXXXX | 128 (4x32) Kwords |
| SA47-SA50 | 1010XXXXX | 128 (4x32) Kwords |
| SA51-SA54 | 1011XXXXX | 128 (4x32) Kwords |
| SA55-SA58 | 1100XXXXX | 128 (4x32) Kwords |
| SA59-SA62 | 1101XXXXX | 128 (4x32) Kwords |
| SA63-SA66 | 1110XXXXX | 128 (4x32) Kwords |
| SA67 | 111100XXX | 32 Kwords |
| SA68 | 111101XXX | 32 Kwords |
| SA69 | 111110XXX | 32 Kwords |
| SA70 | 111111000 | 4 Kwords |
| SA71 | 111111001 | 4 Kwords |
| SA72 | 111111010 | 4 Kwords |
| SA73 | 111111011 | 4 Kwords |
| SA74 | 111111100 | 4 Kwords |
| SA75 | 111111101 | 4 Kwords |
| SA76 | 111111110 | 4 Kwords |
| SA77 | 111111111 | 4 Kwords |

The device is shipped with all sectors unprotected. Optional Eon programming services enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See section 9.8 and section 15.3 for details.

# 10. Sector Protection

The EN29PL032A features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups:

### ■ Persistent Sector Protection

A command sector protection method that replaces the old 11 V controlled protection method.

### ■ WP# Hardware Protection

A write protect pin that can prevent program or erase operations in sectors SA0, SA1, SA76 and SA77.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

### ■ Selecting a Sector Protection Mode

All parts default to operate in the Persistent Sector Protection mode. The device is shipped with all sectors unprotected. Optional Eon's programming services enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See Autoselect Mode for details.

## 10.1 Persistent Sector Protection

The Persistent Sector Protection method replaces the 11 V controlled protection method in previous flash devices. This new method provides the sector protection states:

■ Persistently Locked—The sector is protected and cannot be changed.

To achieve these states, two types of "bits" are used:

■ Persistent Protection Bit

■ Persistent Protection Bit Lock

### 10.1.1 Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to a maximum four sectors (see the sector address tables for specific sector protection groupings). All 4 Kword boot-block sectors have individual sector Persistent Protection Bits (PPBs) for greater flexibility. Each PPB is individually modifiable through the PPB Write Command.

The device erases all PPBs in parallel. If any PPB requires erasure, the device must be instructed to preprogram all of the sector PPBs prior to PPB erasure. Otherwise, a previously erased sector PPBs can potentially be over-erased. The flash device does not have a built-in means of preventing sector PPBs over-erasure.

### 10.1.2 Persistent Protection Bit Lock (PPB Lock)

The Persistent Protection Bit Lock (PPB Lock) is a global volatile bit. When set to "1", the PPBs cannot be changed. When cleared ("0"), the PPBs are changeable. There is only one PPB Lock bit per device. The PPB Lock is cleared after power-up or hardware reset. There is no command sequence to unlock the PPB Lock.

## 10.2 Write Protect (WP#)

The Write Protect feature provides a hardware method of protecting the upper two and lower two sectors without using $V_{ID}$. This function is provided by the WP# pin and overrides the previously discussed *High Voltage Sector Protection* method.

If the system asserts $V_{IL}$ on the WP#/ACC pin, the device disables program and erase functions in the two outermost 4 Kword sectors on both ends of the flash array independent of whether it was previously protected or unprotected.

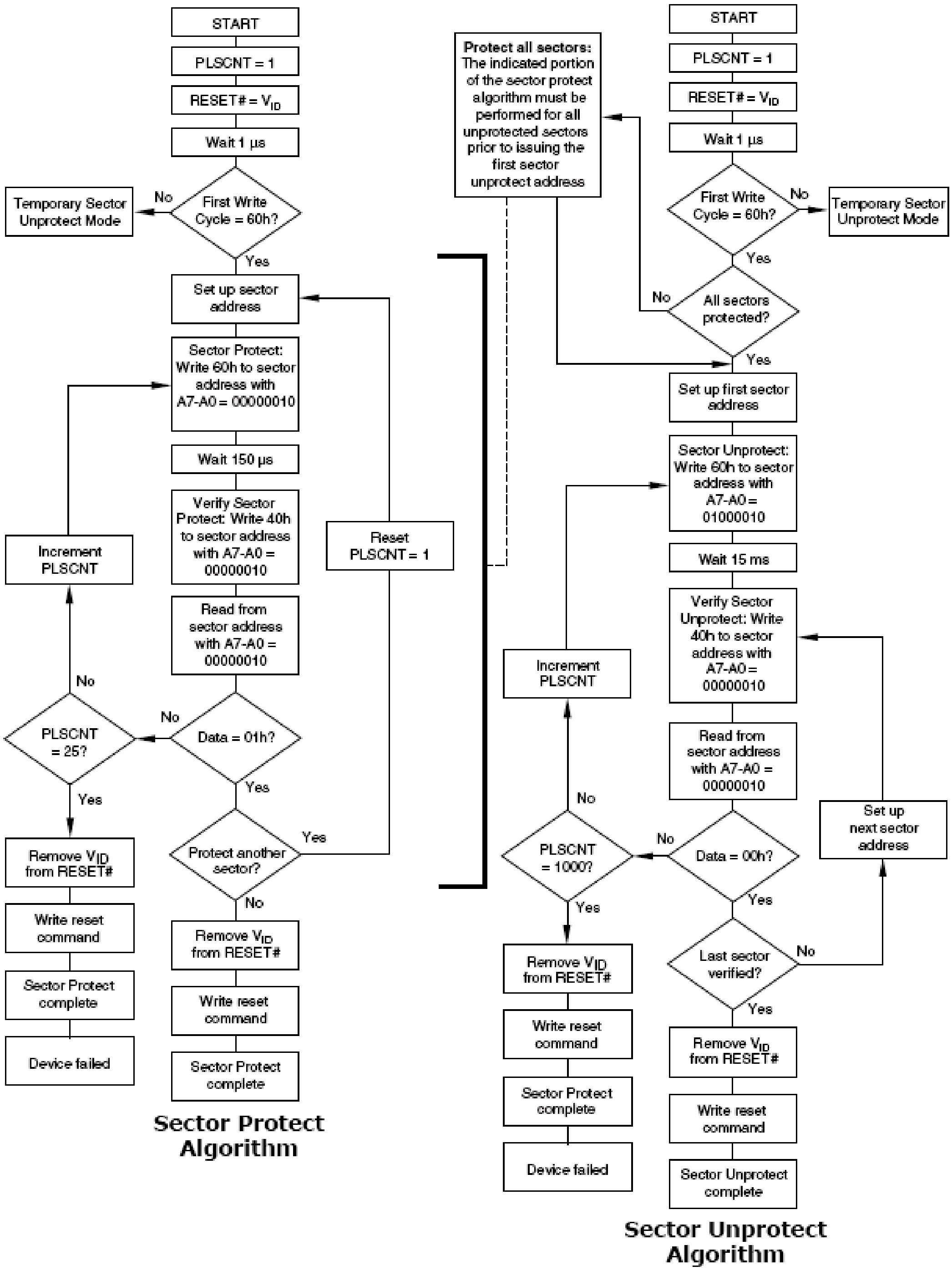
If the system asserts $V_{IH}$ on the WP#/ACC pin, the device reverts the upper two and lower two sectors to whether they were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in the *High Voltage Sector Protection* .

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

## 10.3 High Voltage Sector Protection

Sector protection and unprotection may also be implemented using programming equipment. The procedure requires high voltage ($V_{ID}$) to be placed on the RESET# pin. Refer to Figure 10.1 for details on this procedure. Note that for sector unprotect, all unprotected sectors must first be protected prior to the first sector write cycle.

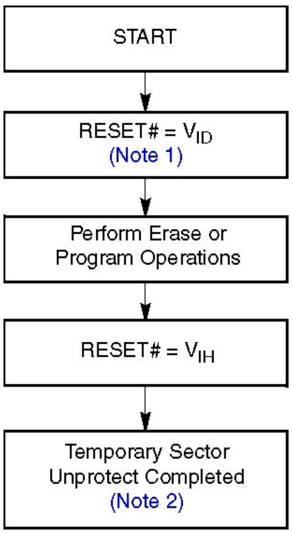
**Figure 10.1** In-System Sector Protection/Sector Unprotection Algorithms



## 11. Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to $V_{ID}$. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once $V_{ID}$ is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 11.1 shows the algorithm, and Figure 21.1 shows the timing diagrams, for this feature. While PPB lock is set, the device cannot enter the Temporary Sector Unprotection Mode.

**Figure 11.1** Temporary Sector Unprotect Operation




**Notes:**

1. All protected sectors unprotected (If WP#/ACC = $V_{IL}$, upper two and lower two sectors will remain protected).
2. All previously protected sectors are protected once again

## 12. Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector provides an extra Flash memory region. The Secured Silicon Sector is 64 words in length and all Secured Silicon read outside of the 64-word address range returns invalid data. The Secured Silicon Sector Indicator Bit, DQ7, (at Autoselect address 03h) is used to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory.

Please note the following general conditions:

- On power-up, or following a hardware reset, the device reverts to sending commands to the normal address space.
- Read outside of sector SA0 return memory array data.
- Sector SA0 is remapped from memory array to Secured Silicon Sector array.
- Once the Secured Silicon Sector Entry Command is issued, the Secured Silicon Sector Exit command must be issued to exit Secured Silicon Sector Mode.
- The Secured Silicon Sector is not accessible when the device is executing an Embedded Program or Embedded Erase algorithm.
- The ACC function is not available when the Secured Silicon Sector is enabled.

## 12.1 Customer- Lockable Secured Silicon Sector (64 words)

The Customer Lockable Secured Silicon Sector is always shipped unprotected (DQ0 set to "0"), allowing customers to utilize that sector in any manner they choose. If the security feature is not required, the Secured Silicon Sector can be treated as an additional Flash memory space.

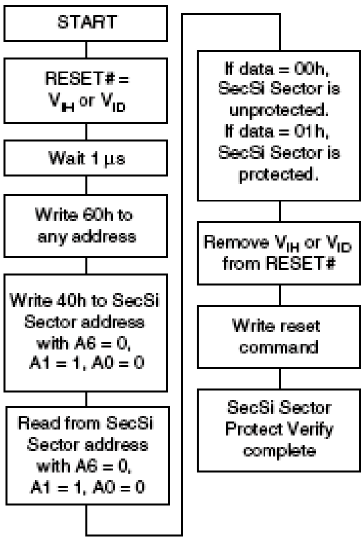
Please note the following:

- Once the Secured Silicon Sector area is protected, the Secured Silicon Sector Indicator Bit (DQ0) is permanently set to "1".
- The Secured Silicon Sector can be read any number of times, but can be programmed and locked only once. The Secured Silicon Sector lock must be used with caution as once locked, there is no procedure available for unlocking the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.
- The accelerated programming (ACC) is not available when the Secured Silicon Sector is enabled.
- Once the Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence which return the device to the memory array at sector 0.

## 12.2 Secured Silicon Sector Protection Bits

The Secured Silicon Sector Protection Bits prevent programming of the Secured Silicon Sector memory area. Once set, the Secured Silicon Sector memory area contents are non-modifiable.

**Figure 12.1 Secured Silicon Sector Protect Verify**



## 13. Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes. In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during $V_{CC}$ power-up and power-down transitions, or from system noise.

### 13.1 Low $V_{cc}$ Write Inhibit

When $V_{CC}$ is less than $V_{LKO}$, the device does not accept any write cycles. This protects data during $V_{CC}$ power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until $V_{CC}$ is greater than $V_{LKO}$. The system must provide the proper signals to the control pins to prevent unintentional writes when $V_{CC}$ is greater than $V_{LKO}$.

### 13.2 Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE#, CE#, or WE# do not initiate a write cycle.

### 13.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = $V_{IL}$, CE# = $V_{IH}$ or WE# = $V_{IH}$. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

### 13.4 Power-Up Write Inhibit

If WE# = CE# = $V_{IL}$ and OE# = $V_{IH}$ during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

## 14. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Table 14.1 to Table 14.4. To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table 14.1 to Table 14.4. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100. Contact your local sales office for copies of these documents.

**Table 14.1** CFI Query Identification String

| Addresses | Data | Description |
|---|---|---|
| 10h<br>11h<br>12h | 0051h<br>0052h<br>0059h | Query Unique ASCII string "QRY" |
| 13h<br>14h | 0002h<br>0000h | Primary OEM Command Set |
| 15h<br>16h | 0040h<br>0000h | Address for Primary Extended Table |
| 17h<br>18h | 0000h<br>0000h | Alternate OEM Command Set (00h = none exists) |
| 19h<br>1Ah | 0000h<br>0000h | Address for Alternate OEM Extended Table (00h = none exists) |

**Table 14.2** System Interface String

| Addresses | Data | Description |
|---|---|---|
| 1Bh | 0027h | $V_{CC}$ Min. (write/erase)<br>D7–D4: volt, D3–D0: 100 millivolt |
| 1Ch | 0036h | $V_{CC}$ Max. (write/erase)<br>D7–D4: volt, D3–D0: 100 millivolt |
| 1Dh | 0000h | $V_{PP}$ Min. voltage (00h = no $V_{PP}$ pin present) |
| 1Eh | 0000h | $V_{PP}$ Max. voltage (00h = no $V_{PP}$ pin present) |
| 1Fh | 0003h | Typical timeout per single byte/word write $2^N$ µs |
| 20h | 0004h | Typical timeout for Min. size buffer write $2^N$ µs (00h = not supported) |
| 21h | 0009h | Typical timeout per individual block erase $2^N$ ms |
| 22h | 0000h | Typical timeout for full chip erase $2^N$ ms (00h = not supported) |
| 23h | 0005h | Max. timeout for byte/word write $2^N$ times typical |
| 24h | 0005h | Max. timeout for buffer write $2^N$ times typical |
| 25h | 0004h | Max. timeout per individual block erase $2^N$ times typical |
| 26h | 0004h | Max. timeout for full chip erase $2^N$ times typical (00h = not supported) |

**Table 14.3** Device Geometry Definition

| Addresses | Data | Description |
|---|---|---|
| 27h | 0016h | Device Size = $2^N$ byte |
| 28h<br>29h | 0001h<br>0000h | Flash Device Interface description (refer to CFI publication 100) |
| 2Ah<br>2Bh | 0006h<br>0000h | Max. number of byte in multi-byte write = $2^N$<br>(00h = not supported) |
| 2Ch | 0003h | Number of Erase Block Regions within device |
| 2Dh<br>2Eh<br>2Fh<br>30h | 0007h<br>0000h<br>0020h<br>0000h | Erase Block Region 1 Information<br>(refer to the CFI specification or CFI publication 100) |
| 31h<br>32h<br>33h<br>34h | 003Dh<br>0000h<br>0000h<br>0001h | Erase Block Region 2 Information<br>(refer to the CFI specification or CFI publication 100) |
| 35h<br>36h<br>37h<br>38h | 0007h<br>0000h<br>0020h<br>0000h | Erase Block Region 3 Information<br>(refer to the CFI specification or CFI publication 100) |
| 39h<br>3Ah<br>3Bh<br>3Ch | 0000h<br>0000h<br>0000h<br>0000h | Erase Block Region 4 Information<br>(refer to the CFI specification or CFI publication 100) |

**Table 14.4** Primary Vendor-Specific Extended Query

| Addresses | Data | Description |
|---|---|---|
| 40h<br>41h<br>42h | 0050h<br>0052h<br>0049h | Query-unique ASCII string "PRI" |
| 43h | 0031h | Major version number, ASCII (reflects modifications to the silicon) |
| 44h | 0034h | Minor version number, ASCII (reflects modifications to the CFI table) |
| 45h | 000Ch | Address Sensitive Unlock (Bits 1-0)<br>00 = Required, 01 = Not Required<br>Silicon technology (Bits 5-2)<br>0001 = 0.18um, 0010 = 0.13um, 0011 = 90nm |
| 46h | 0002h | Erase Suspend<br>0 = Not Supported, 1 = To Read Only, 2 = To Read & Write |
| 47h | 0001h | Sector Protect<br>0 = Not Supported, X = Number of sectors in per group |
| 48h | 0001h | Sector Temporary Unprotect<br>00 = Not Supported, 01 = Supported |
| 49h | 0002h | Sector Protect/Unprotect scheme<br>00h = High Voltage Sector Protection<br>01h = High Voltage + In-System Sector Protection<br>02h = HV + In-System Software Command Sector Protection |
| 4Ah | 003Fh | Simultaneous Operation<br>00 = Not Supported, X = Number of Sectors excluding Bank 1 |
| 4Bh | 0000h | Burst Mode Type<br>00 = Not Supported, 01 = Supported |
| 4Ch | 0001h | Page Mode Type<br>00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page |
| 4Dh | 0085h | ACC (Acceleration) Supply Minimum<br>00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV |
| 4Eh | 0095h | ACC (Acceleration) Supply Maximum<br>00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV |
| 4Fh | 0001h | Top/Bottom Boot Sector Flag<br>00h = Uniform device, 01h = Both top and bottom boot with write protect,<br>02h = Bottom Boot Device, 03h = Top Boot Device,<br>04h = Both Top and Bottom |
| 50h | 0001h | Program Suspend<br>0 = Not supported, 1 = Supported |
| 52h | 0007h | Secured Silicon Sector (Customer OTP Area) Size $2_N$ bytes |
| 53h | 000Fh | Hardware Reset Low Time-out during an embedded algorithm to read mode Maximum $2^N$ ns |
| 54h | 0009h | Hardware Reset Low Time-out not during an embedded algorithm to read<br>mode Maximum $2^N$ ns |
| 55h | 0005h | Erase Suspend Latency Maximum $2^N$ μs |
| 56h | 0005h | Program Suspend Latency Maximum $2^N$ μs |
| 57h | 0004h | Bank Organization<br>00 = Data at 4Ah is zero, X = Number of Banks |
| 58h | 000Fh | Bank 1 Region Information<br>X = Number of Sectors in Bank 1 |
| 59h | 0018h | Bank 2 Region Information<br>X = Number of Sectors in Bank 2 |
| 5Ah | 0018h | Bank 3 Region Information<br>X = Number of Sectors in Bank 3 |
| 5Bh | 000Fh | Bank 4 Region Information<br>X = Number of Sectors in Bank 4 |

## 15. Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table 15.1 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** may place the device in an unknown state. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to *AC Characteristic* for timing diagrams.

### 15.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. The system can read array data using the standard read timing, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See *Erase Suspend/Erase Resume Commands* for more information.

After the device accepts a Program Suspend command, the corresponding bank enters the program-suspend-read mode, after which the system can read data from any non-program-suspended sector within the same bank. See *Program Suspend/Program Resume Commands* for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, *Reset Command*, for more information.

See also *Requirements for Reading Array Data* for more information. The table *AC Characteristic* provides the read parameters, and Figure 16.2 shows the timing diagram.

### 15.2 Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don’t cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend and program-suspend-read mode if that bank was in Program Suspend).

## 15.3 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read any number of autoselect codes without reinitiating the command sequence.

Table 15.1 shows the address and data requirements. To determine sector protection information, the system must write to the appropriate bank address (BA) and sector address (SA).

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

## 15.4 Enter/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing a random, eight word electronic serial number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. The Secured Silicon Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 15.2 shows the address and data requirements for both command sequences. See also *Secured Silicon Sector Flash Memory Region* for further information. *Note that the ACC function mode is not available when the Secured Silicon Sector is enabled.*

## 15.5 Word Program Command Sequence

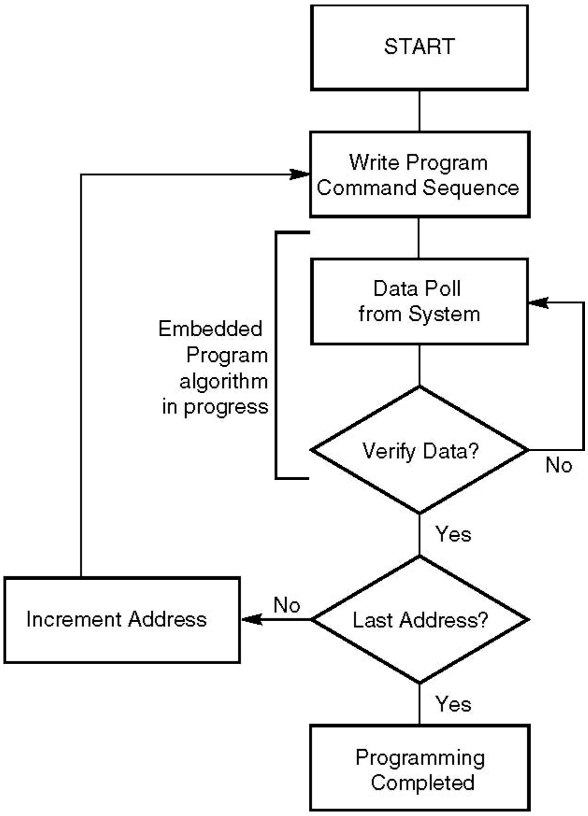
Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 15.1 shows the address and data requirements for the program command sequence. *Note that the Secured Silicon Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to *Write Operation Status* for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity. Note that the Secured Silicon Sector, autoselect and CFI functions are unavailable when the Secured Silicon Sector is enabled.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

**Figure 15.1** Program Operation




**Note**
See Table 15.1 for program command sequence.

## 15.6 Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 15.1 shows the address and data requirements for the chip erase command sequence.

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/ BY#. Refer to *Write Operation Status* for information on these status bits.

Any commands written during the chip erase operation are ignored. *Note that Secured Silicon Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.* However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 15.2 illustrates the algorithm for the erase operation. Refer to the tables in *Erase/Program Operations* for parameters, and Figure 20.8 for timing diagrams.

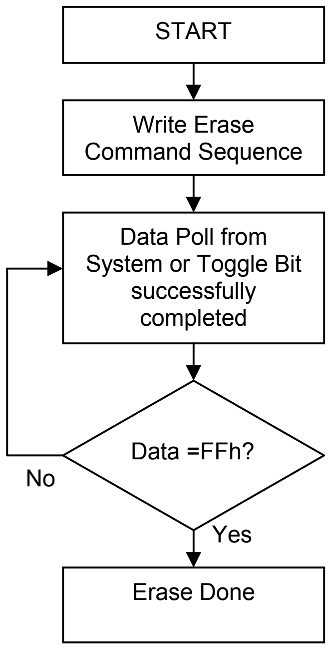
## 15.7 Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the address of the sector to be erased, and the sector erase command. The command Definitions table shows the address and data requirements for the sector erase command sequence.

Once the sector erase operation has begun, only the Sector Erase Suspend command is valid. All other commands are ignored. If there are several sectors to be erased, Sector Erase Command sequences must be issued for each sector. That is, only **a sector address can be specified for each Sector Erase command**. Users must issue another Sector Erase command for the next sector to be erased after the previous one is completed.

When the Embedded Erase algorithm is completed, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. Refer to "Write Operation Status" for information on these status bits. Refer to the Erase/Program Operations tables in the "AC Characteristics" section for parameters, and to the Sector Erase Operations Timing diagram for timing waveforms.

**Figure 15.2** Erase Operation



## 15.8 Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The sector address is required when writing this command. This command is valid only during the sector erase operation. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm. Addresses are don't-cares when writing the Sector Erase Suspend command.

When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 μs to suspend the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device "erase suspends" all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using write operation status bits, just as in the standard Word Program operation.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect for details.

To resume the sector erase operation, the system must write the Erase Resume command (address bits are don't care). The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

## 15.9 Program Suspend/Program Resume Commands

The Program Suspend command allows the system to interrupt an embedded programming operation so that data can read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the programming operation within 15 μs maximum (5 μs typical) and updates the status bits. Addresses are "don't-cares" when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not within a sector in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area, then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in Program Suspend mode. The device allows reading autoselect codes in the suspended sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation. See "Autoselect Command Sequence" for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the write operation status bits, just as in the standard program operation. See "Write Operation Status" for more information. The system must write the Program Resume command (address bits are "don't care") to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume command are ignored. Another Program Suspend command can be written after the device has resumed programming.

## 15.10 Command Definitions Tables

**Table 15.1** Memory Array Command Definitions

| Command Sequence | | Cycles | Bus Cycles (Notes 1- 4) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1st Cycle | | 2nd Cycle | | 3rd Cycle | | 4th Cycle | | 5th Cycle | | 6th Cycle | |
| | | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read (5) | | 1 | RA | RD | | | | | | | | | | |
| Reset (6) | | 1 | XXX | F0 | | | | | | | | | | |
| Autoselect | Manufacturer ID | 4 | 555 | AA | 2AA | 55 | (BA) 555 | 90 | (BA) 000<br>(BA) 100 | 007F<br>001C | | | | |
| | Device ID (10) | 6 | 555 | AA | 2AA | 55 | (BA) 555 | 90 | (BA) X01 | 227E | (BA) X0E | 220A | (BA) X0F | 2201 |
| | Secured Silicon Sector Factory Protect (8) | 4 | 555 | AA | 2AA | 55 | (BA) 555 | 90 | X03 | (8) | | | | |
| | Sector Group Protect Verify (9) | 4 | 555 | AAA | 2AA | 55 | (BA) 555 | 90 | (SA) X02 | XX00<br>XX01 | | | | |
| Program | | 4 | 555 | AA | 2AA | 55 | 555 | A0 | PA | PD | | | | |
| Chip Erase | | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | 555 | 10 |
| Sector Erase | | 6 | 555 | AA | 2AA | 55 | 555 | 80 | 555 | AA | 2AA | 55 | SA | 30 |
| Erase/Program Suspend (11) | | 1 | BA | B0 | | | | | | | | | | |
| Erase/Program Resume (12) | | 1 | BA | 30 | | | | | | | | | | |
| CFI Query (13) | | 1 | 55 | 98 | | | | | | | | | | |
| Accelerated Program | | 2 | XX | A0 | PA | PD | | | | | | | | |

**Legend**
X = Don't care
RA = Address of the memory to be read.
RD = Data read from location RA during read operation.
BA = Address of bank switching to autoselect mode or erase operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first.
SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits Amax–A16 uniquely select any sector.

### Notes

1. See Table 9.1 for description of bus operations.
2. All values are in hexadecimal.
3. Shaded cells in table denote read cycles. All other cycles are write operations.
4. During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.
5. No unlock or command cycles required when bank is reading array data.
6. The Reset command is required to return to reading array (or to erase-suspend-read mode if previously in Erase Suspend) when bank is in autoselect mode, or if DQ5 goes high (while bank is providing status information).
7. Fourth cycle of autoselect command sequence is a read cycle. System must provide bank address to obtain manufacturer ID or device ID information. See Autoselect Command Sequence for more information.
8. The data is DQ6=1 for customer locked.
9. The data is 00h for an unprotected sector group and 01h for a protected sector group.
10. Device ID must be read across cycles 4, 5, and 6. (X01h = 227Eh, X0Eh = 220Ah, X0Fh = 2201h).
11. System may read and program in non-erasing sectors, or enter autoselect mode, when in Program/Erase Suspend mode. Program/ Erase Suspend command is valid only during a sector erase operation, and requires bank address.
12. Program/Erase Resume command is valid only during Erase Suspend mode, and requires bank address.
13. Command is valid when device is ready to read array data or when device is in autoselect mode.
14. WP#/ACC must be at VID during the entire operation of command.

**Table 15.2** Sector Protection Command Definitions

| Command Sequence | Cycles | Bus Cycles (Notes 1-4) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1st Cycle | | 2nd Cycle | | 3rd Cycle | | 4th Cycle | | 5th Cycle | | 6th Cycle | |
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Reset | 1 | XXX | F0 | | | | | | | | | | |
| Secured Silicon Sector Entry (12) | 3 | 555 | AA | 2AA | 55 | 555 | 88 | | | | | | |
| Secured Silicon Sector Exit (12) | 4 | 555 | AA | 2AA | 55 | 555 | 90 | XX | 00 | | | | |
| Secured Silicon Protection Bit Program (Notes 5, 7) | 6 | 555 | AA | 2AA | 55 | 555 | 60 | OW | 68 | OW | 48 | OW | RD (0) |
| Secured Silicon Protection Bit Status | 5 | 555 | AA | 2AA | 55 | 555 | 60 | OW | 48 | OW | RD (0) | | |
| PPB Program (Notes 5, 7, 8) | 6 | 555 | AA | 2AA | 55 | 555 | 60 | (SA) WP | 68 | (SA) WP | 48 | (SA) WP | RD (0) |
| PPB Status | 4 | 555 | AA | 2AA | 55 | (BA) 555 | 90 | (SA) WP | RD (0) | | | | |
| All PPB Erase (Notes 5, 6, 7, 9, 10) | 6 | 555 | AA | 2AA | 55 | 555 | 60 | (BA) WP | 60 | (SA) | 40 | (SA) WP | RD (0) |
| PPB Lock Bit Set | 3 | 555 | AA | 2AA | 55 | 555 | 78 | | | | | | |
| PPB Lock Bit Status (11) | 4 | 555 | AA | 2AA | 55 | (BA) 555 | 58 | SA | RD (1) | | | | |

**Legend**
OW = Address (A7:A0) is (00011010)
PD[3:0] = Password Data (1 of 4 portions)
PPB = Persistent Protection Bit
RD(0) = Read Data DQ0 for protection indicator bit.
RD(1) = Read Data DQ1 for PPB Lock status.
SA = Sector Address where security command applies. Address bits Amax: A12 uniquely select any sector.
SL = Persistent Protection Mode Lock Address (A7:A0) is (00010010)
WP = PPB Address (A7:A0) is (00000010)
X = Don't care

**Notes**
1. See Table 9.1 for description of bus operations.
2. All values are in hexadecimal.
3. Shaded cells in table denote read cycles. All other cycles are write operations.
4. During unlock and command cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.
5. The reset command returns device to reading array.
6. If will retry the All PPB Erase, the reset command must be issued again before the All PPB Erase command.
7. Cycle 4 programs the addressed locking bit. Cycles 5 and 6 validate bit has been fully programmed when DQ0 = 1. If DQ0 = 0 in cycle 6, program command must be issued and verified again.
8. A 2 μs timeout is required between any two portions of password.
9. A 1.2 ms timeout is required between cycles 4 and 5.
10. Cycle 4 erases all PPBs. Cycles 5 and 6 validate bits have been fully erased when DQ0 = 0. If DQ0 = 1 in cycle 6, erase command must be issued and verified again. Before issuing erase command, all PPBs should be programmed to prevent PPB over erasure.
11. DQ1 = 1 if PPB locked, 0 if unlocked.
12. Once the Secured Silicon Sector Entry Command sequence has been entered, the standard array cannot be accessed until the Exit SecSi Sector command has been entered or the device has been reset.

## 16. Write Operation Status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 16.1 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

### 16.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

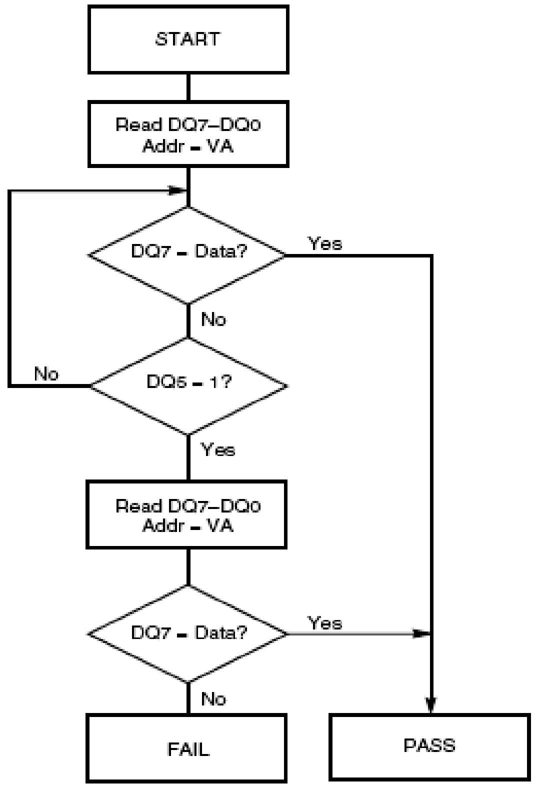
During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 1 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ15–DQ0 on the *following* read cycles. Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ15–DQ0 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ15–DQ0 may be still invalid. Valid data on DQ15–DQ0 will appear on successive read cycles.

Table 16.1 shows the outputs for Data# Polling on DQ7. Figure 16.1 shows the Data# Polling algorithm. Figure 20.10 shows the Data# Polling timing diagram.

**Figure 16.1** Data# Polling Algorithm




***Notes***

1. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
2. DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

## 16.2 RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to $V_{CC}$.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 16.1 shows the outputs for RY/BY#.

## 16.3 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 400 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

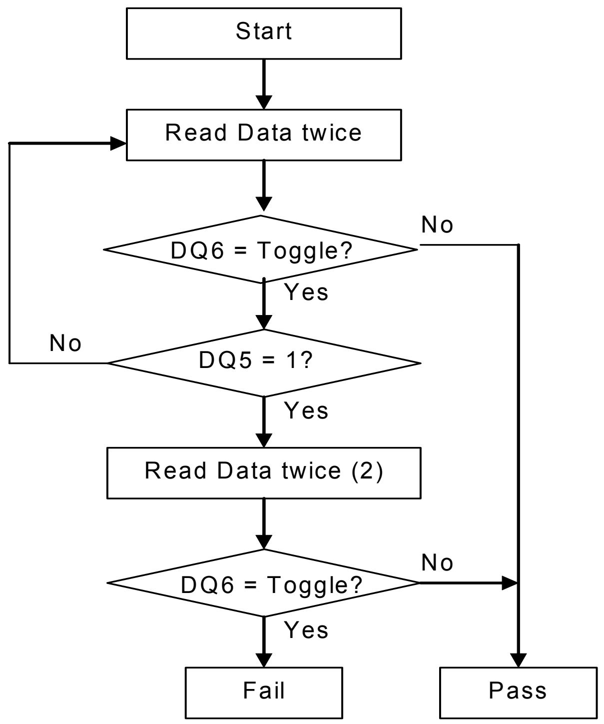
The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the *DQ7: Data# Polling* ).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 16.1 shows the outputs for Toggle Bit I on DQ6. Figure 16.2 shows the toggle bit algorithm. Figure 20.11 shows the toggle bit timing diagrams. Figure 20.12 shows the differences between DQ2 and DQ6 in graphical form. See also the *DQ2: Toggle Bit II*.

**Figure 16.2** Toggle Bit Algorithm




***Note:***
The system should recheck the toggle bit even if DQ5 = “1” because the toggle bit may stop toggling as DQ5 changes to “1.” See the DQ6: Toggle Bit I and DQ2: Toggle Bit II for more information.

## 16.4 DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 16.1 to compare outputs for DQ2 and DQ6.

Figure 16.2 shows the toggle bit algorithm in flowchart form, and the *DQ2: Toggle Bit II* explains the algorithm. See also the *DQ6: Toggle Bit I*. Figure 20.11 shows the toggle bit timing diagram. Figure 20.12 shows the differences between DQ2 and DQ6 in graphical form.

## 16.5 Reading Toggle Bits DQ6/DQ2

Refer to Figure 16.2 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

## 16.6 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

## 16.7 DQ3: Sector Erase Timer

After writing a sector erase command sequence, the output on DQ3 can be checked to determine whether or not an erase operation has begun. (The sector erase timer does not apply to the chip erase command.) When sector erase starts, DQ3 switches from "0" to "1". This device does not support multiple sector erase (continuous sector erase) command sequences so it is not very meaningful since it immediately shows as a "1" after the first 30h command. Future devices may support this feature.

**Table 16.1** Write Operation Status

| Status | | | DQ7 (Note 2) | DQ6 | DQ5 (Note 1) | DQ3 | DQ2 (Note 2) | RY/BY# |
|---|---|---|---|---|---|---|---|---|
| Standard Mode | Embedded Program Algorithm | | DQ7# | Toggle | 0 | N/A | No toggle | 0 |
| | Embedded Erase Algorithm | | 0 | Toggle | 0 | 1 | Toggle | 0 |
| Erase Suspend Mode | Erase Suspend-Read | Erase Suspended Sector | 1 | No toggle | 0 | N/A | Toggle | 1 |
| | | Non-Erase Suspended Sector | Data | Data | Data | Data | Data | 1 |
| | Erase-Suspend -Program | | DQ7# | Toggle | 0 | N/A | N/A | 0 |
| Program Suspend Mode **(Note 3)** | Reading within Program Suspended Sector | | Invalid (Not Allowed) | Invalid (Not Allowed) | Invalid (Not Allowed) | Invalid (Not Allowed) | Invalid (Not Allowed) | 1 |
| | Reading within Non-program Suspended Sector | | Data | Data | Data | Data | Data | 1 |

**Notes:**

1. DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to DQ5: Exceeded Timing Limits for more information.
2. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
3. When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.

## 17. Absolute Maximum Ratings

| Parameter | | Value | Unit |
|---|---|---|---|
| Storage Temperature | | -65 to +150 | ℃ |
| Plastic Packages | | -65 to +125 | ℃ |
| Ambient Temperature With Power Applied | | -55 to +125 | ℃ |
| Output Short Circuit Current[1] | | 200 | mA |
| Voltage with Respect to Ground | A9, RESET# and WP#/ACC[2] | -0.5 to +9.5 | V |
| | All other pins [3] | -0.5 to Vcc+0.5 | V |
| | Vcc | -0.5 to + 4.0 | V |

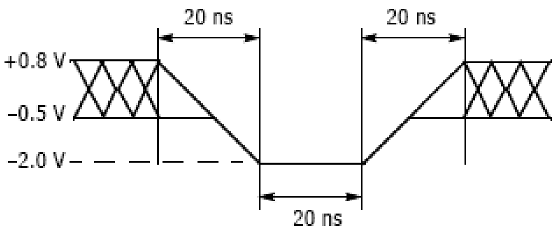
Notes:

1. No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.
2. Minimum DC input voltage on A9, OE#, RESET# and WP#/ACC pins is –0.5V. During voltage transitions, A9, OE#, RESET# and WP#/ACC pins may undershoot $V_{ss}$ to –1.0V for periods of up to 50ns and to –2.0V for periods of up to 20ns. See figure below. Maximum DC input voltage on A9, OE#, and RESET# is 8.5V which may overshoot to 9.5V for periods up to 20ns.
3. Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot $V_{ss}$ to –1.0V for periods of up to 50ns and to –2.0 V for periods of up to 20ns. See figure below. Maximum DC voltage on output and I/O pins is $V_{cc}$ + 0.5 V. During voltage transitions, outputs may overshoot to $V_{cc}$ + 1.5 V for periods up to 20ns. See figure below.
4. Stresses above the values so mentioned above may cause permanent damage to the device. These values are for a stress rating only and do not imply that the device should be operated at conditions up to or above these values. Exposure of the device to the maximum rating values for extended periods of time may adversely affect the device reliability.

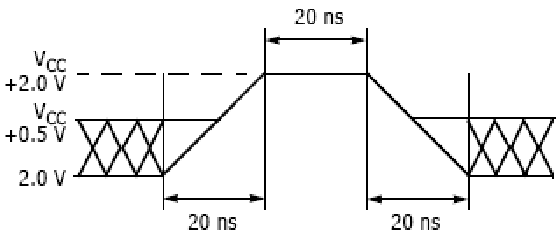
## 18. RECOMMENDED OPERATING RANGES[1]

| Parameter | Value | Unit |
|---|---|---|
| Ambient Operating Temperature<br>Industrial Devices<br>Wireless Devices (For MCP product) | -40 to 85<br>-25 to 85 | ℃ |
| Operating Supply Voltage<br>Vcc | Full Voltage Range:<br>2.7 to 3.6V | V |

1. Recommended Operating Ranges define those limits between which the functionality of the device is guaranteed.




Maximum Negative Overshoot Waveform




Maximum Positive Overshoot Waveform

# 19. DC Characteristics

**Table 19.1** CMOS Compatible

| Parameter | Parameter Description (notes) | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Load Current | $V_{IN} = V_{SS}$ to $V_{CC}$, $V_{CC} = V_{CC}$ max | | | | ±1.0 | µA |
| $I_{LIT}$ | A9, OE#, RESET# Input Load Current | $V_{CC} = V_{CC}$ max; $V_{ID}$= 9.5 V | | | | 35 | µA |
| $I_{LR}$ | Reset Leakage Current | $V_{CC} = V_{CC}$ max; $V_{ID}$= 9.5 V | | | | 35 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{OUT} = V_{SS}$ to $V_{CC}$, OE# = $V_{IH}$ $V_{CC} = V_{CC}$ max | | | | ±1.0 | µA |
| $I_{CC1}$ | $V_{CC}$ Active Read Current (1, 2) | OE# = $V_{IH}$, $V_{CC} = V_{CC}$ max | 5 MHz | | 10 | 30 | mA |
| | | | 10 MHz | | 20 | 55 | |
| $I_{CC2}$ | $V_{CC}$ Active Write Current (2, 3) | OE# = $V_{IH}$, WE# = $V_{IL}$ | | | 15 | 30 | mA |
| $I_{CC3}$ | $V_{CC}$ Standby Current (2) | CE#, RESET#, WP#/ACC = $V_{IO}$ ± 0.3 V | | | 0.2 | 10 | µA |
| $I_{CC4}$ | $V_{CC}$ Reset Current (2) | RESET# = $V_{SS}$ ± 0.3 V | | | 0.2 | 10 | µA |
| $I_{CC5}$ | Automatic Sleep Mode (Notes 2, 4) | $V_{IH} = V_{IO}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V | | | 0.2 | 10 | µA |
| $I_{CC6}$ | $V_{CC}$ Active Read-While-Program Current (1, 2) | OE# = $V_{IH}$, | 5 MHz | | 21 | 45 | mA |
| | | | 10 MHz | | 46 | 70 | |
| $I_{CC7}$ | $V_{CC}$ Active Read-While-Erase Current (1, 2) | OE# = $V_{IH}$, | 5 MHz | | 21 | 45 | mA |
| | | | 10 MHz | | 46 | 70 | |
| $I_{CC8}$ | $V_{CC}$ Active Program-While-Erase-Suspended Current (2, 5) | OE# = $V_{IH}$ | | | 17 | 25 | mA |
| $I_{CC9}$ | $V_{CC}$ Active Page Read Current (2) | OE# = $V_{IH}$, 4 word Page Read | | | 10 | 15 | mA |
| $V_{IL}$ | Input Low Voltage | $V_{IO}$ = 2.7–3.6 V | | –0.5 | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | $V_{IO}$ = 2.7–3.6 V | | 2 | | $V_{CC}$+0.3 | V |
| $V_{HH}$ | Voltage for ACC Program Acceleration | $V_{CC}$ = 3.0 V ± 10% | | 8.5 | | 9.5 | V |
| $V_{ID}$ | Voltage for Autoselect and Temporary Sector Unprotect | $V_{CC}$ = 3.0 V ± 10% | | 8.5 | | 9.5 | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 2.0 mA, $V_{CC} = V_{CC}$ min, $V_{IO}$ = 2.7–3.6 V | | | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = –100 µA, $V_{IO} = V_{CC}$ min | | $V_{CC}$-0.2V | | | V |
| $V_{LKO}$ | Low $V_{CC}$ Lock-Out Voltage (5) | | | 2.3 | | 2.5 | V |

## Notes

1. The $I_{CC}$ current listed is typically less than 5 mA/MHz, with OE# at $V_{IH}$.
2. Maximum $I_{CC}$ specifications are tested with $V_{CC} = V_{CC}$max.
3. $I_{CC}$ active while Embedded Erase or Embedded Program is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for $t_{ACC}$ + 30 ns. Typical sleep mode current is 2 µA.
5. Not 100% tested.

# 20. AC Characteristic

## 20.1 Test Conditions

**Figure 20.1** Test Setups

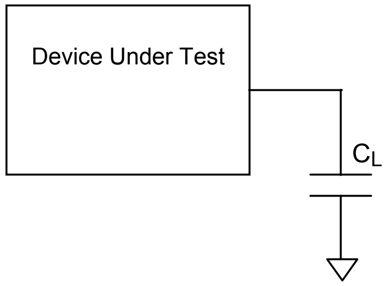



**Table 20.1** Test Specifications

| Test Conditions | All Speeds | Unit |
|---|---|---|
| Output Load Capacitance, $C_L$ (including jig capacitance) | 30 | pF |
| Input Rise and Fall Times | 5 | ns |
| Input Pulse Levels | 0.0-3.0 | V |
| Input timing measurement reference levels | $V_{cc}/2$ | V |
| Output timing measurement reference levels | $V_{cc}/2$ | V |

## 20.2 Switching Waveforms

**Table 20.2** Key To Switching Waveforms

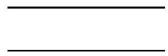
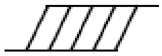
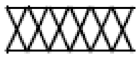
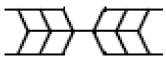
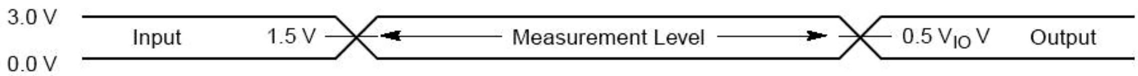
| Waveform | Inputs | Outputs |
|---|---|---|
|  | Steady | |
|  | Changing from H to L | |
|  | Changing from L to H | |
|  | Don't Care, Any Change Permitted | Changing, State Unknown |
|  | Does Not Apply | Center Line is High Impedance State (High Z) |

**Figure 20.2** Input Waveforms and Measurement Levels




## 20.3 VCC Ramp Rate

All DC characteristics are specified for a $V_{CC}$ ramp rate > 1V/100 μs. If the $V_{CC}$ ramp rate is < 1V/100 μs, a hardware reset required.

## 20.4 Read Operations

**Table 20.3** Read-Only Operations

| Parameter | | Description (Notes) | Test Setup | | Speed Options | Unit |
|---|---|---|---|---|---|---|
| JEDEC | Std. | | | | 70 | |
| $t_{AVAV}$ | $t_{RC}$ | Read Cycle Time (1) | | Min | 70 | ns |
| $t_{AVQV}$ | $t_{ACC}$ | Address to Output Delay | CE#, OE# = $V_{IL}$ | Max | 70 | ns |
| $t_{ELQV}$ | $t_{CE}$ | Chip Enable to Output Delay | OE# = $V_{IL}$ | Max | 70 | ns |
| | $t_{PACC}$ | Page Access Time | | Max | 25 | ns |
| $t_{GLQV}$ | $t_{OE}$ | Output Enable to Output Delay | | Max | 25 | ns |
| $t_{EHQZ}$ | $t_{DF}$ | Chip Enable to Output High Z (3) | | Max | 16 | ns |
| $t_{GHQZ}$ | $t_{DF}$ | Output Enable to Output High Z (1, 3) | | Max | 16 | ns |
| $t_{AXQX}$ | $t_{OH}$ | Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First (3) | | Min | 5 | ns |
| | $t_{OEH}$ | Output Enable Hold Time (1) | Read | Min | 0 | ns |
| | | | Toggle and Data# Polling | Min | 10 | ns |

**Notes**

1. Not 100% tested.
2. See Figure 20.1 and Table 20.1 for test specifications
3. Measurements performed by placing a 50 ohm termination on the data pin with a bias of VCC /2. The time from OE# high to the data bus driven to VCC /2 is taken as tDF.

**Figure 20.3** Read Operation Timings

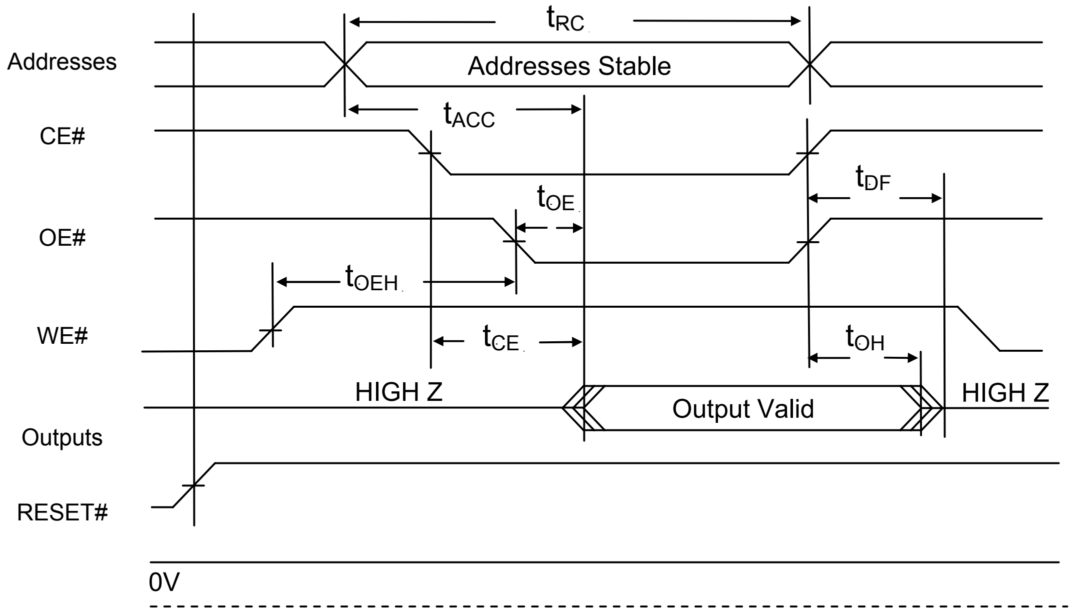
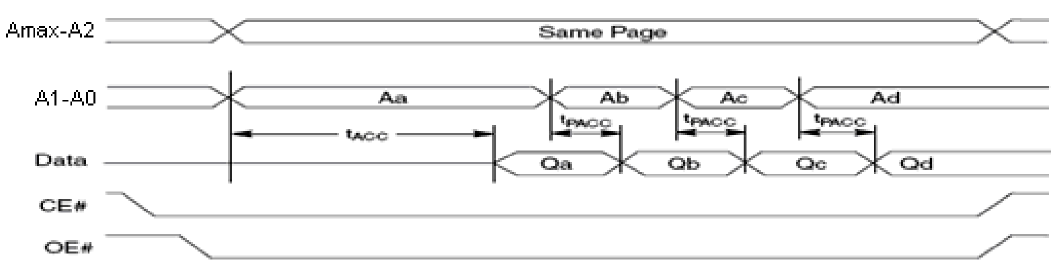



**Figure 20.4** Page Read Operation Timings



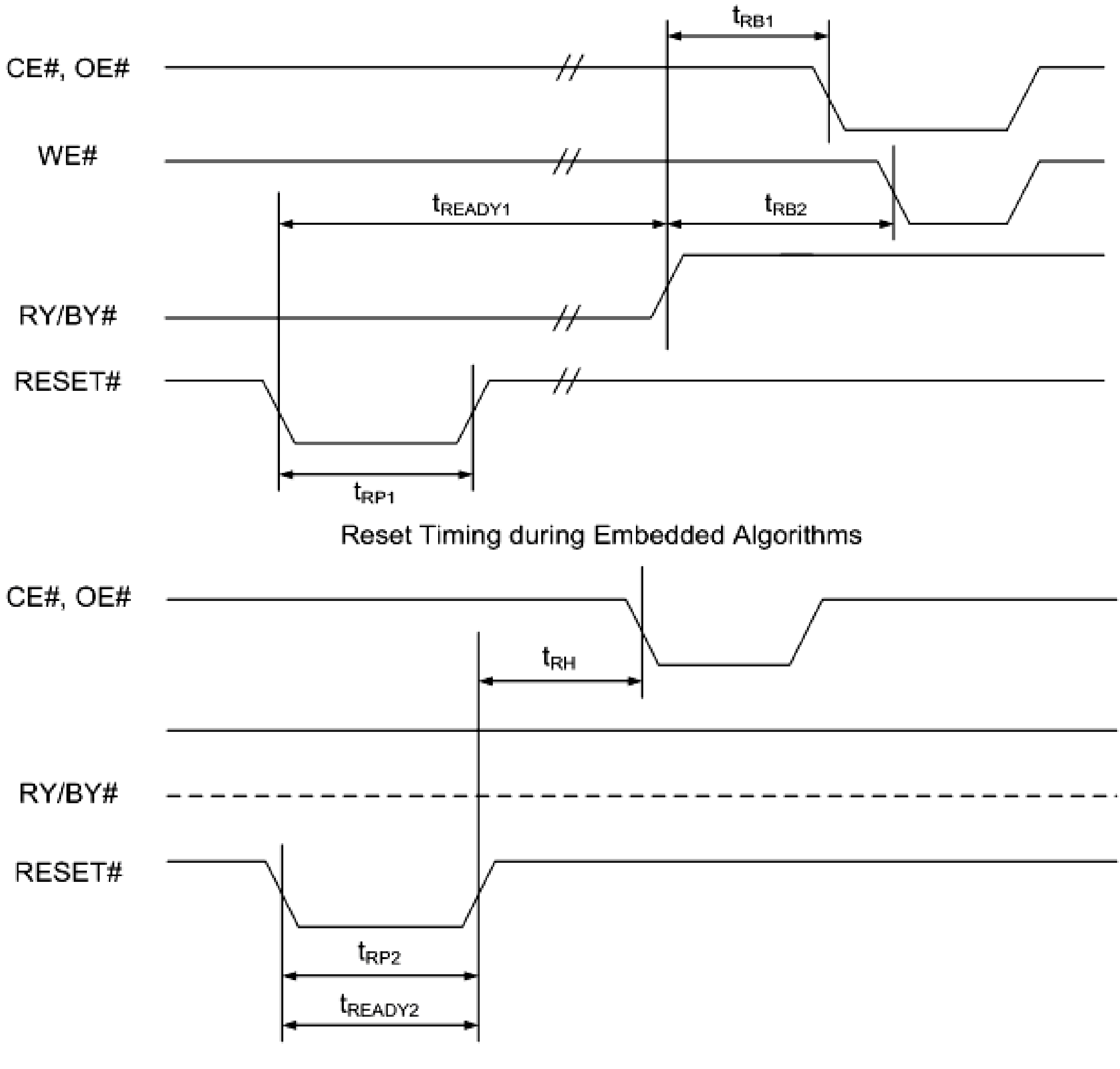
## 20.5 Reset

**Table 20.4** Hardware Reset (RESET#)

| Parameter | | Description | | All Speed Options | Unit |
|---|---|---|---|---|---|
| JEDEC | Std | | | | |
| | $t_{RP1}$ | RESET# Pulse Width (During Embedded Algorithms) | Min | 10 | us |
| | $t_{RP2}$ | RESET# Pulse Width (NOT During Embedded Algorithms) | Min | 500 | ns |
| | $t_{RH}$ | Reset# High Time Before Read | Min | 50 | ns |
| | $t_{RB1}$ | RY/BY# Recovery Time ( to CE#, OE# go low) | Min | 0 | ns |
| | $t_{RB2}$ | RY/BY# Recovery Time ( to WE# go low) | Min | 50 | ns |
| | $t_{READY1}$ | Reset# Pin Low (During Embedded Algorithms) to Read Mode (See Note) | Max | 20 | us |
| | $t_{READY2}$ | Reset# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note) | Max | 500 | ns |

**Note**
Not 100% tested.

**Figure 20.5** Reset Timings




Reset Timing during Embedded Algorithms

Reset Timing NOT during Embedded Algorithms

## 20.6 Erase/Program Operations

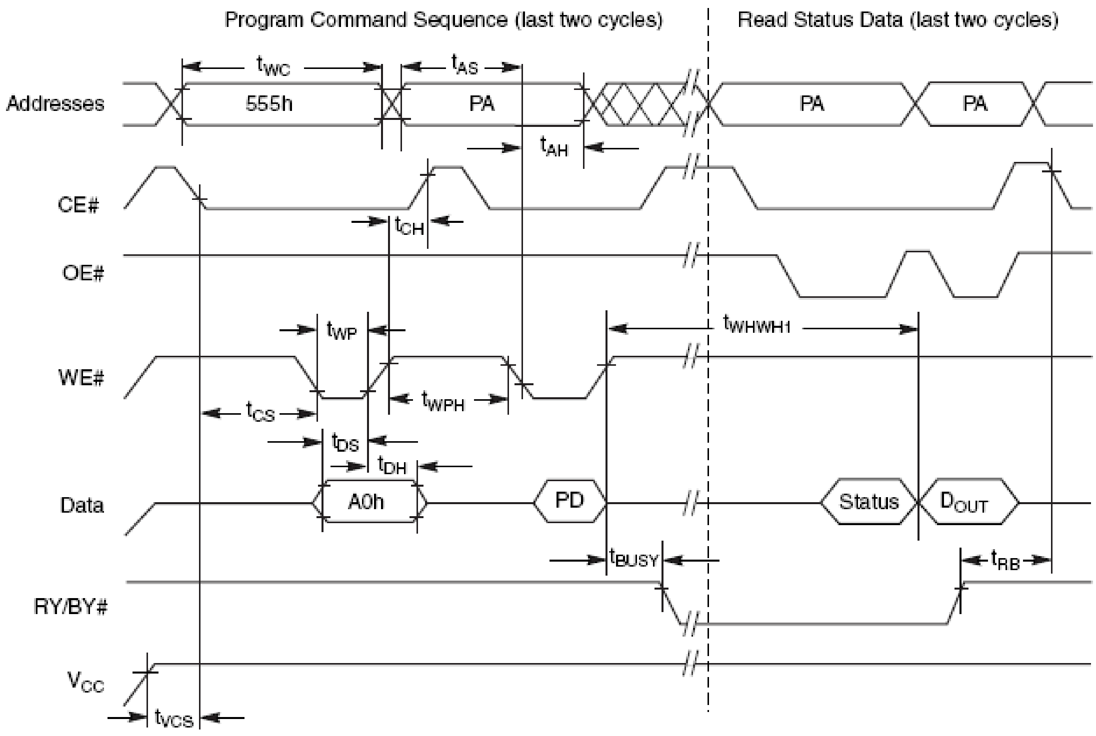
**Table 20.5** Erase and Program Operations

| Parameter | | Description | | Speed Options (ns) | |
|---|---|---|---|---|---|
| JEDEC | Std | | | 70 | Unit |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time (Note 1) | Min | 70 | |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | Min | 0 | ns |
| | $t_{ASO}$ | Address Setup Time to OE# low during toggle bit polling | Min | 15 | ns |
| $t_{WLAX}$ | $t_{AH}$ | Address Hold Time | Min | 35 | ns |
| | $t_{AHT}$ | Address Hold Time From CE# or OE# high during toggle bit polling | Min | 0 | ns |
| $t_{DVWH}$ | $t_{DS}$ | Data Setup Time | Min | 30 | ns |
| $t_{WHDX}$ | $t_{DH}$ | Data Hold Time | Min | 0 | ns |
| | $t_{OEPH}$ | Output Enable High during toggle bit polling | Min | 10 | ns |
| $t_{GHWL}$ | $t_{GHWL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | Min | 0 | ns |
| $t_{ELWL}$ | $t_{CS}$ | CE# Setup Time | Min | 0 | ns |
| $t_{WHEH}$ | $t_{CH}$ | CE# Hold Time | Min | 0 | ns |
| $t_{WLWH}$ | $t_{WP}$ | Write Pulse Width | Min | 35 | ns |
| $t_{WHDL}$ | $t_{WPH}$ | Write Pulse Width High | Min | 25 | ns |
| | $t_{SR/W}$ | Latency Between Read and Write Operations | Min | 0 | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Programming Operation (Note 2) | Typ | 8 | µs |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Accelerated Programming Operation (Note 2) | Typ | 7 | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2) | Typ | 0.1 | sec |
| | $t_{VCS}$ | $V_{CC}$ Setup Time (Note 1) | Min | 50 | µs |
| | $t_{RB}$ | Write Recovery Time from RY/BY# | Min | 0 | ns |
| | $t_{BUSY}$ | Program/Erase Valid to RY/BY# Delay | Max | 90 | ns |
| | | | Min | 35 | ns |
| | $t_{PSL}$ | Program Suspend Latency | Max | 35 | µs |
| | $t_{ESL}$ | Erase Suspend Latency | Max | 35 | µs |

**Notes:**
1. Not 100% tested.
2. See Table 21.4 for more information.

## 20.7 Timing Diagrams

**Figure 20.6** Program Operation Timings




**Notes**

1. PA = program address, PD = program data, $D_{OUT}$ is the true data at the program address

**Figure 20.7** Accelerated Program Timing Diagram

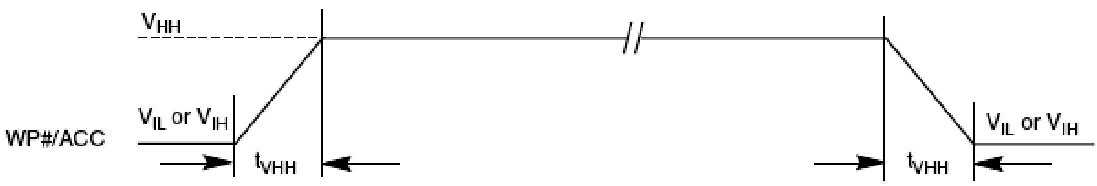
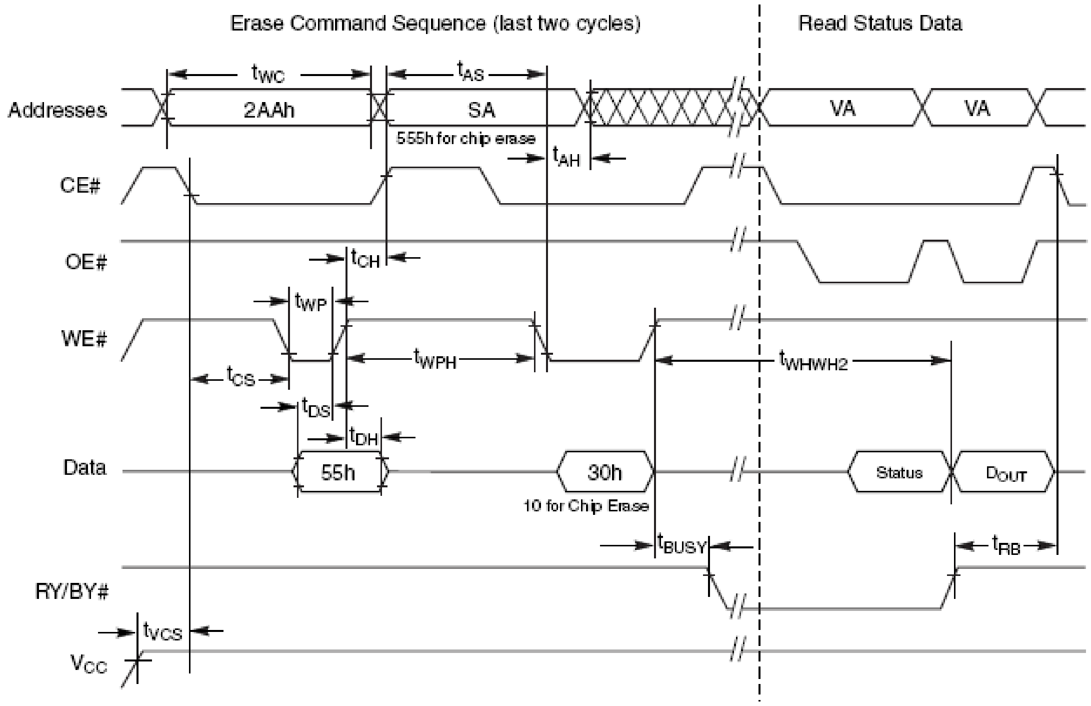


**Figure 20.8** Chip/Sector Erase Operation Timings




**Notes**

1. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see Write Operation Status )

**Figure 20.9** Back-to-back Read/Write Cycle Timings

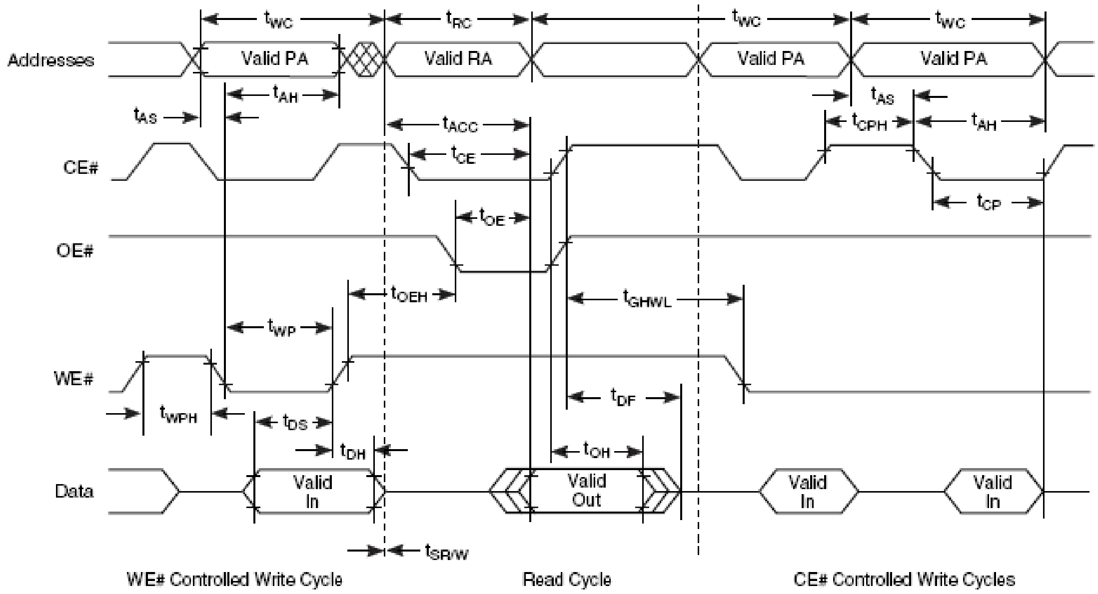
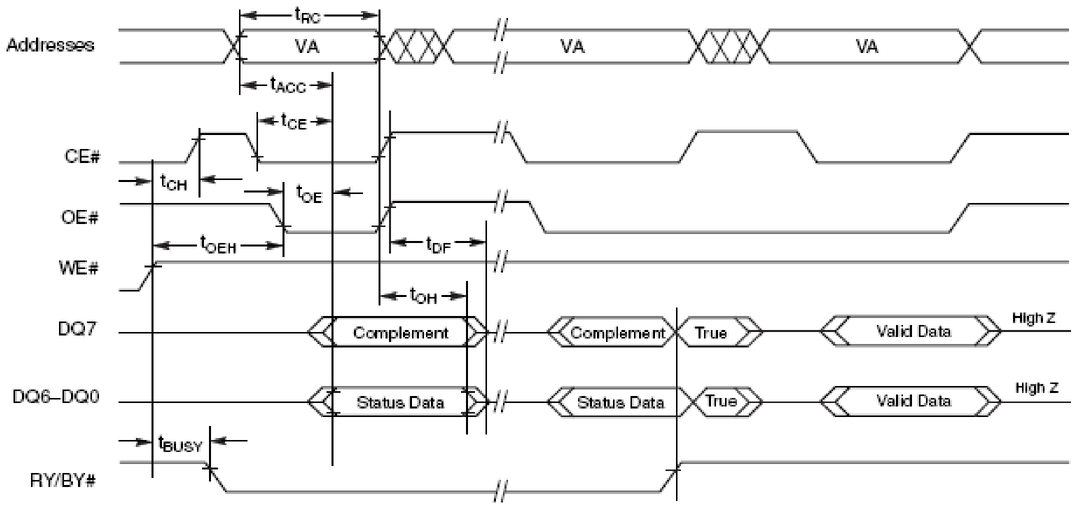
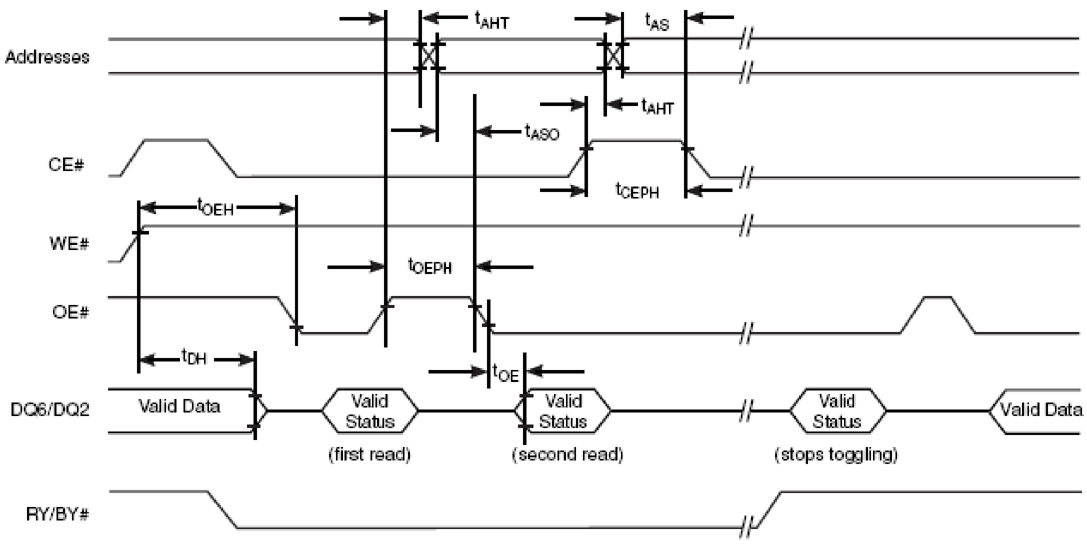


**Figure 20.10** Data# Polling Timings (During Embedded Algorithms)



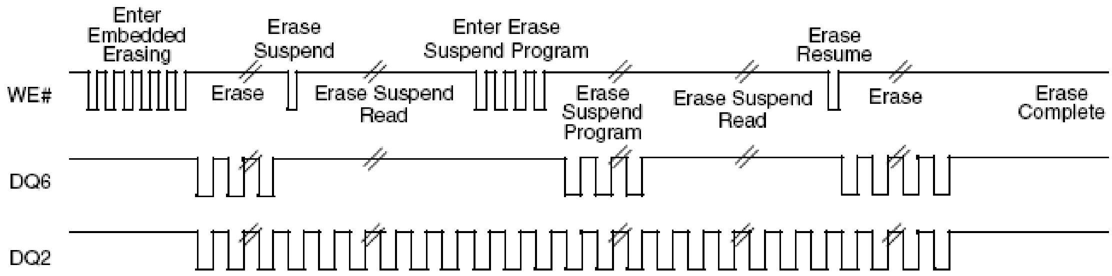

**Note**
VA = Valid address. The illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle

**Figure 20.11** Toggle Bit Timings (During Embedded Algorithms)




**Notes**
1. VA = Valid address; not required for DQ6. The illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle

**Figure 20.12** DQ2 vs. DQ6




**Note**
DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.

## 21. Protect/Unprotect

**Table 21.1** Temporary Sector Unprotect

| Parameter | | Description | | All Speed Options | Unit |
|---|---|---|---|---|---|
| JEDEC | Std | | | | |
| | $t_{VIDR}$ | $V_{ID}$ Rise and Fall Time (See Note) | Min | 500 | ns |
| | $t_{VHH}$ | $V_{HH}$ Rise and Fall Time (See Note) | Min | 250 | ns |
| | $t_{RSP}$ | RESET# Setup Time for Temporary Sector Unprotect | Min | 4 | μs |
| | $t_{RRB}$ | RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect | Min | 4 | μs |

**Note**
Not 100% tested

**Figure 21.1** Temporary Sector Unprotect Timing Diagram

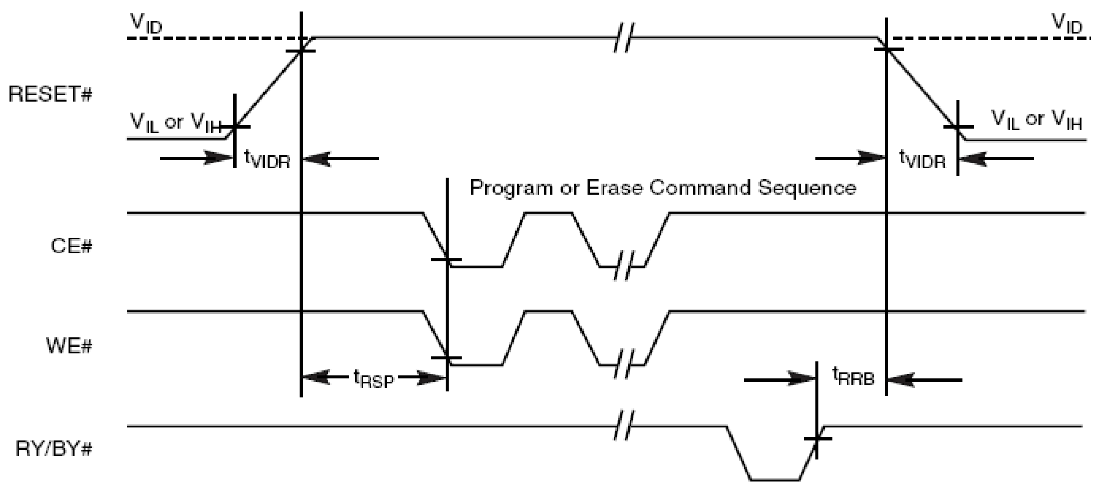
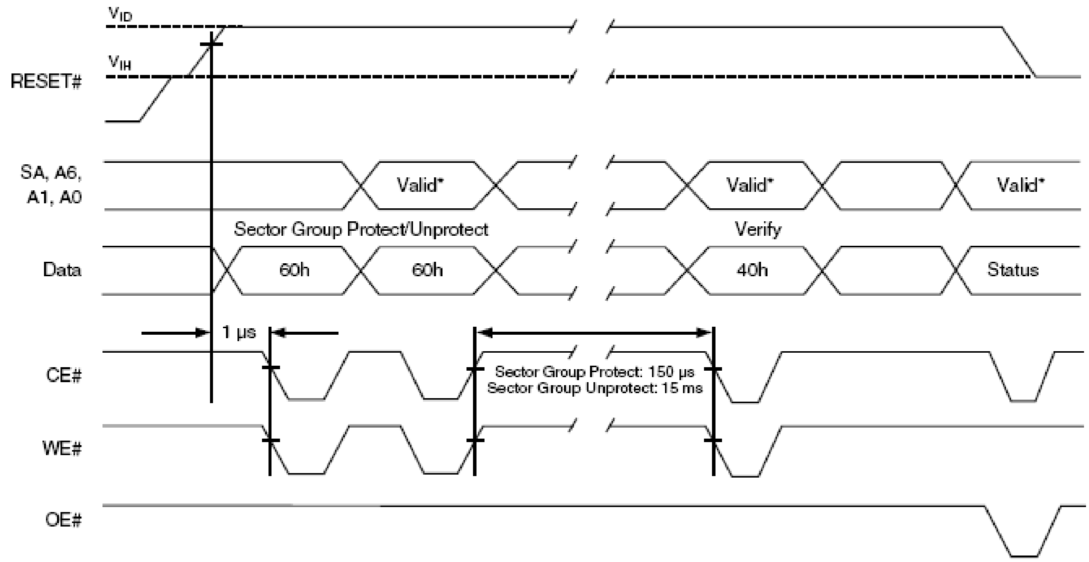


**Figure 21.2** Sector/Sector Block Protect and Unprotect Timing Diagram




**Notes**
1. For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0.

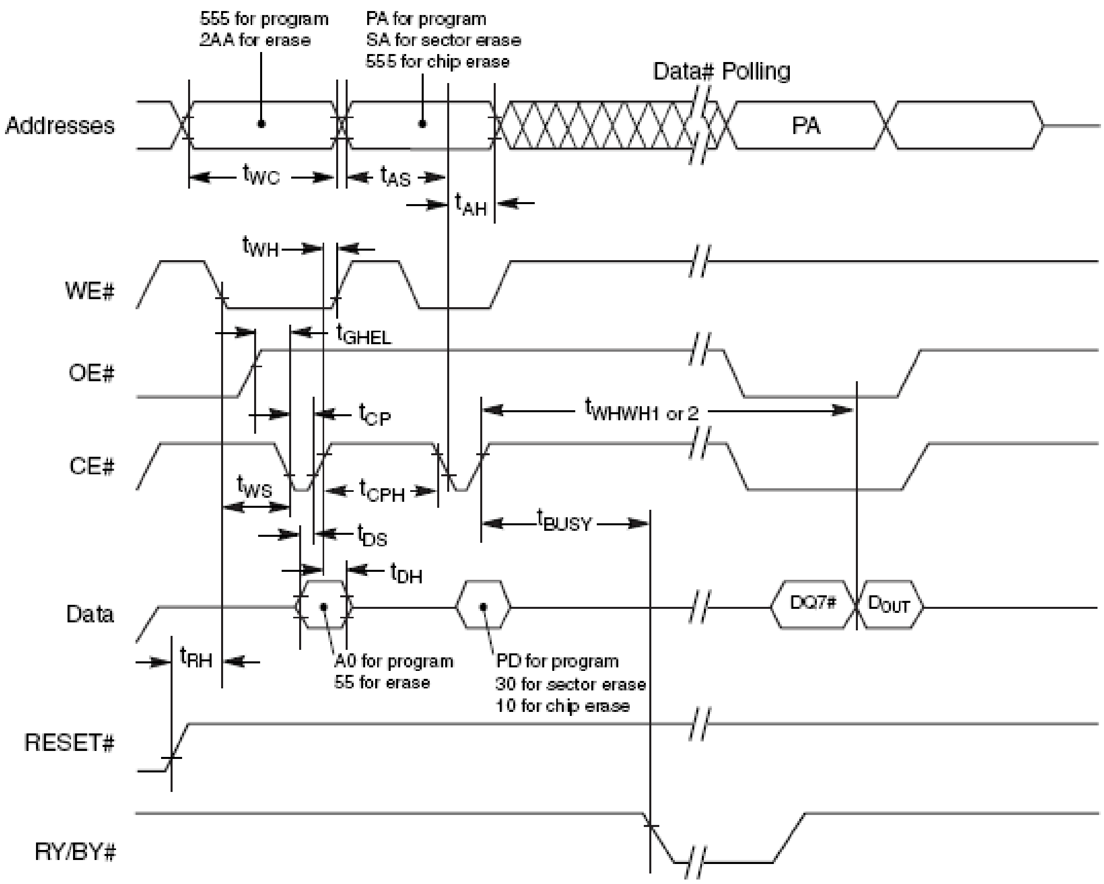
## 21.1 Controlled Erase Operations

**Table 21.2** Alternate CE# Controlled Erase and Program Operations

| Parameter | | Description (Notes) | | Speed Options | Unit |
|---|---|---|---|---|---|
| JEDEC | Std | | | 70 | |
| $t_{AVAV}$ | $t_{WC}$ | Write Cycle Time (Note 1) | Min | 70 | ns |
| $t_{AVWL}$ | $t_{AS}$ | Address Setup Time | Min | 0 | ns |
| $t_{ELAX}$ | $t_{AH}$ | Address Hold Time | Min | 35 | ns |
| $t_{DVEH}$ | $t_{DS}$ | Data Setup Time | Min | 30 | ns |
| $t_{EHDX}$ | $t_{DH}$ | Data Hold Time | Min | 0 | ns |
| $t_{GHEL}$ | $t_{GHEL}$ | Read Recovery Time Before Write (OE# High to WE# Low) | Min | 0 | ns |
| $t_{WLEL}$ | $t_{WS}$ | WE# Setup Time | Min | 0 | ns |
| $t_{EHWH}$ | $t_{WH}$ | WE# Hold Time | Min | 0 | ns |
| $t_{ELEH}$ | $t_{CP}$ | CE# Pulse Width | Min | 35 | ns |
| $t_{EHEL}$ | $t_{CPH}$ | CE# Pulse Width High | Min | 25 | ns |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Programming Operation (Note 2) | Typ | 8 | µs |
| $t_{WHWH1}$ | $t_{WHWH1}$ | Accelerated Programming Operation (Note 2) | Typ | 7 | µs |
| $t_{WHWH2}$ | $t_{WHWH2}$ | Sector Erase Operation (Note 2) | Typ | 0.1 | sec |

**Notes**
1. Not 100% tested.
2. See Erase and Programming Performance for more information.

**Figure 21.3** Alternate CE# Controlled Write (Erase/Program) Operation Timings 555 for program PA for program




**Notes**

1. Figure indicates last two bus cycles of a program or erase operation.
2. PA = program address, SA = sector address, PD = program data.
3. DQ7# is the complement of the data written to the device. $D_{OUT}$ is the data written to the device

**Table 21.4** Erase and Programming Performance

| Parameter | Typ (Note 1) | Max (Note 2) | Unit | Comments |
|---|---|---|---|---|
| Sector Erase Time | 0.1 | 2 | sec | Excludes 00h programming prior to erasure (Note 4) |
| Chip Erase Time | 8 | 62.4 | sec | |
| Word Program Time | 8 | 200 | µs | Excludes system level overhead (Note 5) |
| Accelerated Word Program Time | 7 | 200 | µs | |
| Chip Program Time (Note 3) | 12.6 | 25.2 | sec | |

## Notes

1. Typical program and erase times assume the following conditions: 25°C, 3.0V $V_{CC}$, Additionally, programming typical assume checkerboard pattern. All values are subject to change.
2. Under worst case conditions of $V_{CC}$ = 2.7 V, 100,000 cycles. All values are subject to change.
3. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.
4. In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.
5. System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 15.1 for further information on command definitions.
6. The device has a minimum erase and program cycle endurance of 100,000 cycles.

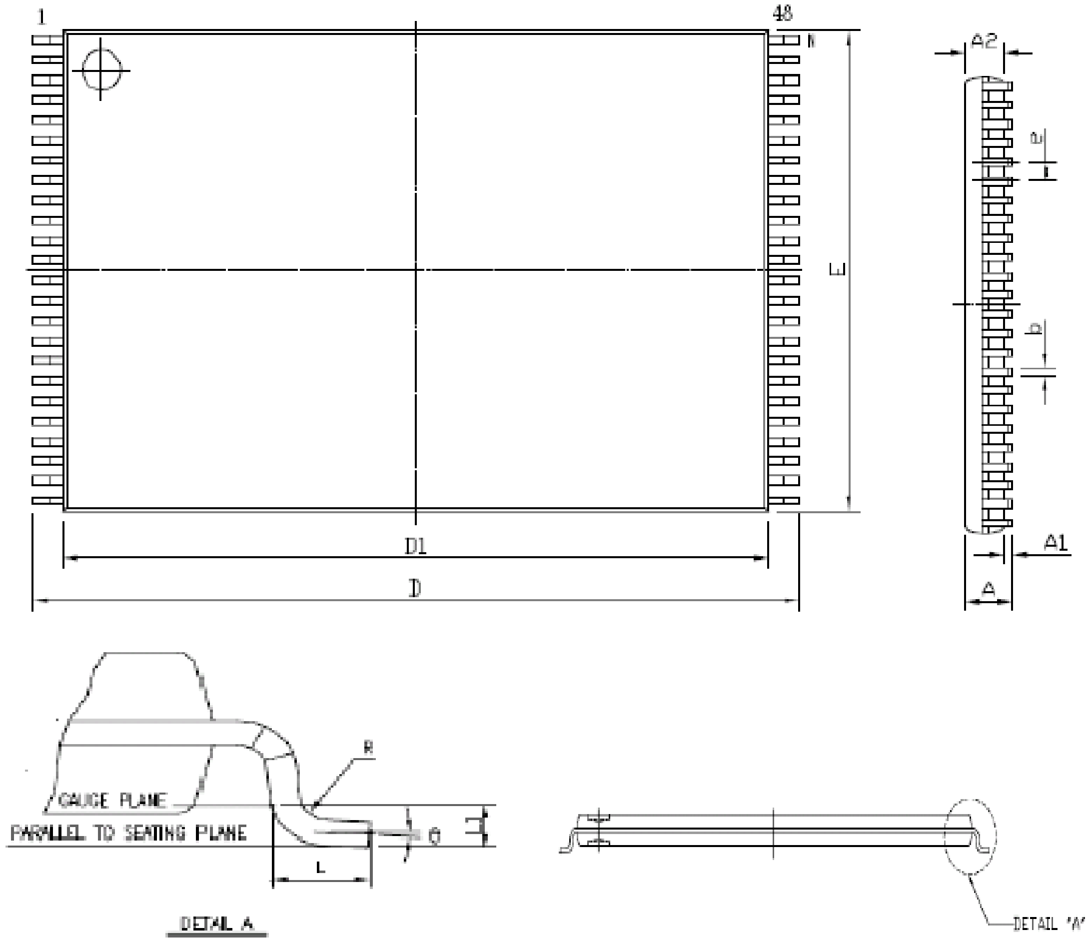
## 22. 48-PIN TSOP PACKAGE CAPACITANCE

| Parameter Symbol | Parameter Description | Test Setup | Typ | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0 | 6 | 7.5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0 | 8.5 | 12 | pF |
| $C_{IN2}$ | Control Pin Capacitance | $V_{IN}$ = 0 | 7.5 | 9 | pF |

**Note:** Test conditions are Temperature = 25°C and f = 1.0 MHz

## 23. Physical Dimensions

### Figure 24.1 TSOP 48-pin 12mm x 20mm




| SYMBOL | DIMENSION IN MM | | |
|---|---|---|---|
| | MIN. | NOR | MAX |
| A | - - - | - - - | 1.20 |
| A1 | 0.05 | - - - | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| D | 19.80 | 20.00 | 20.20 |
| D1 | 18.30 | 18.40 | 18.50 |
| E | 11.9 | 12.00 | 12.10 |
| e | - - - | 0.50 | - - - |
| b | 0.17 | 0.22 | 0.27 |
| L | 0.5 | 0.60 | 0.70 |
| L1 | - - - | 0.25 | - - - |
| R | 0.08 | - - - | 0.20 |
| θ | $0^0$ | $3^0$ | $5^0$ |

Note : 1. Coplanarity: 0.1 mm
2. Max. allowable mold flash is 0.15 mm at the pkg ends, 0.25 mm between leads.

## Revisions List

| Revision No | Description | Date |
|---|---|---|
| A | Initial Release | 2010/11/23 |
| B | Update Selecting a Sector Protection Mode description on page 17. | 2010/12/27 |