EN71SN10F

1.8V NAND Flash + 1.8V Mobile DDR SDRAM Multi-Chip Package

Features

- Multi-Chip Package
  - NAND Flash Density: 1-Gbits
  - Mobile DDR SDRAM Density: 512-Mbit
- Device Packaging
  - 107 balls FBGA

  Area: 10.5x13 mm; Height: 1.2 mm
- Operating Voltage
  - NAND : 1.7V to 1.95V
  - Mobile DDR SDRAM : 1.7V to 1.95V
- Operating Temperature :-25 °C to +85 °C

NAND FLASH

- Voltage Supply: 1.8V (1.7V ~ 1.95V)
- Organization
  - Memory Cell Array :
    (128M + 4M) x 8bit for 1Gb
  - Multiplexed address/ data
  - Data Register : (2K + 64) x 8bit
- Automatic Program and Erase
  - Page Program : (2K + 64) bytes
  - Block Erase : (128K + 4K) bytes
- Page Read Operation
  - Page Size : (2K + 64) bytes
  - Random Read : 25µs (Max.)
  - Serial Access : 45ns (Min.)
- Memory Cell: 1bit/Memory Cell
- Fast Write Cycle Time
  - Page Program Time : 250µs (Typ.)
  - Block Erase Time : 2ms (Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
- Endurance:
  - 100K Program/Erase Cycles (with 1 bit/528 bytes ECC)
  - Data Retention: 10 Years
- Command Register Operation
- Automatic Page 0 Read at Power-Up Option
  - Boot from NAND support
  - Automatic Memory Download
- NOP: 4 cycles
- Cache Program/Read Operation
- Copy-Back Operation
- EDO mode
- OTP Operation

Mobile DDR SDRAM

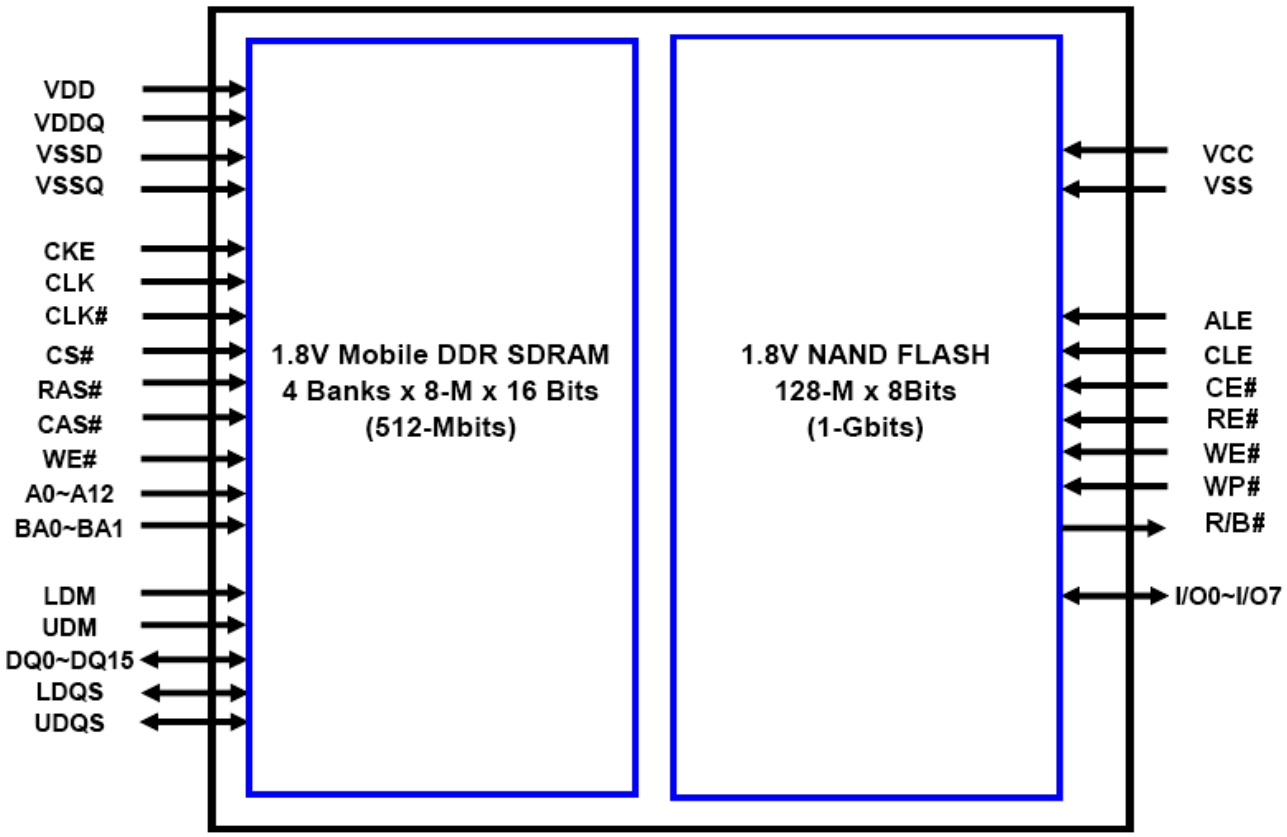
- Density: 512M bits
- Organization: 8M words x16 bits x 4 banks
- Power supply: V_{DD}/V_{DDQ}= 1.70~1.95V
- Speed: 400Mbps (max.) for data rate
- 2KB page size
  - Row address: A0 to A12
  - Column address: A0 to A9
- Four internal banks for concurrent operation
- Interface: LVCMOS
- Burst Length : 2, 4, 8, or 16
- Burst Type : Sequential and Interleave
- CAS# Latency (CL) : 3
- Precharge: auto precharge option for each burst access
- Drive Strength: normal, 1/2, 1/4, 1/8
- Refresh: auto Refresh and self-refresh
- Refresh cycles: 8192 cycles/64ms
- Optional Partial Array Self Refresh (PASR)
- Auto Temperature Compensated Self Refresh (ATCSR) by built-in temperature sensor
- Deep Power Down Mode
- Burst termination by burst stop command and precharge command
- DLL in not implemented
- Double-data-rate architecture, two data access per clock cycle
- The high-speed data transfer is realized by the 2 bits prefetch pipelined architecture
- Bidirectional data strobe (DQS) is transmitted /received with data for capturing data at the receiver
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CLK and CLK#)
- Commands entered on each positive CLK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data

Rev. A, Issue Date: 2012/12/07

Ordering Information

Product ID	NAND Flash		Mobile DDR SDRAM		Package	Operation Temperature Range
	Configuration	Speed	Configuration	Speed		
EN71SN10F-45CFWP	1Gb (128M X 8 bits)	45ns	512Mb (4 Banks X 8M X 16 bits)	200MHz	107 ball FBGA	Wireless

MCP Block Diagram



Ball Configuration

(TOP VIEW)
(FBGA 107, 10.5mmx13mmx1.2mm Boby, 0.8mm Ball Pitch)

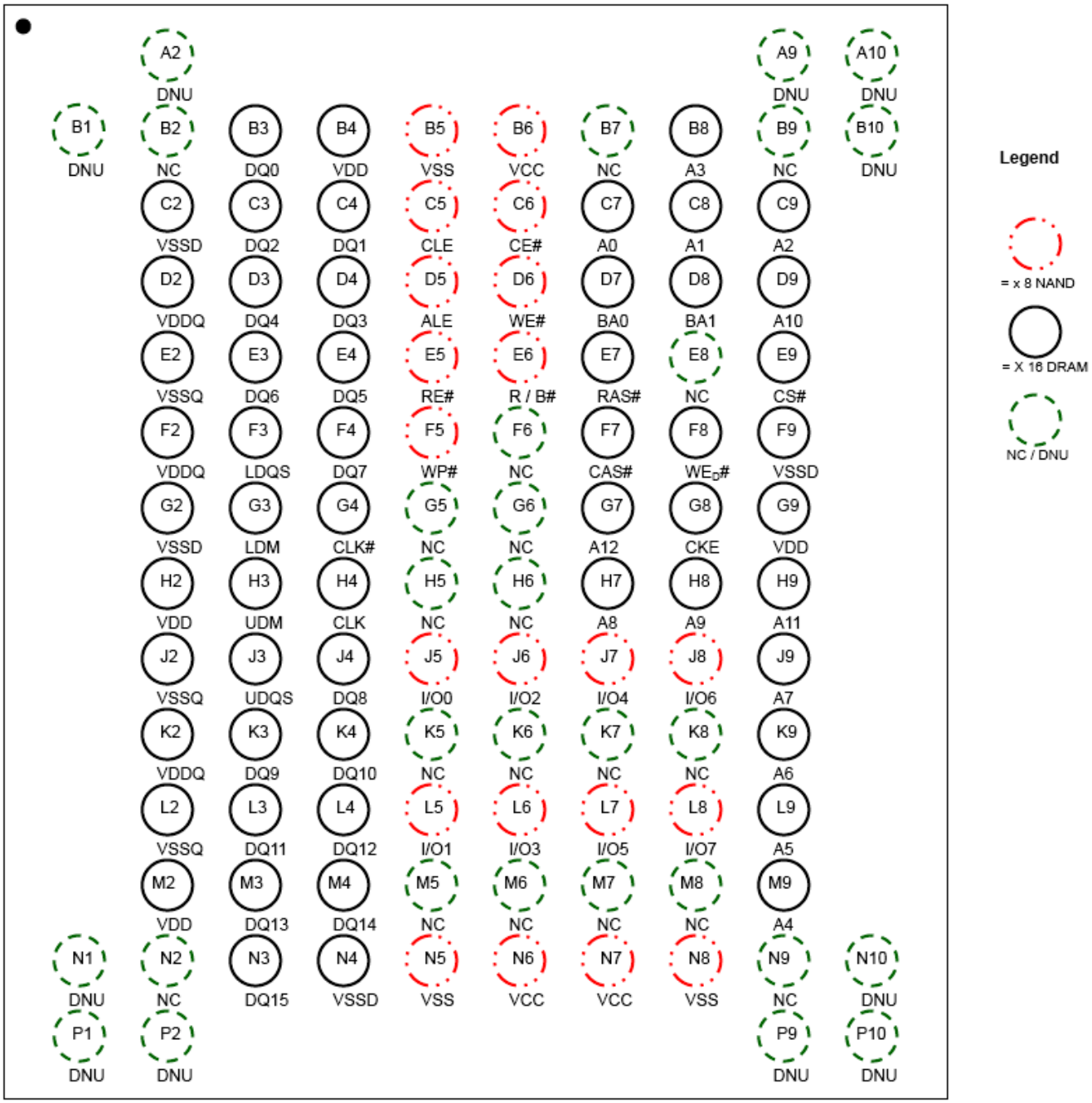
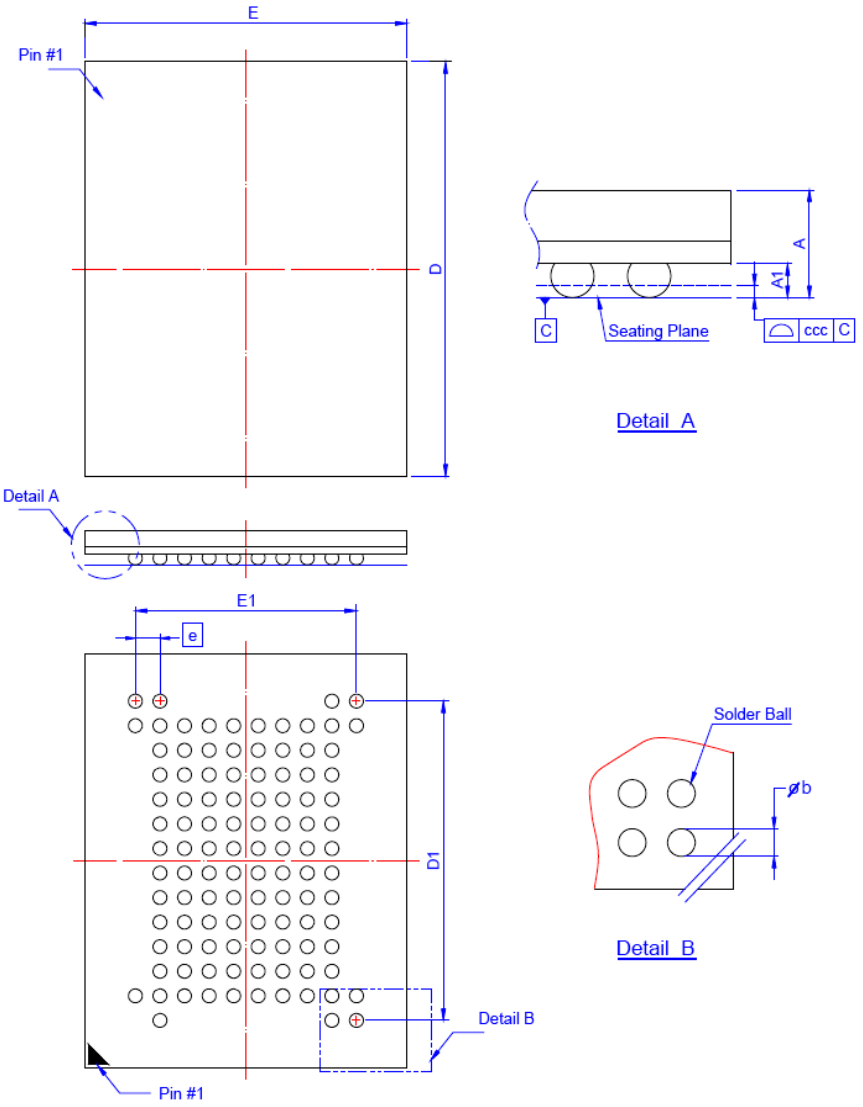


Table 1. Ball Description

Pin Name	Type	Function
NAND		
VCC	Supply	Supply Voltage
VSS	Supply	Ground
I/O0-7	Input/output	Data input/outputs, address inputs, or command inputs
ALE	Input	Address Latch Enable
CLE	Input	Command Latch Enable
CE#	Input	Chip Enable
RE#	Input	Read Enable
WE#	Input	Write Enable
WP#	Input	Write Protect
R / B#	Output	Ready/Busy (open-drain output)
Mobile DDR SDRAM		
VDD	Supply	Power Supply
VSSD	Supply	Ground
VDDQ	Supply	DQ's Power Supply: Isolated on the die for improved noise immunity.
VSSQ	Supply	Ground
CLK, CLK#	Input	CLK and CLK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of CLK# . Input and output data is referenced to the crossing of CLK and CLK# (both directions of crossing). Internal clock signals are derived from CLK, CLK#
CKE	Input	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWERDOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CLK, CLK# and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
CS#	Input	CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.
RAS# , CAS# , WE#	Input	CAS#, RAS# , and WE# (along with CS#) define the command being entered.
A0-A12	Input	Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ / WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command.
BA0, BA1	Input	BA0 and BA1 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
DQ0-15	Input / Output	Data Input/Output pins operate in the same manner as on conventional DRAMs.
LDQS, UDQS	Input / Output	Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. LDQS corresponds to the data on DQ0-DQ7, UDQS corresponds to the data on DQ8-DQ15.
LDM, UDM	Input	DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading. LDM corresponds to the data on DQ0-DQ7, UDM corresponds to the data on DQ8-DQ15.

PACKAGE DIMENSION
107-BALL FBGA (10.5x13 mm)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	1.07	1.14	1.21	0.042	0.045	0.048
A_1	0.35	0.40	0.45	0.014	0.016	0.018
Φb	0.45	0.50	0.55	0.018	0.020	0.022
D	12.90	13.00	13.10	0.508	0.512	0.516
E	10.40	10.50	10.60	0.409	0.413	0.417
D_1	10.40 BSC			0.409 BSC		
E_1	7.20 BSC			0.283 BSC		
e	0.80 BSC			0.031 BSC		
ccc	———	———	0.10	———	———	0.004

Controlling dimension : Millimeter.

NAND Flash Memory Operations

General Description

The NAND Flash is a 128Mx8bit with spare 4Mx8bit capacity. The NAND Flash is offered in 1.8V VCC Power Supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The NAND Flash contains 1024 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. A program operation allows to write the 1056-Word page in typical 250us and an erase operation can be performed in typical 2ms on a 128K-Byte for device block.

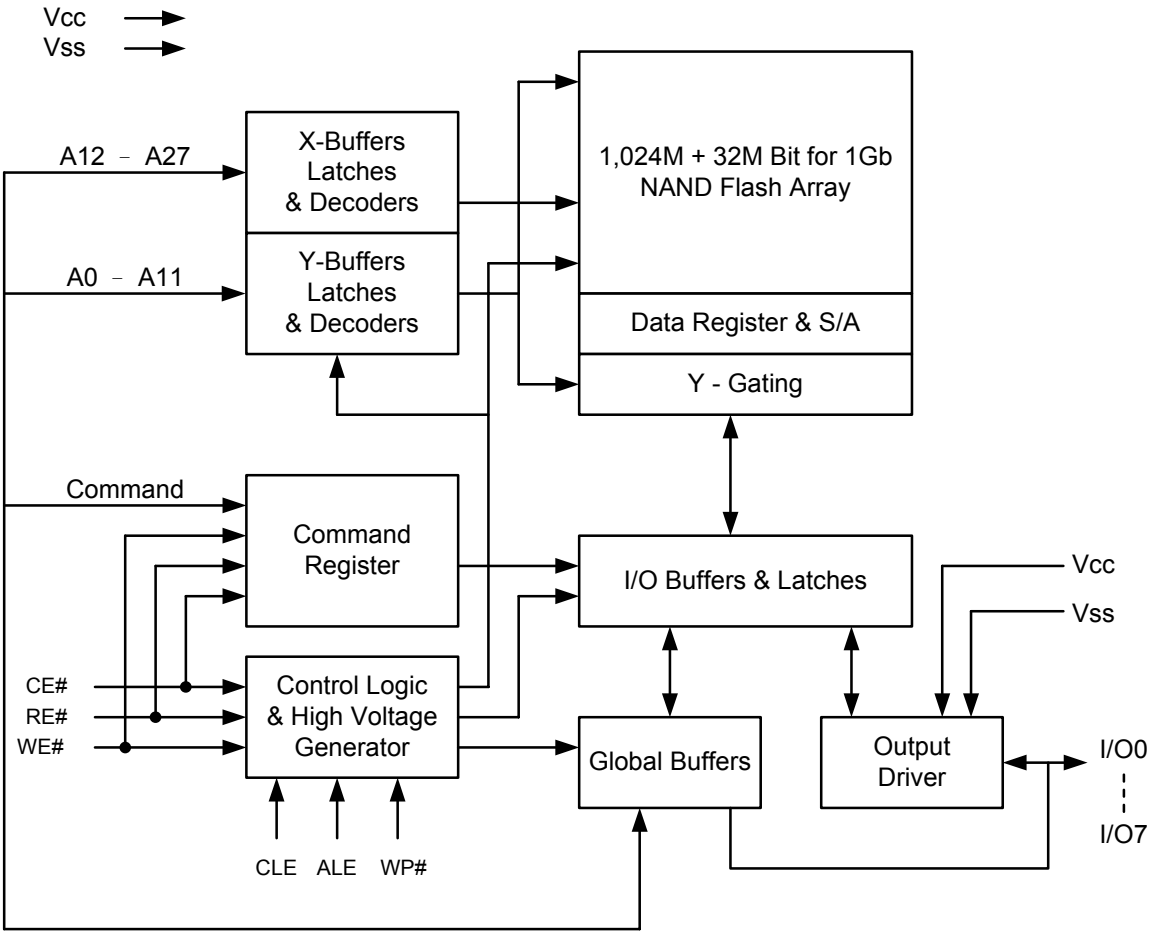
Data in the page mode can be read out at 45ns cycle time per Byte. The I/O pins serve as the ports for address and command inputs as well as data input/output. The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. The cache program feature allows the data insertion in the cache register while the data register is copied into the Flash array. This pipelined program operation improves the program throughput when long files are written inside the memory. A cache read feature is also implemented. This feature allows to dramatically improving the read throughput when consecutive pages have to be streamed out. This NAND Flash includes extra feature: Automatic Read at Power Up.

Table 2. Pin Description

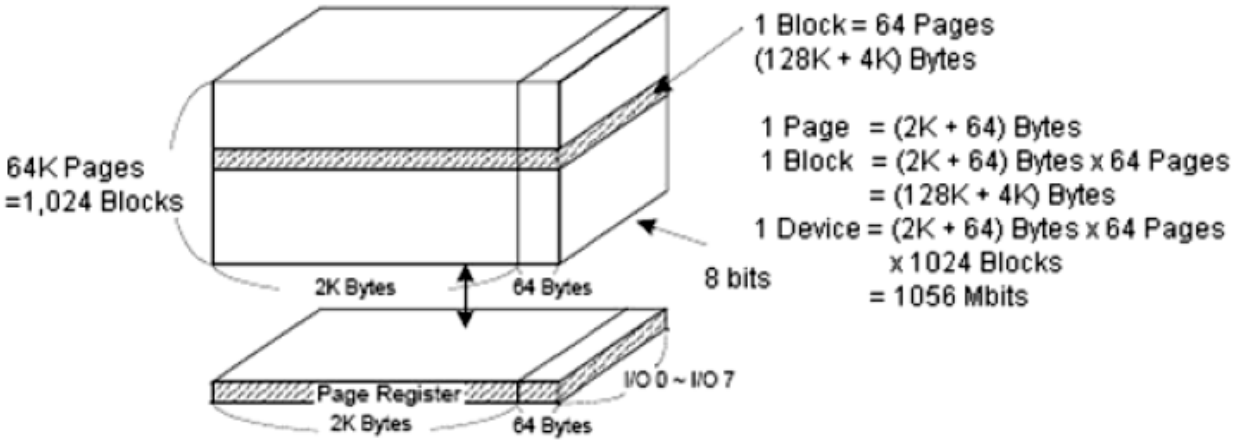
Symbol	Pin Name	Function
I/O0 – I/O7	Data Inputs/Outputs	The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to Hi-Z when the chip is deselected or when the outputs are disabled.
CLE	Command Latch Enable	The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE# signal.
ALE	Address Latch Enable	The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE# with ALE high.
CE#	Chip Enable	The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE# control during read operation, refer to 'Page read' section of Device operation.
RE#	Read Enable	The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t_{REA} after the falling edge of RE# which also increments the internal column address counter by one.
WE#	Write Enable	The WE# input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	Write Protect	The WP# pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	Ready/Busy Output	The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to Hi-Z condition when the chip is deselected or when outputs are disabled.
V_{CC}	Power Supply	V_{CC} is the power supply for device.
V_{SS}	Ground	
NC	No Connection	Lead is not internally connected.

Note: Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs. Do not leave V_{CC} or V_{SS} disconnected.

Block Diagram



Array Organization



Address Cycle Map

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	Address
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	**Column Address**
2nd Cycle	A8	A9	A10	A11	L*	L*	L*	L*	**Column Address**
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	**Row Address**
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	**Row Address**

Note:

1. Column Address : Starting Address of the Register.
2. * L must be set to “Low”.
3. * The device ignores any additional input of address cycles than required.

Product Introduction

The NAND Flash is a 1,056Mbit memory organized as 64K rows (pages) by 2,112x8 columns. Spare 64x8 columns are located from column address of 2,048~2,111. A 2,112-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 1,024 separately erasable 128K-byte blocks. It indicates that the bit-by-bit erase operation is prohibited on the NAND Flash.

The NAND Flash has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE# to low while CE# is low. Those are latched on the rising edge of WE#. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution.

In addition to the enhanced architecture and interface, the NAND Flash incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory.

Command Set

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input (1)	85h	-	
Random Data Output (1)	05h	E0h	
Read Status	70h	-	O
Cache Program	80h	15h	
Cache Read	31h	-	
Read Start for Last Page Cache Read	3Fh	-	

Note:
1. Random Data Input / Output can be executed in a page.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	-0.6 to +2.45	V
	V_{IN}	-0.6 to +2.45	
	$V_{I/O}$	-0.6 to VCC + 0.3 (< 2.45)	
Temperature Under Bias	T_{BIAS}	-40 to +125	℃
Storage Temperature	T_{STG}	-65 to +150	℃
Short Circuit Current	I_{OS}	5	mA

Note:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

(Voltage reference to GND, T_A = – 25°C to 85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	1.7	1.8	1.95	V
Supply Voltage	V_{SS}	0	0	0	V

DC AND OPERATION CHARACTERISTICS

(Recommended operating conditions otherwise noted)

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating Current	Page Read with Serial Access	I_{CC1}	t_{RC}=45ns, CE# =V_{IL}, I_{OUT}=0mA	-	15	30	mA
	Program	I_{CC2}	-	-	15	30	
	Erase	I_{CC3}	-	-	15	30	
Stand-by Current (TTL)		I_{SB1}	CE# =V_{IH}, WP# =0V/V_{CC}	-	-	1	mA
Stand-by Current (CMOS)		I_{SB2}	CE# = V_{CC} -0.2, WP# =0V/ V_{CC}	-	10	50	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to V_{CC} (max)	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to V_{CC} (max)	-	-	±10	uA
Input High Voltage		V_{IH} (1)	-	0.8 x V_{CC}	-	V_{CC} +0.3	V
Input Low Voltage, All inputs		V_{IL} (1)	-	-0.3	-	0.2 x V_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH}=-100uA	V_{CC} -0.1	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}=+100uA	-	-	0.1	V
Output Low Current (R/B#)		I_{OL} (R /B#)	V_{OL}=0.1V	3	4	-	mA

Note:

1. V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to V_{CC}+0.4V for durations of 20ns or less.
2. Typical value are measured at V_{CC} =1.8V, T_A = 25℃. And not 100% tested.

VALID BLOCK

Symbol	Min.	Typ.	Max.	Unit
N_{VB}	1,004	-	1,024	Blocks

Note:

1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented as first shipped. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 1 bit/528 bytes ECC.

AC TEST CONDITION

(T_A = – 25°C to 85°C, V_{CC}=1.7V~1.95V)

Parameter	Condition
Input Pulse Levels	0V to V_{CC}
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	V_{CC} /2
Output Load	1 TTL Gate and C_L=30pF

Note:

* Refer to Ready / Busy# section, R/B# output's Busy to Ready time is decided by the pull-up resistor (R_P) tied to R/B# pin.

CAPACITANCE

(T_A = 25°C, V_{CC}=1.8V, f =1.0MHz)

Item	Symbol	Test Condition	Min.	Max.	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL} = 0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	10	pF

Note: Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L		H	X	Read Mode	Command Input
L	H	L		H	X		Address Input (4 clock)
H	L	L		H	H	Write Mode	Command Input
L	H	L		H	H		Address Input (4 clock)
L	L	L		H	H	Data Input	
L	L	L	H		X	Data Output	
X	X	X	X	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X (1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC} (2)	Stand-by	

Note:
1. X can be V_{IL} or V_{IH}.
2. WP# should be biased to CMOS high or CMOS low for stand-by.

Program / Erase Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Program Time	t_{PROG}	-	250	700	us
Dummy Busy Time for Cache Program	t_{CBSY}	-	3	700	us
Number of Partial Program Cycles in the Same Page	N_{OP}	-	-	4	Cycle
Block Erase Time	t_{BERS}	-	2	10	ms

Note:
1. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 1.8V V_{CC} and 25°C temperature.
2. t_{PROG} is the average program time of all pages. Users should be noted that the program time variation from page to page is possible.
3. Max. time of t_{CBSY} depends on timing between internal program completion and data in.

AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min.	Max.	Unit
CLE Setup Time	t_{CLS} (1)	25	-	ns
CLE Hold Time	t_{CLH}	10	-	ns
CE# Setup Time	t_{CS} (1)	35	-	ns
CE# Hold Time	t_{CH}	10	-	ns
WE# Pulse Width	t_{WP}	25	-	ns
ALE Setup Time	t_{ALS} (1)	25	-	ns
ALE Hold Time	t_{ALH}	10	-	ns
Data Setup Time	t_{DS} (1)	20	-	ns
Data Hold Time	t_{DH}	10	-	ns
Write Cycle Time	t_{WC}	45	-	ns
WE# High Hold Time	t_{WH}	15	-	ns
ALE to Data Loading Time	t_{ADL} (2)	100	-	ns

Note:

1. The transition of the corresponding control pins must occur only once while WE# is held low.
2. t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

AC Characteristics for Operation

Parameter		Symbol	Min.	Max.	Unit
Data Transfer from Cell to Register		t_R	-	25	us
ALE to RE# Delay		t_{AR}	10	-	ns
CLE to RE# Delay		t_{CLR}	10	-	ns
Ready to RE# Low		t_{RR}	20	-	ns
RE# Pulse Width		t_{RP}	25	-	ns
WE# High to Busy		t_{WB}	-	100	ns
WP# Low to WE# Low (disable mode)		t_{WW}	100	-	ns
WP# High to WE# Low (enable mode)					
Read Cycle Time		t_{RC}	45	-	ns
RE# Access Time		t_{REA}	-	30	ns
CE# Access Time		t_{CEA}	-	45	ns
RE# High to Output Hi-Z		t_{RHZ}	-	100	ns
CE# High to Output Hi-Z		t_{CHZ}	-	30	ns
CE# High to ALE or CLE Don't Care		t_{CSD}	0	-	ns
RE# High to Output Hold		t_{RHOH}	15	-	ns
RE# Low to Output Hold		t_{RLOH}	5	-	ns
CE# High to Output Hold		t_{COH}	15	-	ns
RE# High Hold Time		t_{REH}	15	-	ns
Output Hi-Z to RE# Low		t_{IR}	0	-	ns
RE# High to WE# Low		t_{RHW}	100	-	ns
WE# High to RE# Low		t_{WHR}	60	-	ns
Device Resetting Time during ...	Read	t_{RST}	-	5	us
	Program		-	10	us
	Erase		-	500	us
	Ready		-	5[1]	us
Cache Busy in Read Cache (following 31h and 3Fh)		t_{DCBSYR}	-	30	us

Note:

1. If reset command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

NAND Flash Technical Notes

Mask Out Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Eon. The information regarding the initial invalid block(s) is called as the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

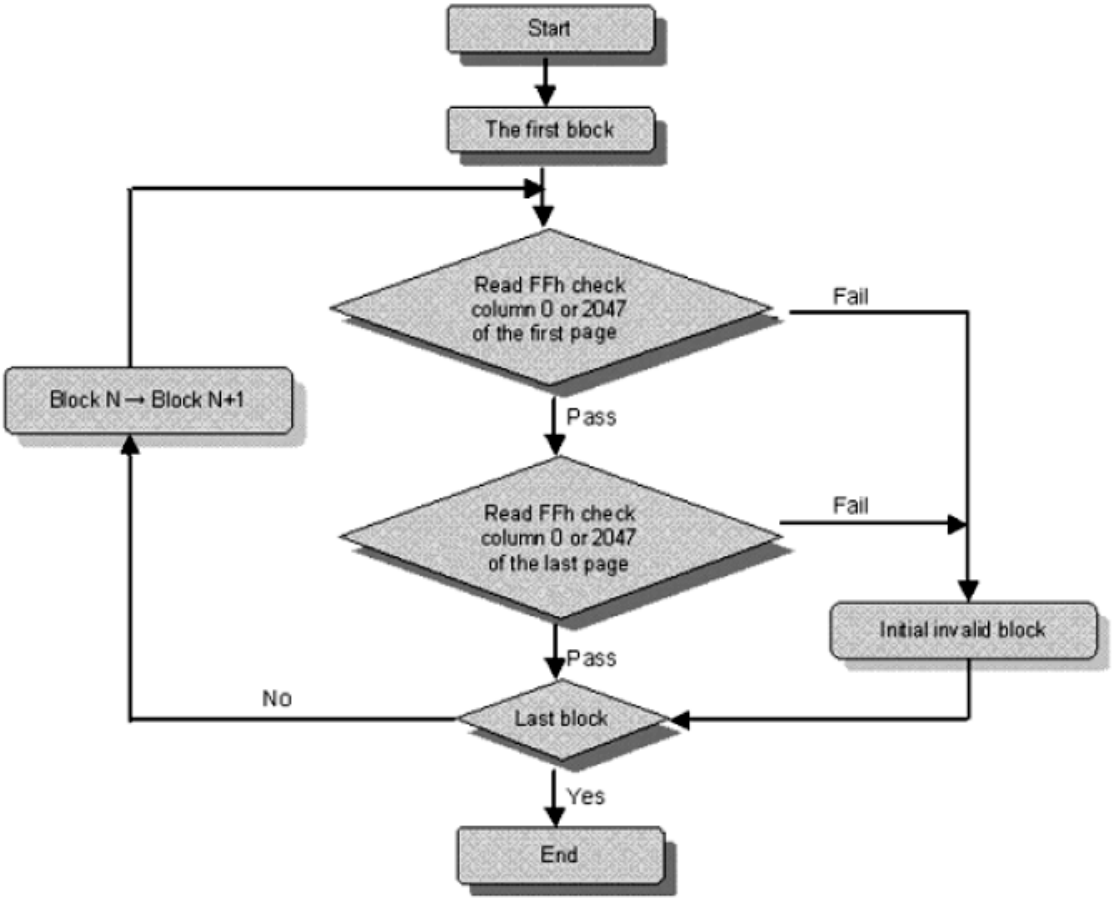
The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1 bit/528 bytes ECC.

Identifying Initial Invalid Block(s) and Block Replacement Management

Unpredictable behavior may result from programming or erasing the defective blocks. The under figure illustrates an algorithm for searching factory-mapped defects, and the algorithm needs to be executed prior to any erase or program operations.

A host controller has to scan blocks from block 0 to the last block using page read command and check the data at the column address of 0 or 2,047. If the read data is not FFh, the block is interpreted as an invalid block. The initial invalid block information is erasable, and which is impossible to be recovered once it has been erased. Therefore, the host controller must be able to recognize the initial invalid block information and to create a corresponding table to manage block replacement upon erase or program error when additional invalid blocks develop with Flash memory usage.

Algorithm for Bad Block Scanning




```
For (i=0; i<Num_of_LUs; i++)
{
      For (j=0; j<Blocks_Per_LU; j++)
      {
            Defect_Block_Found=False;

            Read_Page(lu=i, block=j, page=0);
            If (Data[coloumn=0]!=FFh)     Defect_Block_Found=True;
            If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

            Read_Page(lu=i, block=j, page=Page_Per_Block-1);
            If (Data[coloumn=0]!=FFh)     Defect_Block_Found=True;
            If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

            If (Defect_Block_Found)       Mark_Block_as_Defective(lu=i, block=j);
      }
}
```

Error in Write or Read Operation

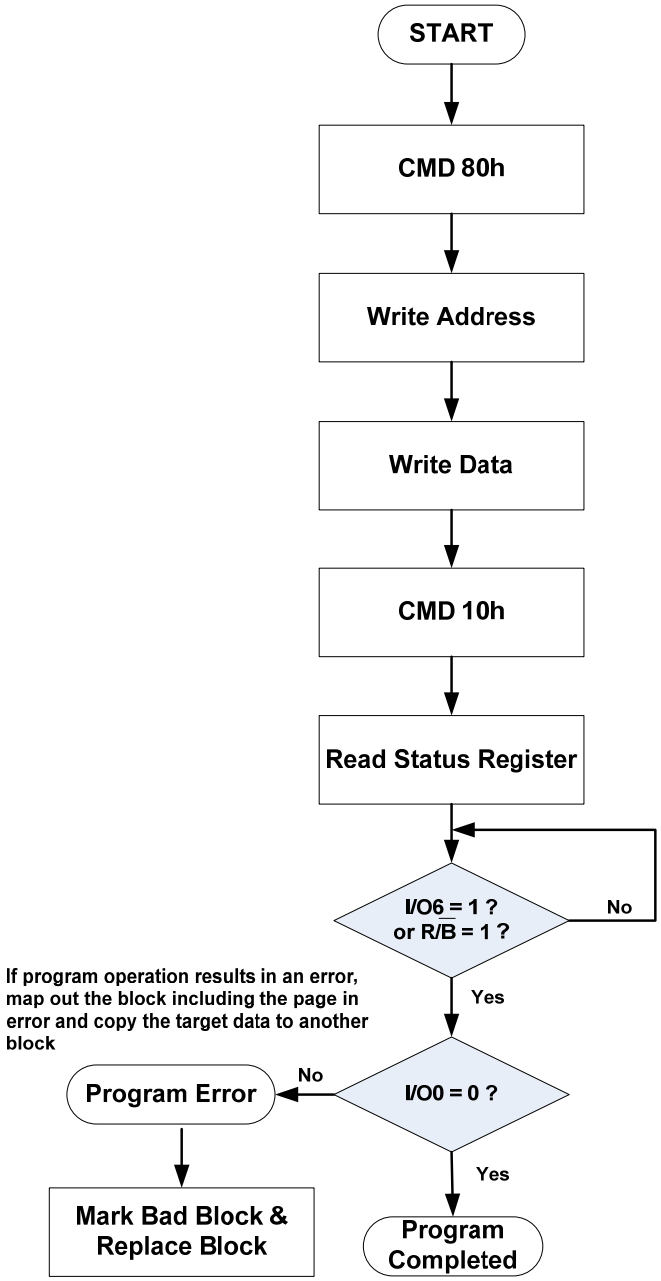
Within its lifetime, the additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.

Failure		Detection and Countermeasure sequence
Write	Erase Failure	Read Status after Erase → Block Replacement
	Program Failure	Read Status after Program → Block Replacement
Read	Single Bits Failure	Verify ECC → ECC Correction

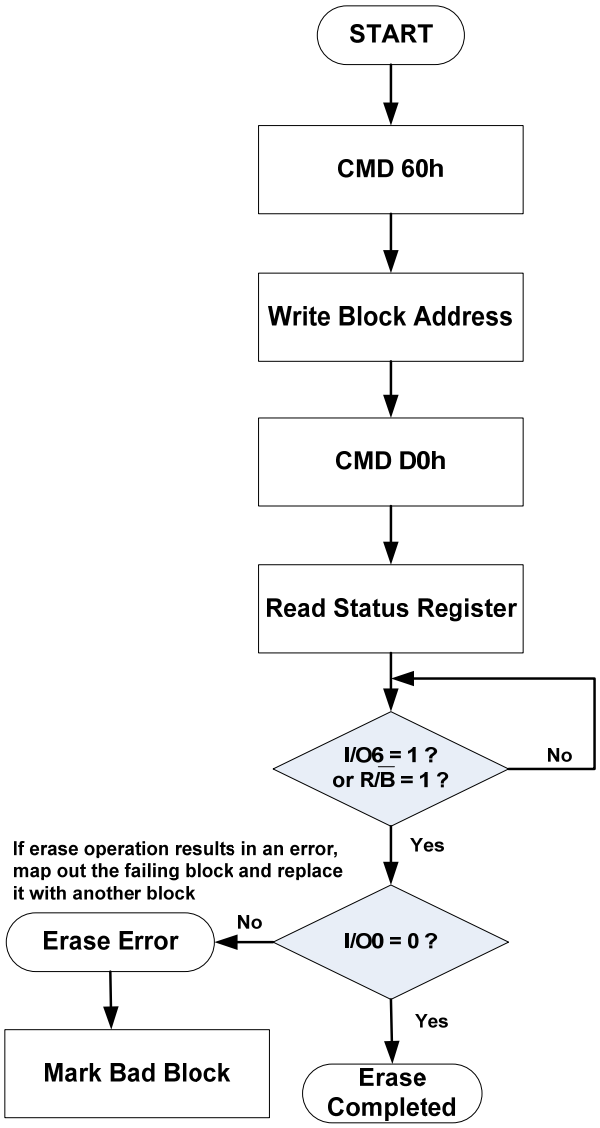
Note:

1. Error Correcting Code --> Hamming Code etc.
2. Example: 1bit correction / 528 Byte

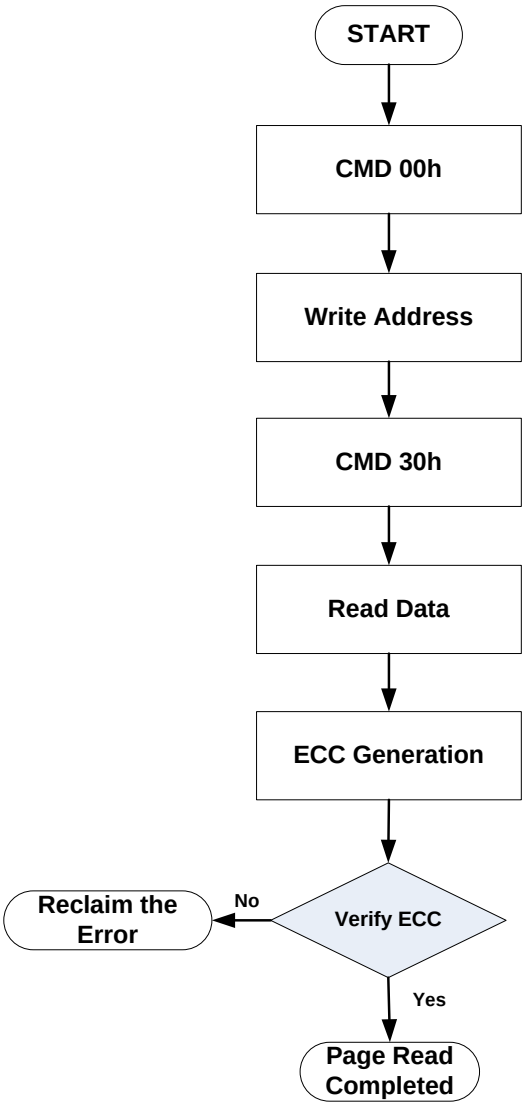
Program Flow Chart



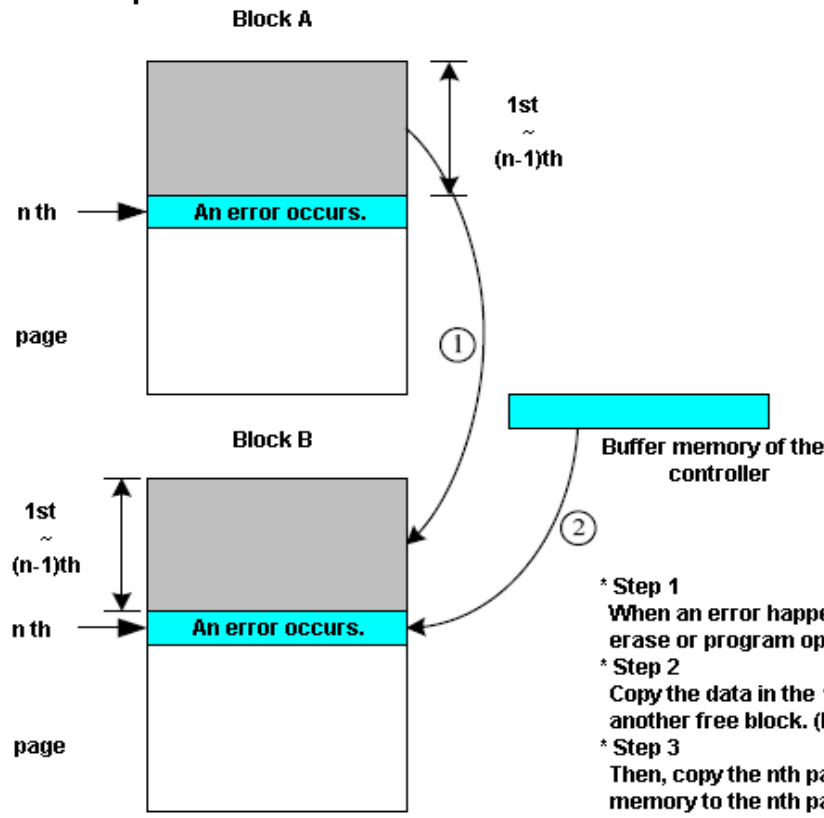
Erase Flow Chart



Read Flow Chart



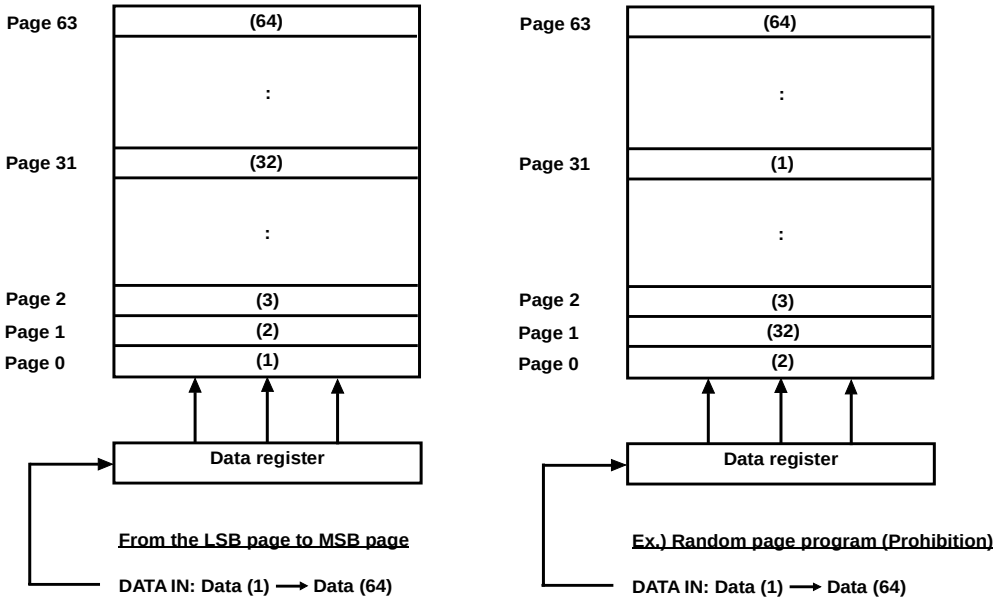
Block Replacement



* Step 1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step 2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step 3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
* Step 4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

Addressing for program operation

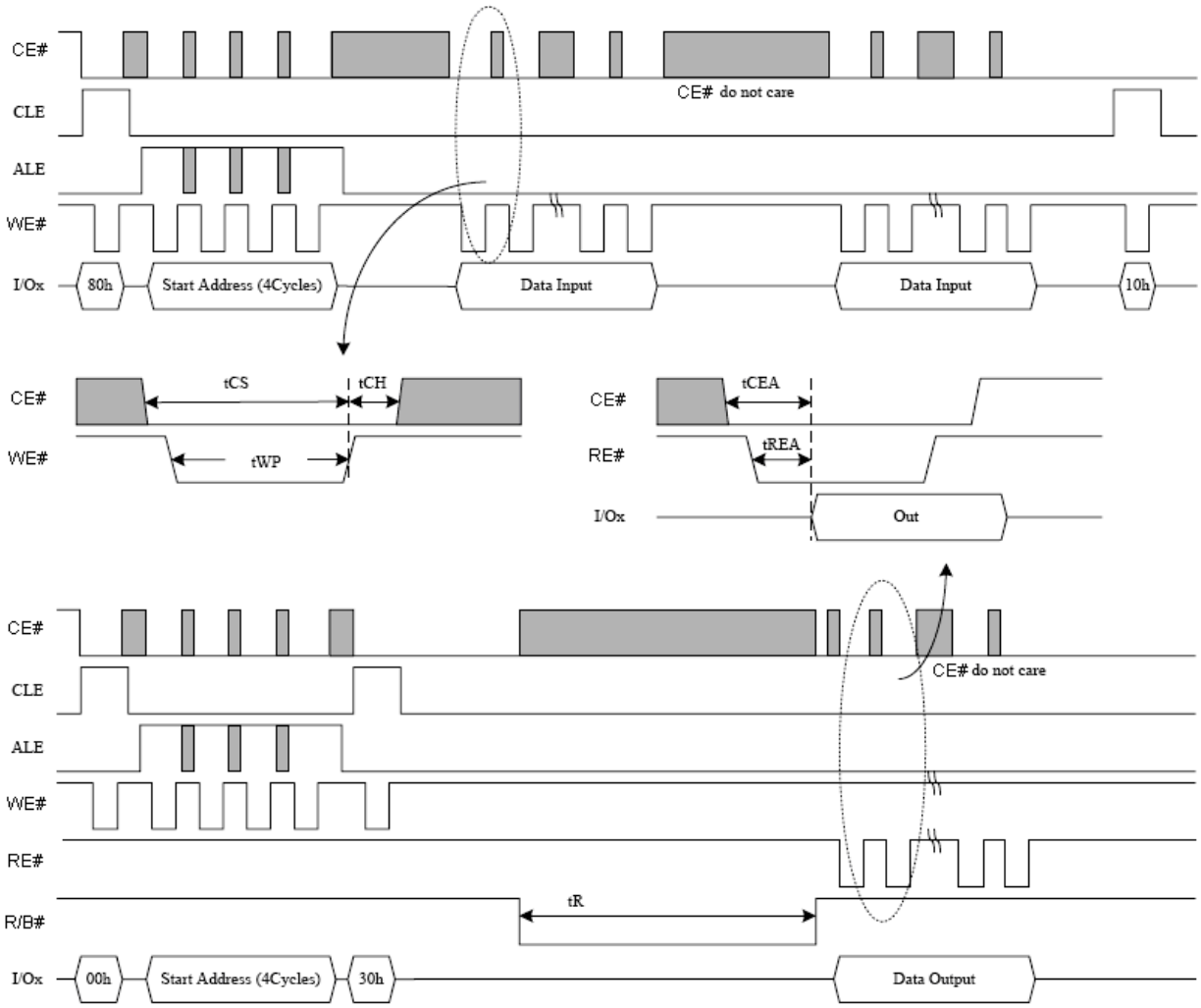
Within a block, the pages must be programmed consecutively from the LSB (Least Significant Bit) page of the block to MSB (Most Significant Bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.



System Interface Using CE# don't-care

For an easier system interface, CE# may be inactive during the data-loading or serial access as shown below. The internal 2,112 bytes page registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications that use slow cycle time on the order of u-seconds, de-activating CE# during the data-loading and serial access would provide significant savings in power consumption.

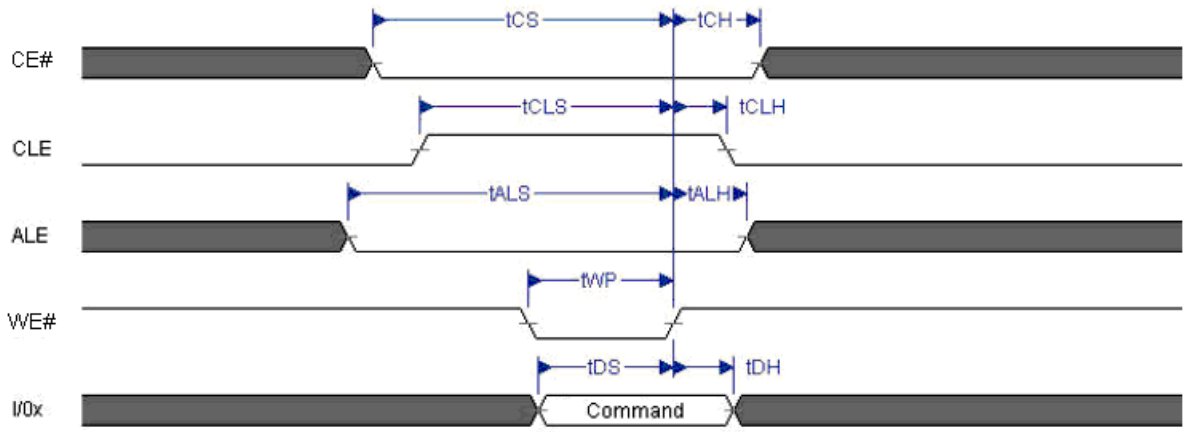
Program / Read Operation with "CE# not-care"



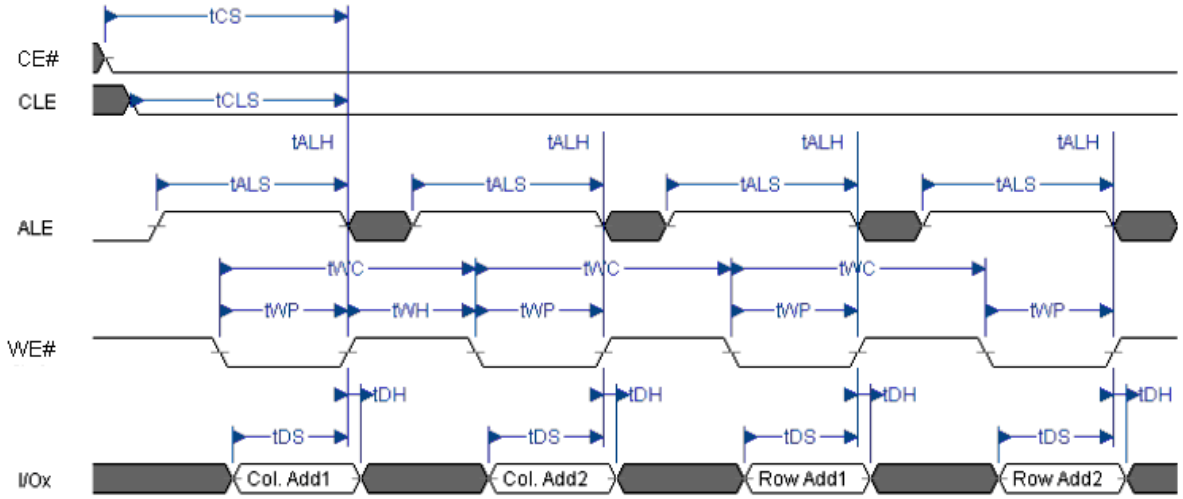
Address Information

DATA	I/O	ADDRESS			
Data In / Out	I/Ox	Col. Add1	Col. Add2	Row Add1	Row Add2
2,112 bytes	I/O0~ I/O7	A0 ~ A7	A8 ~ A11	A12 ~ A19	A20 ~ A27

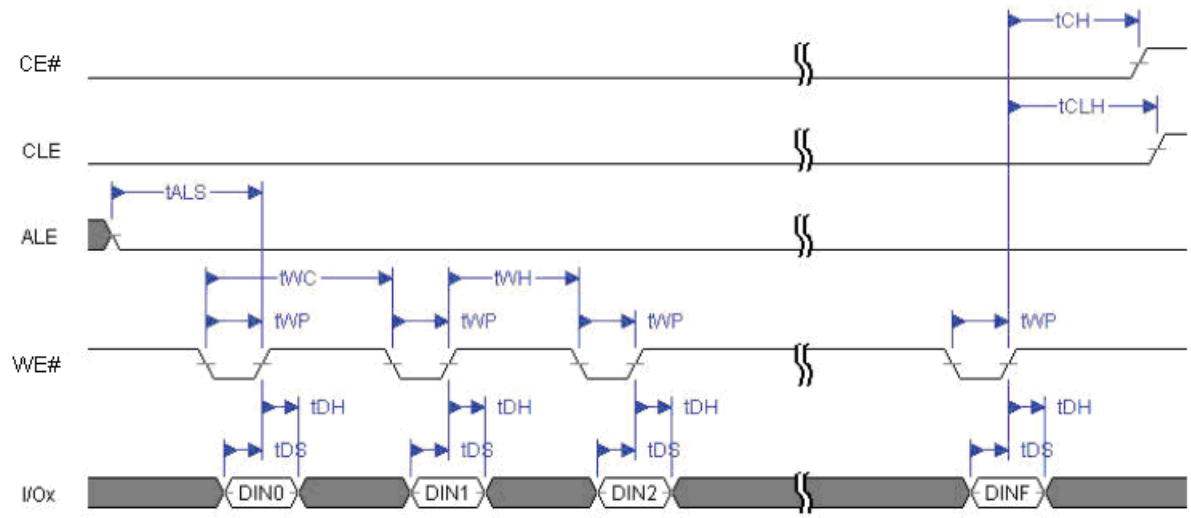
Command Latch Cycle



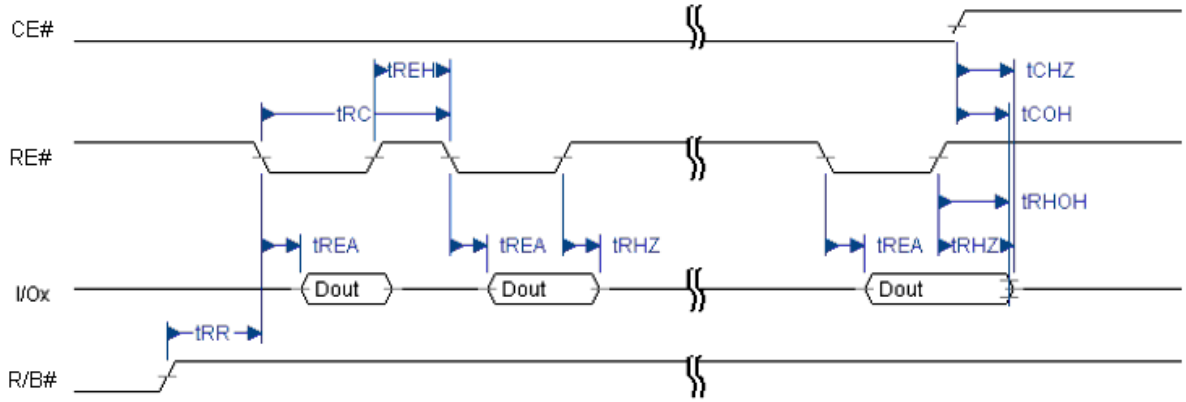
Address Latch Cycle



Input Data Latch Cycle

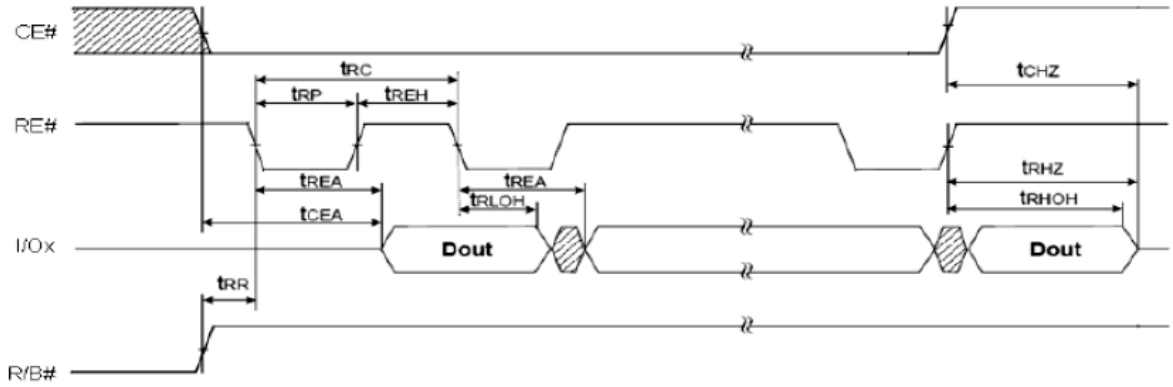


Serial access Cycle after Read (CLE = L, WE# = H, ALE = L)



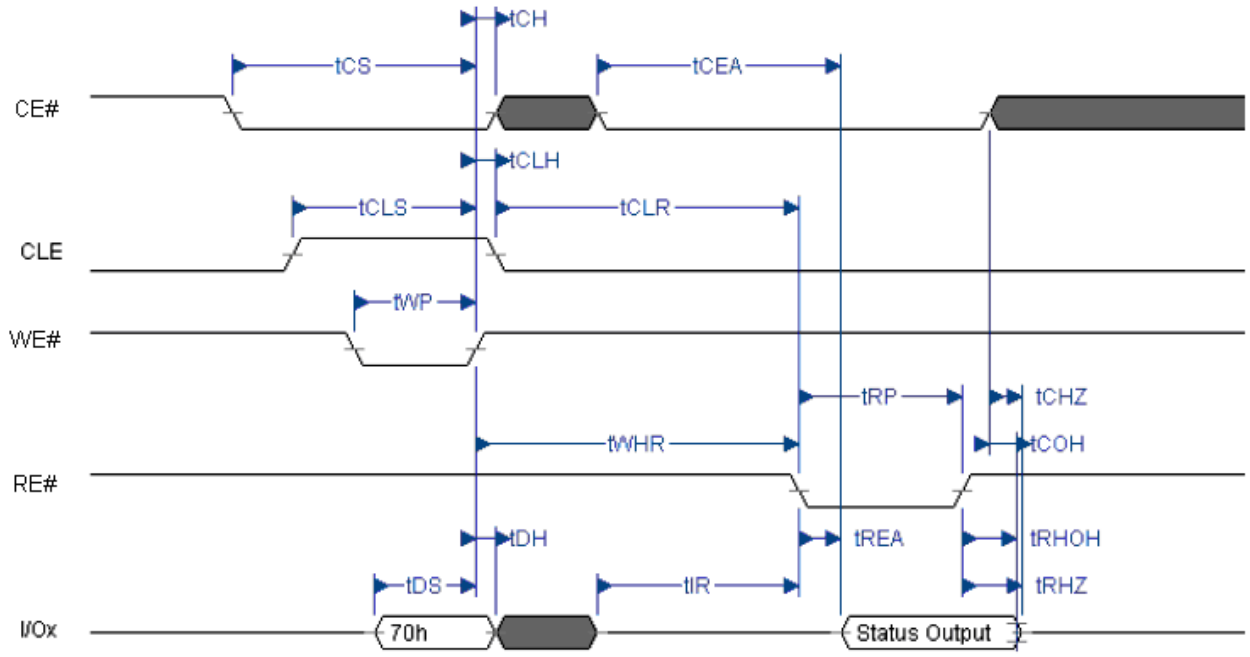
Note:
1. Dout transition is measured at ±200mV from steady state voltage at I/O with load.
2. t_{RHOH} starts to be valid when frequency is lower than 20MHz.

Serial access Cycle after Read (EDO Type CLE = L, WE# = H, ALE = L)

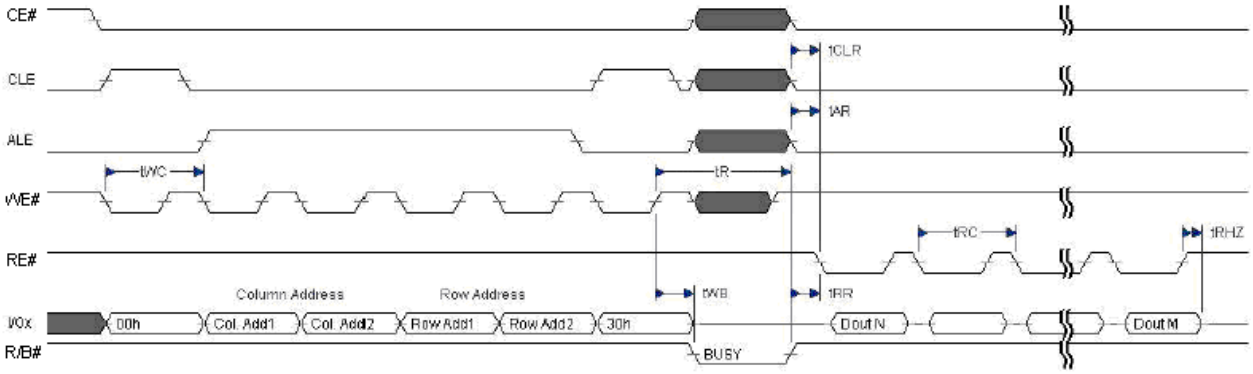


Note:
1. Transition is measured at ±200mV from steady state voltage with load.
2. This parameter is sampled and not 100% tested.
3. t_{RLOH} is valid when frequency is higher than 20MHz.
4. t_{RHOH} starts to be valid when frequency is lower than 20MHz.

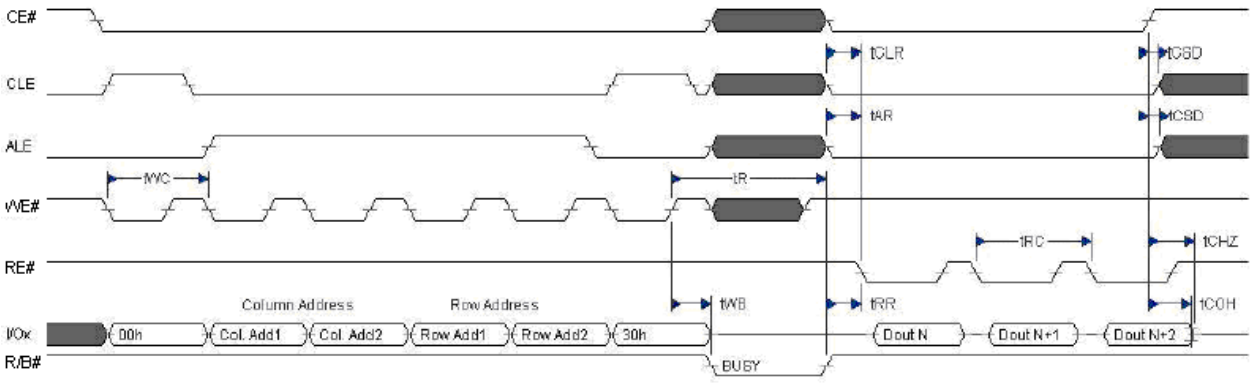
Status Read Cycle



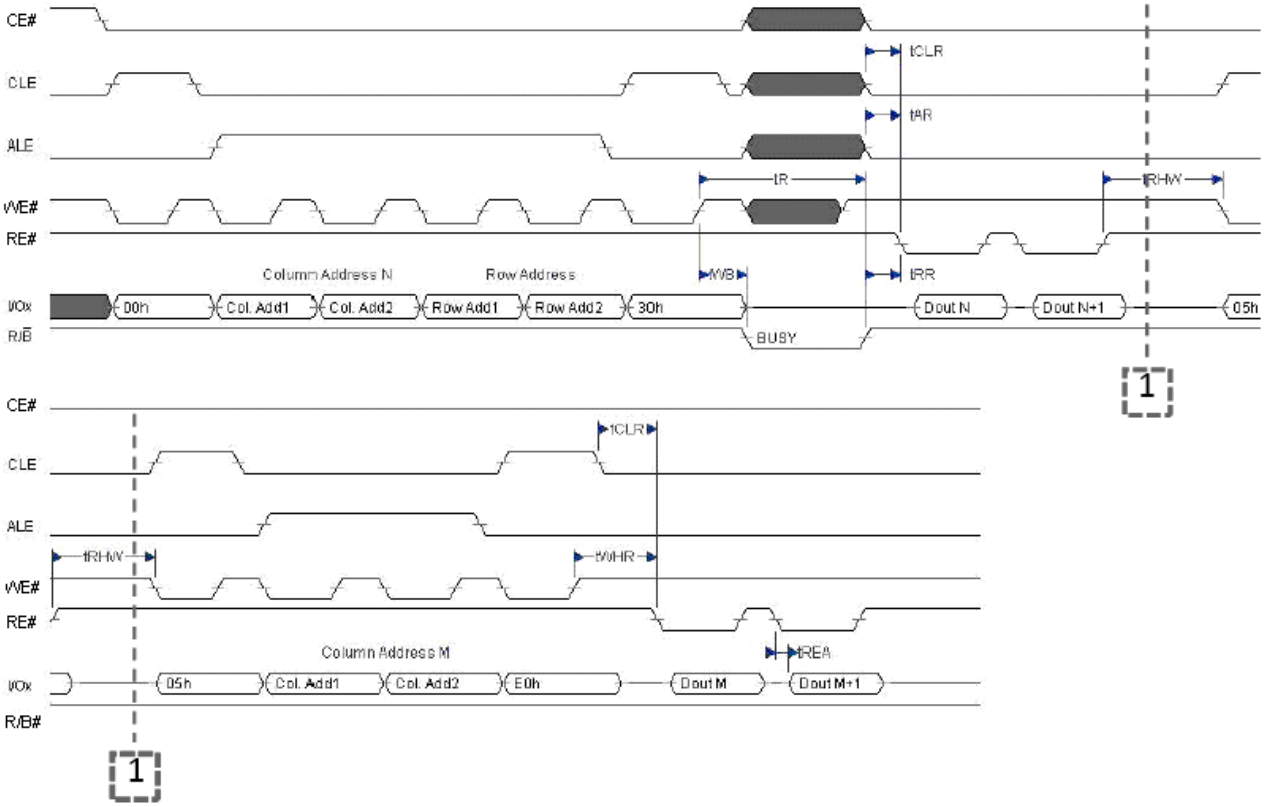
Read Operation



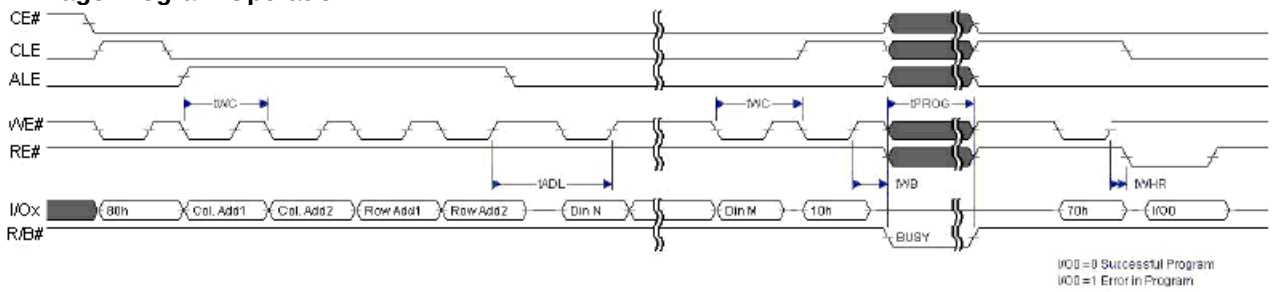
Read Operation (Intercepted by CE#)



Random Data Output In a Page

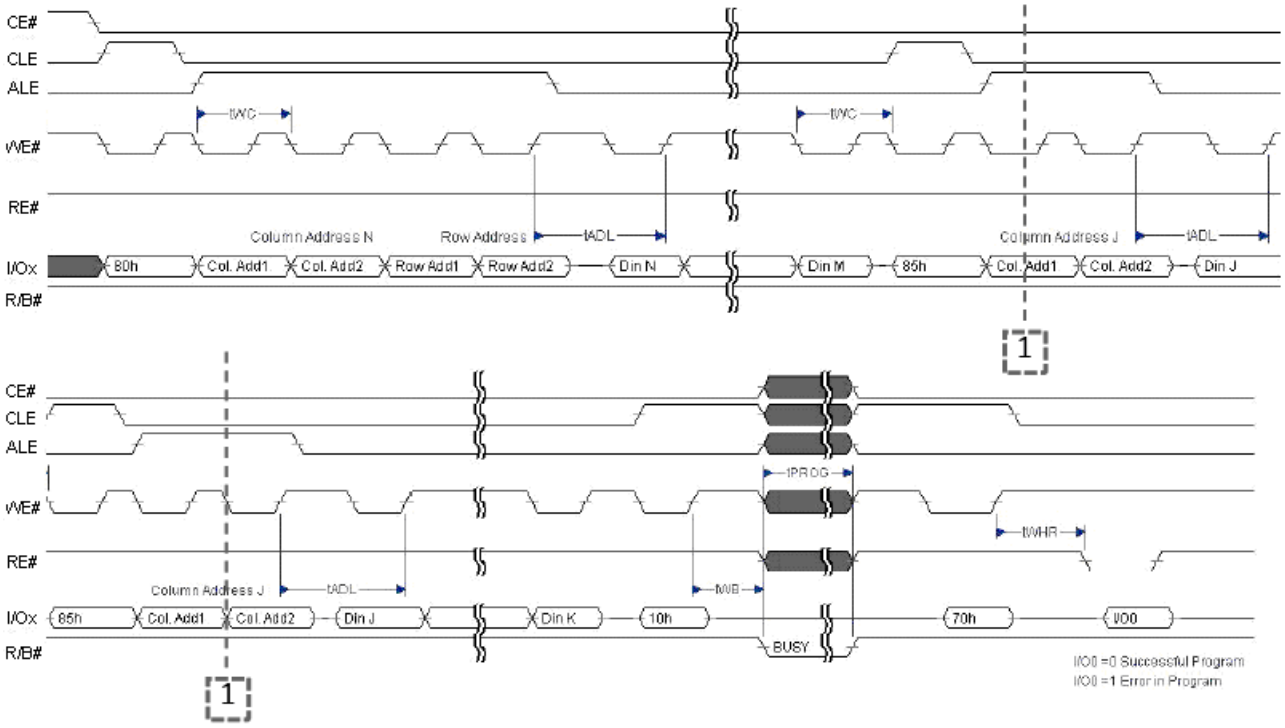


Page Program Operation



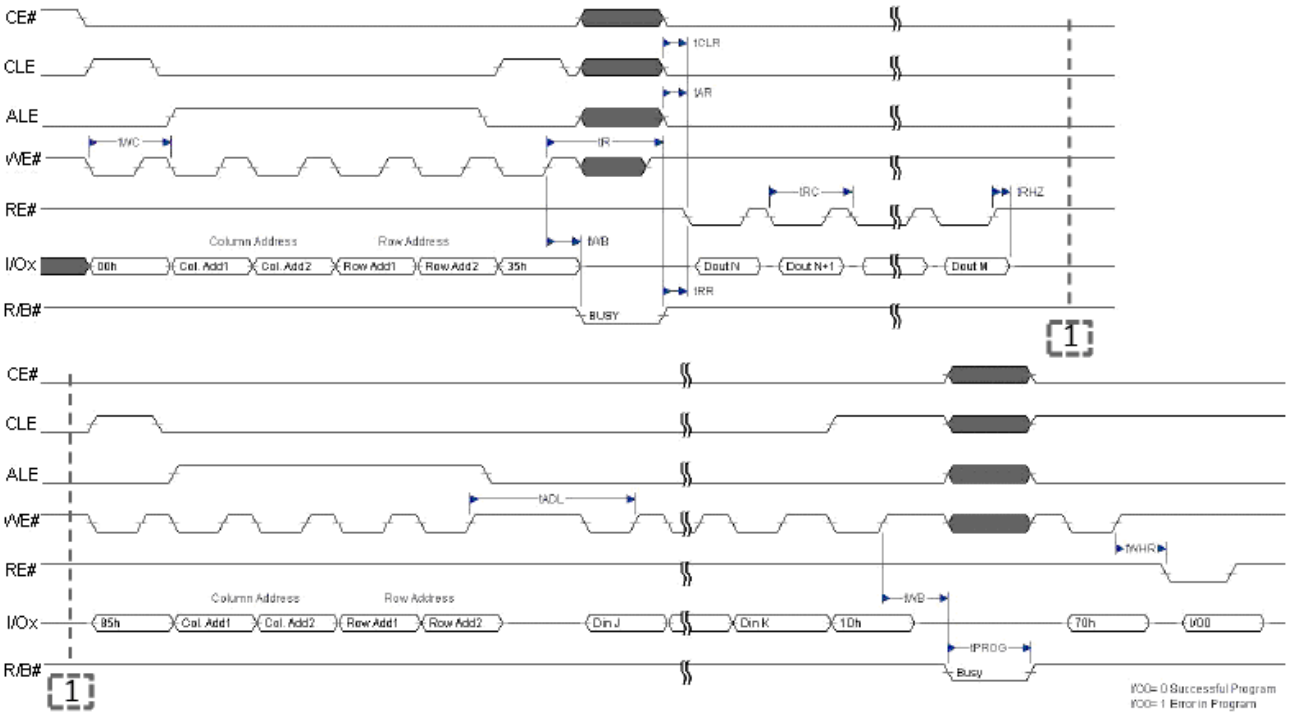
Note: t_{ADL} is the time from WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

Page Program Operation with Random Data Input

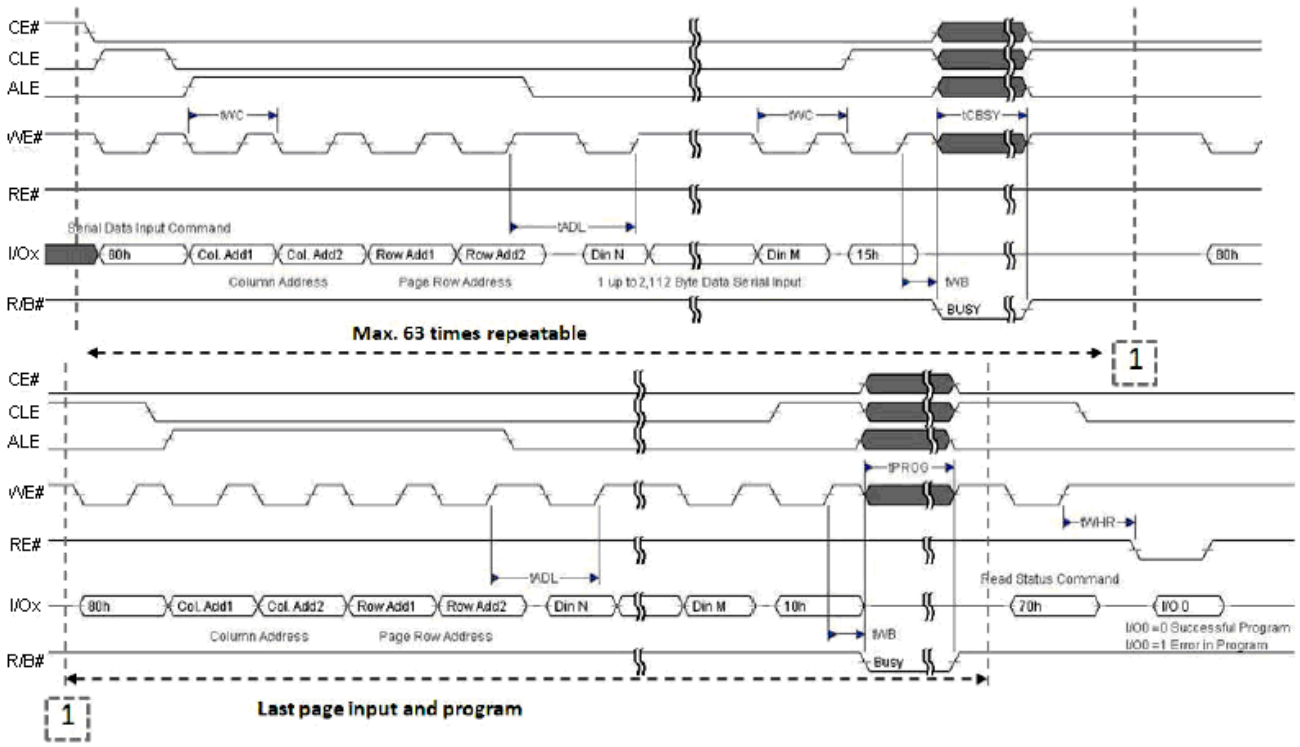


Note: t_{ADL} is the time from WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

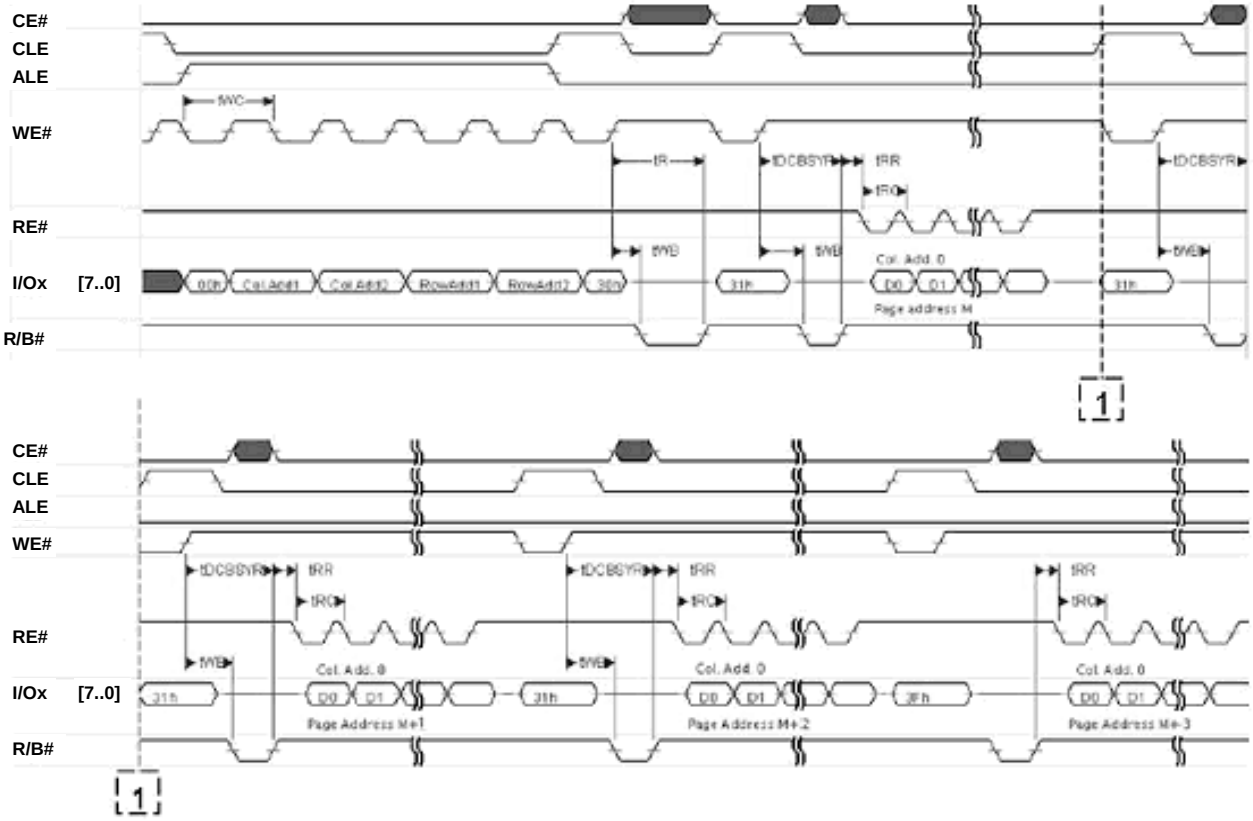
Copy-Back Program Operation with Random Data Input



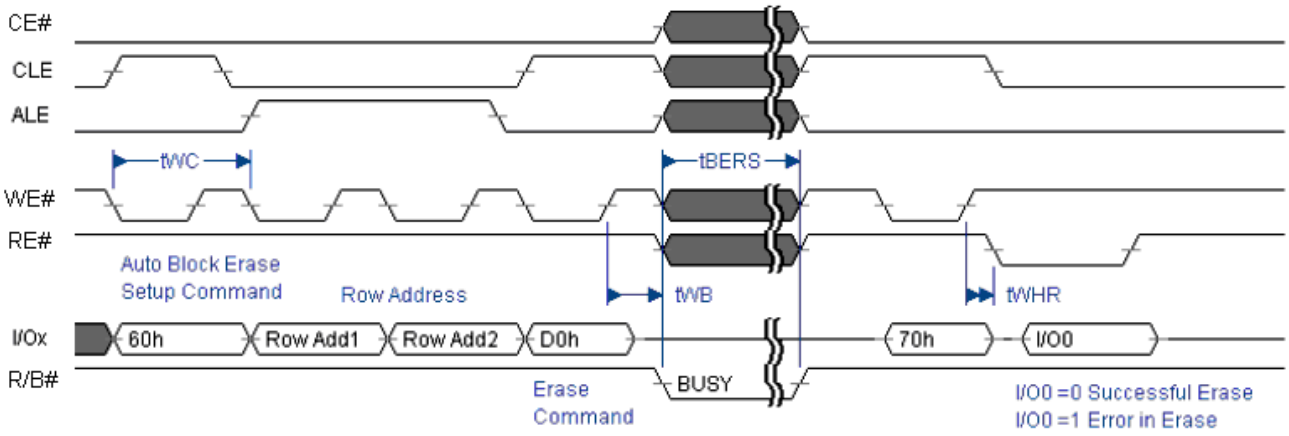
Cache Program Operation



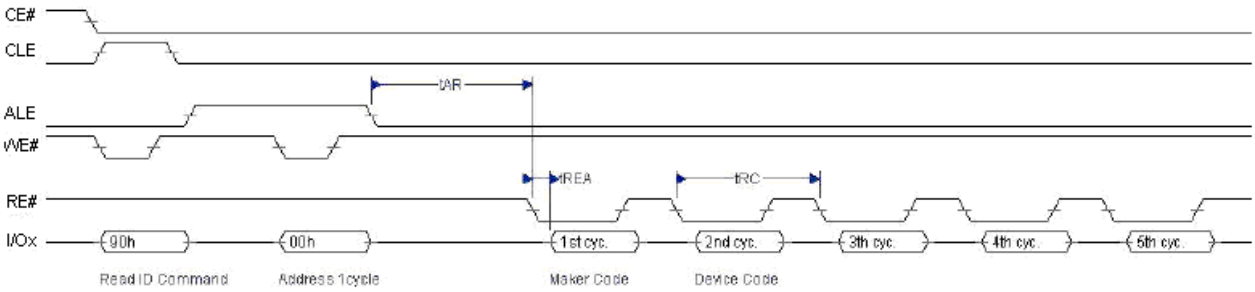
Cache Read Operation



Block Erase Operation



Read ID Operation



ID Definition Table

ID Access command = 90h

1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle
C8h	A1h	80h	15h	40h

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, etc.
4th Byte	Page Size, Block Size, Redundant Area Size, Organization, Serial Access Minimum.
5th Byte	Plane Number, Plane Size

3rd ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously Programmed Page	1 2 4 8			0 0 1 1	0 1 0 1				
Interleave Program Between multiple chips	Not Support Support		0 1						
Cache Program	Not Support Support	0 1							

4th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	1KB 2KB 4KB 8KB							0 0 1 1	0 1 0 1
Redundant Area Size (byte/512byte)	8 16						0 1		
Block Size (w/o redundant area)	64KB 128KB 256KB 512KB			0 0 1 1	0 1 0 1				
Organization	x8 x16		0 1						
Serial Access Minimum	45ns Reserved Reserved Reserved	0 0 1 1				0 1 0 1			

5th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
ECC Level	1 bit ECC/512Byte 2 bit ECC/512Byte 4 bit ECC/512Byte Reserved							0 0 1 1	0 1 0 1
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
Plane Size (w/o redundant area)	64Mb 128Mb 256Mb 512Mb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Reserved	Reserved	0							

DEVICE OPERATION

Page Read

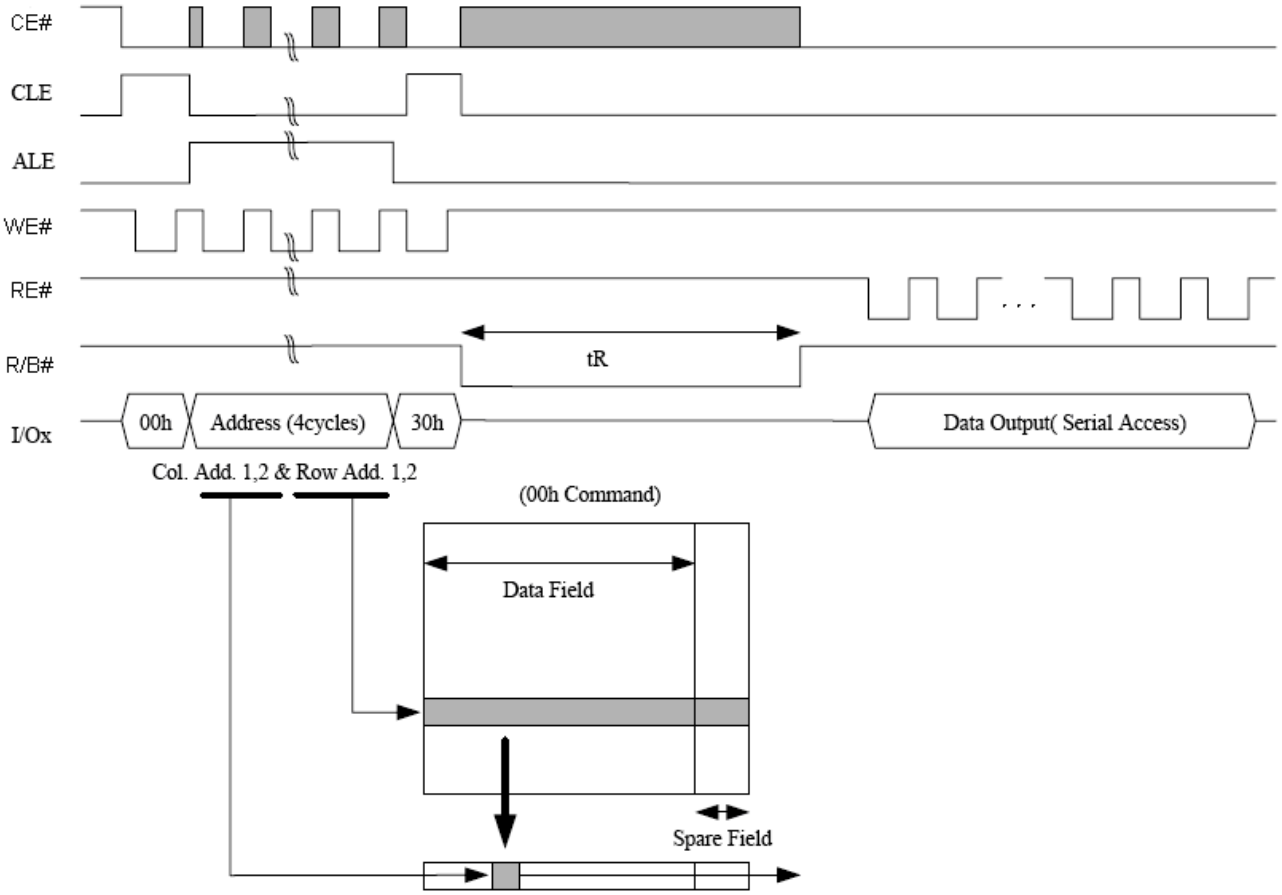
Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h command, four-cycle address, and 30h command. After initial power up, the 00h command can be skipped because it has been latched in the command register. The 2,112Byte of data on a page are transferred to cache registers via data registers within 25us (t_R). Host controller can detect the completion of this data transfer by checking the R/B# output. Once data in the selected page have been loaded into cache registers, each Byte can be read out in 45ns cycle time by continuously pulsing RE#. The repetitive high-to-low transitions of RE# clock signal make the device output data starting from the designated column address to the last column address.

The device can output data at a random column address instead of sequential column address by using the Random Data Output command. Random Data Output command can be executed multiple times in a page.

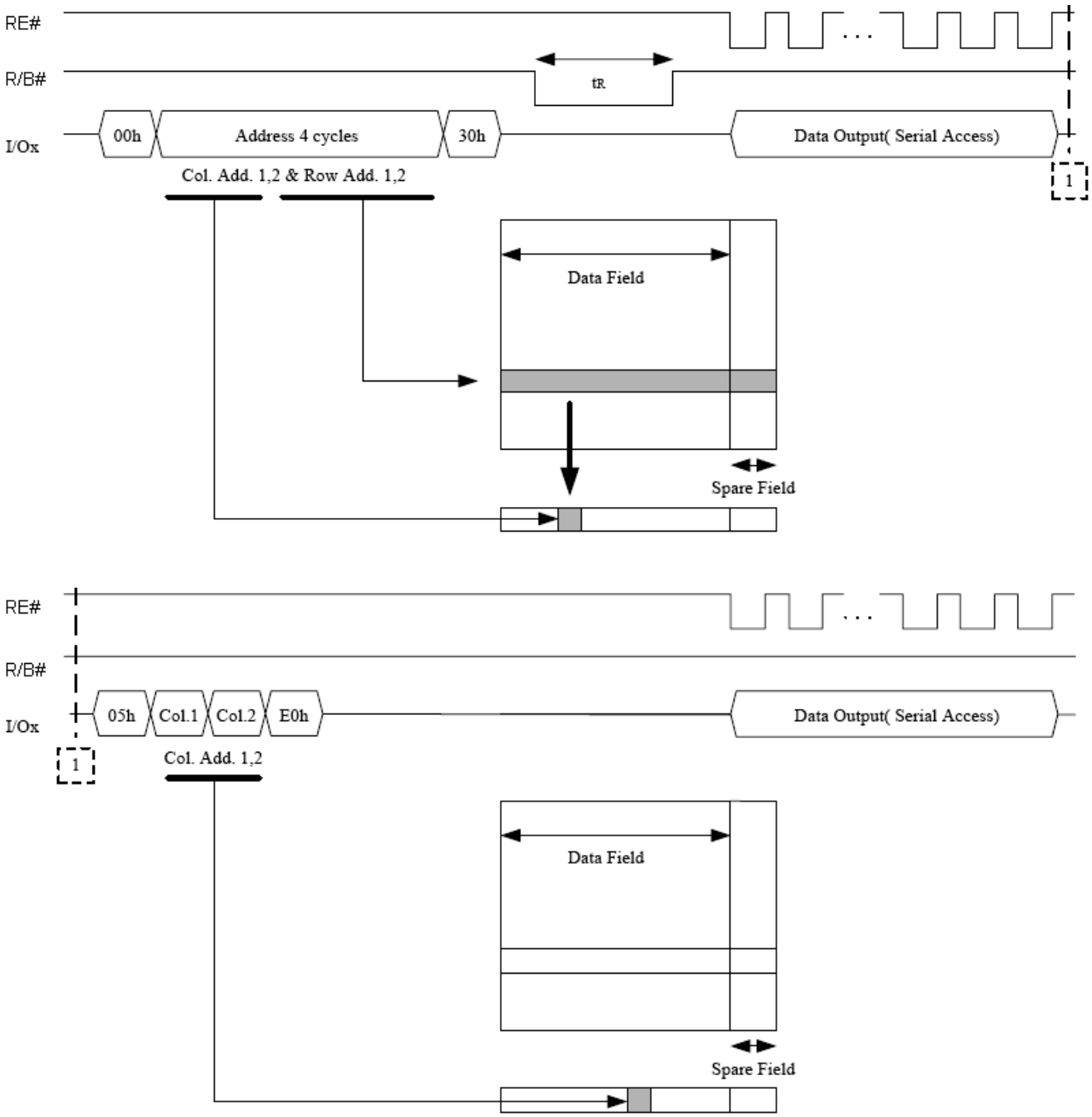
After power up, device is in read mode so 00h command cycle is not necessary to start a read operation.

A page read sequence is illustrated in under figure, where column address, page address are placed in between commands 00h and 30h. After t_R read time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 30h. Host controller can toggle RE# to access data starting with the designated column address and their successive bytes.

Read Operation



Random Data Output In a Page



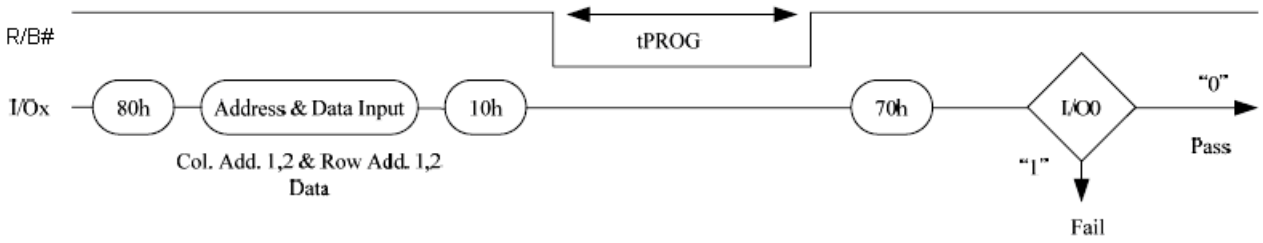
Page Program

The device is programmed based on the unit of a page, and consecutive partial page programming on one page without intervening erase operation is strictly prohibited. Addressing of page program operations within a block should be in sequential order. A complete page program cycle consists of a serial data input cycle in which up to 2,112 byte of data can be loaded into data register via cache register, followed by a programming period during which the loaded data are programmed into the designated memory cells.

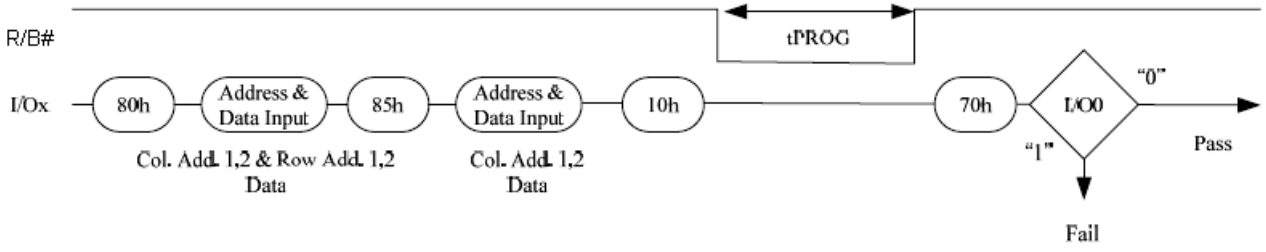
The serial data input cycle begins with the Serial Data Input command (80h), followed by a four-cycle address input and then serial data loading. The bytes not to be programmed on the page do not need to be loaded. The column address for the next data can be changed to the address follows Random Data Input command (85h). Random Data Input command may be repeated multiple times in a page. The Page Program Confirm command (10h) starts the programming process. Writing 10h alone without entering data will not initiate the programming process. The internal write engine automatically executes the corresponding algorithm and controls timing for programming and verification, thereby freeing the host controller for other tasks. Once the program process starts, the host controller can detect the completion of a program cycle by monitoring the R/B# output or reading the Status bit (I/O6) using the Read Status command. Only Read Status and Reset commands are valid during programming. When the Page Program operation is completed, the host controller can check the Status bit (I/O0) to see if the Page Program operation is successfully done. The command register remains the Read Status mode unless another valid command is written to it.

A page program sequence is illustrated in under figure, where column address, page address, and data input are placed in between 80h and 10h. After t_{PROG} program time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 10h.

Program & Read Status Operation



Random Data Input In a page

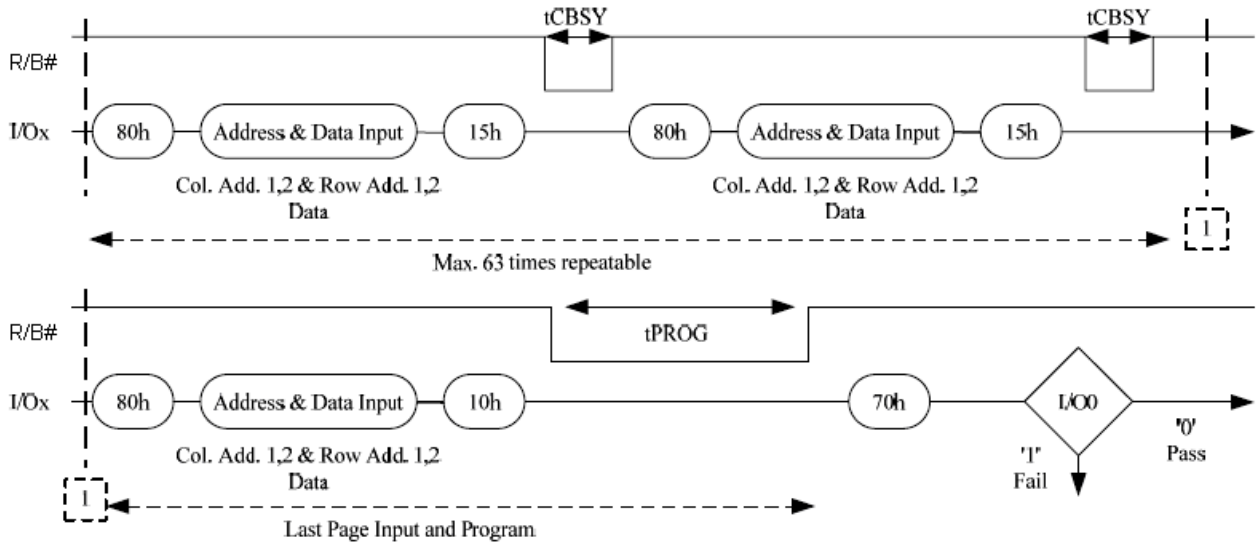


Cache Program

Cache Program is an extension of Page Program, which is executed with 2,112 byte data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell.

After writing the first set of data up to 2,112 bytes into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time (t_{CBSY}) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit (I/O6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command, t_{CBSY} is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit (I/O5) for internal Ready/Busy may be polled to identity the completion of internal programming. If the system monitors the progress of programming only with R/B#, the last page of the target programming sequence must be programmed with actual Page Program command (10h).

Cache Program (available only within a block)



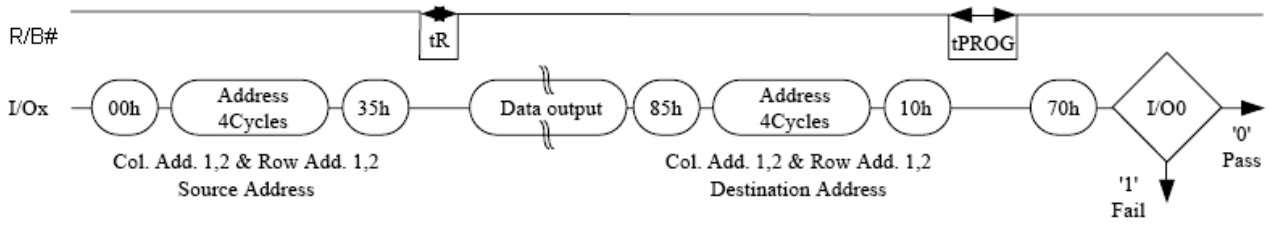
Note:

1. Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.
2. t_{PROG} = Program time for the last page + Program time for the (last-1)th page – (Program command cycle time + Last page data loading time)

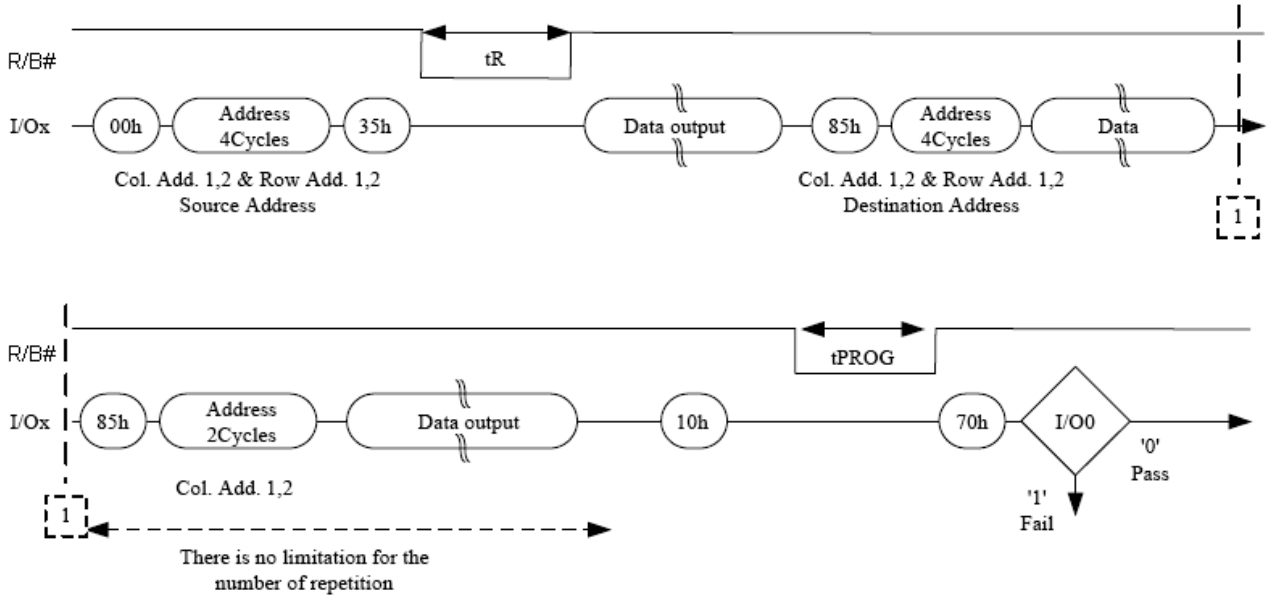
Copy-Back Program

Copy-Back Program is designed to efficiently copy data stored in memory cells without time-consuming data reloading when there is no bit error detected in the stored data. The benefit is particularly obvious when a portion of a block is updated and the rest of the block needs to be copied to a newly assigned empty block. Copy-Back operation is a sequential execution of Read for Copy-Back and of Copy-Back Program with Destination address. A Read for Copy-Back operation with “35h” command and the Source address moves the whole 2,112byte data into the internal buffer. The host controller can detect bit errors by sequentially reading the data output. Copy-Back Program is initiated by issuing Page-Copy Data-Input command (85h) with Destination address. If data modification is necessary to correct bit errors and to avoid error propagation, data can be reloaded after the Destination address. Data modification can be repeated multiple times as shown in under figure. Actual programming operation begins when Program Confirm command (10h) is issued. Once the program process starts, the Read Status command (70h) may be entered to read the status register. The host controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. When the Copy-Back Program is complete, the Status Bit (I/O0) may be checked. The command register remains Read Status mode until another valid command is written to it.

Page Copy-Back Program Operation



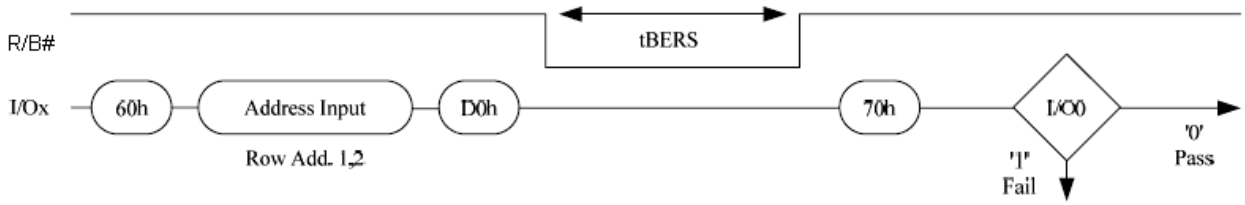
Page Copy-Back Program Operation with Random Data Input



Block Erase

The block-based Erase operation is initiated by an Erase Setup command (60h), followed by a two-cycle row address, in which only Plane address and Block address are valid while Page address is ignored. The Erase Confirm command (D0h) following the row address starts the internal erasing process. The two-step command sequence is designed to prevent memory content from being inadvertently changed by external noise. At the rising edge of WE# after the Erase Confirm command input, the internal control logic handles erase and erase-verify. When the erase operation is completed, the host controller can check Status bit (I/O0) to see if the erase operation is successfully done. The under figure illustrates a block erase sequence, and the address input (the first page address of the selected block) is placed in between commands 60h and D0h. After t_{BERASE} erase time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after D0h to check the execution status of erase operation.

Block Erase Operation



Read Status

A status register on the device is used to check whether program or erase operation is completed and whether the operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the status register to I/O pins on the falling edge of CE# or RE#, whichever occurs last. These two commands allow the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to toggle for status change.

The command register remains in Read Status mode unless other commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h) is needed to start read cycles.

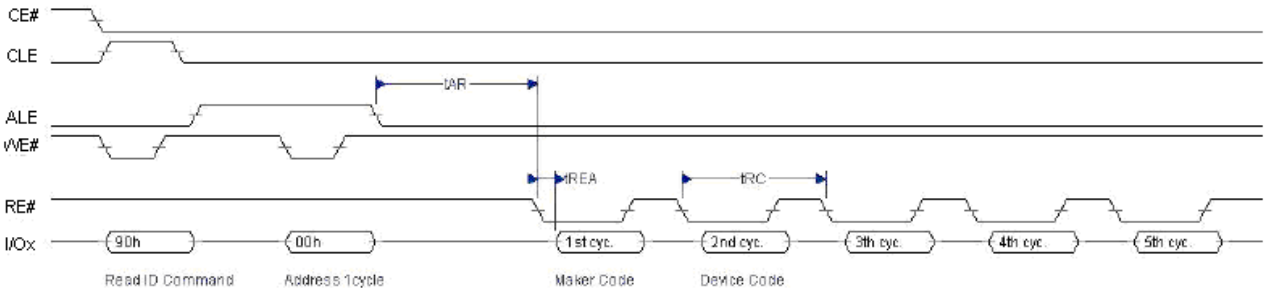
Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Read	Cache Read	Definition
I/O0	Pass / Fail	Pass / Fail	NA	NA	Pass: 0 Fail: 1
I/O1	NA	NA	NA	NA	Don't cared
I/O2	NA	NA	NA	NA	Don't cared
I/O3	NA	NA	NA	NA	Don't cared
I/O4	NA	NA	NA	NA	Don't cared
I/O5	NA	NA	NA	True Ready / Busy	Busy: 0 Ready: 1
I/O6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Busy: 0 Ready: 1
I/O7	Write Protect	Write Protect	Write Protect	Write Protect	Protected: 0 Not Protected: 1

Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacturer code (C8h), and the device code and 3rd, 4th and 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.

Read ID Operation



ID Definition Table

Maker Code	Device Code	3rd Cycle	4th Cycle	5th Cycle
C8h	A1h	80h	15h	40h

Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy State during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP# is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B# pin changes to low for t_{RST} after the Reset command is written. Refer to Figure below.

Reset Operation

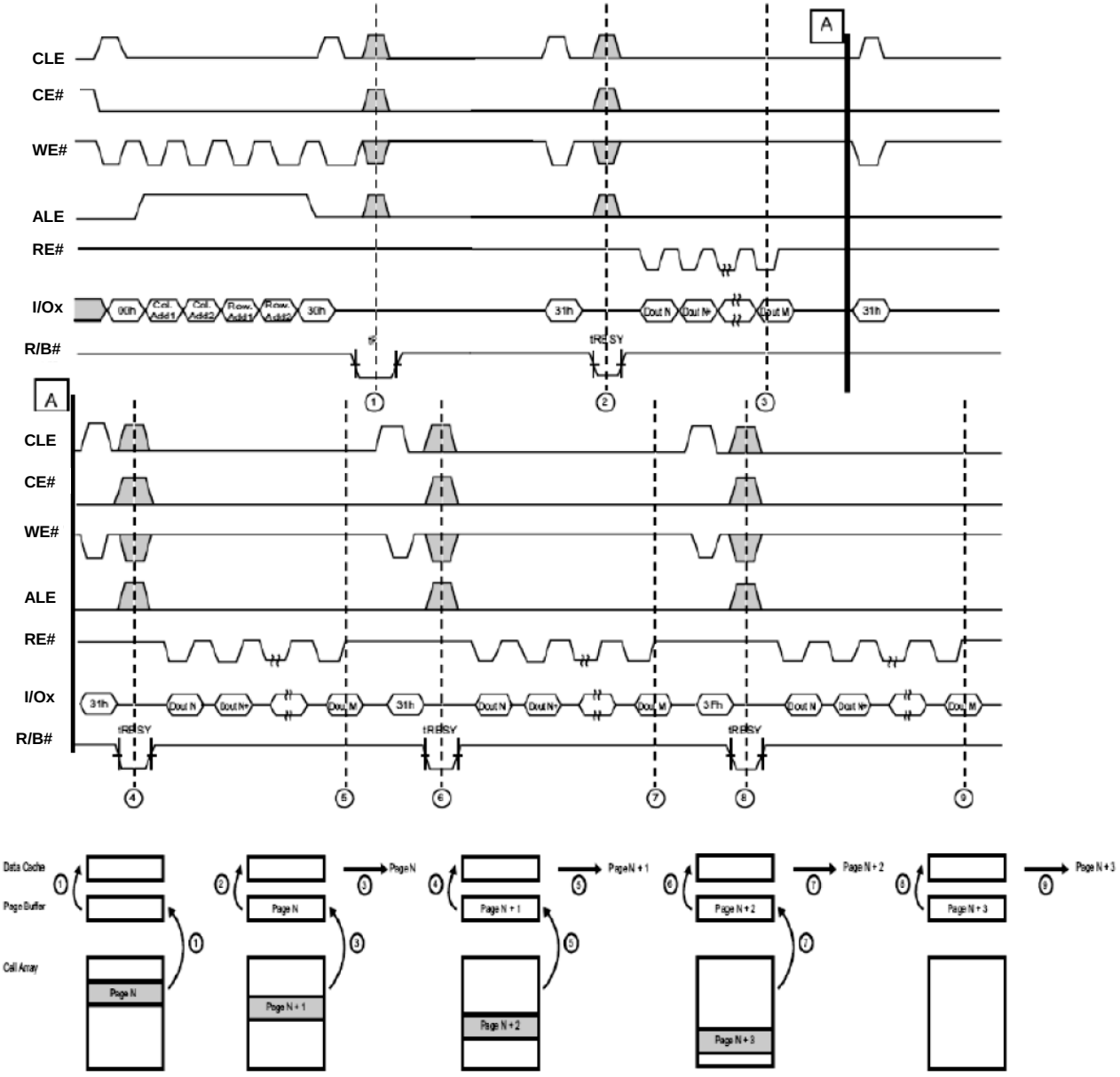
Device Status Table

	After Power-up	After Reset
Operation mode	00h Command is latched	Waiting for next command

Cache Read

Cache Read is an extension of Page Read, and is available only within a block. The normal Page Read command (00h-30h) is always issued before invoking Cache Read. After issuing the Cache Read command (31h), read data of the designated page (page N) are transferred from data registers to cache registers in a short time period of t_{DCBSYR}, and then data of the next page (page N+1) is transferred to data registers while the data in the cache registers are being read out. Host controller can retrieve continuous data and achieve fast read performance by iterating Cache Read operation. The Read Start for Last Page Cache Read command (3Fh) is used to complete data transfer from memory cells to data registers.

Read Operation with Cache Read



Ready/Busy#

The device has an R/B# output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B# pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tr (R/B#) and current drain during busy (ibusy), an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.

Ready/ Busy# Pin Electrical Specifications

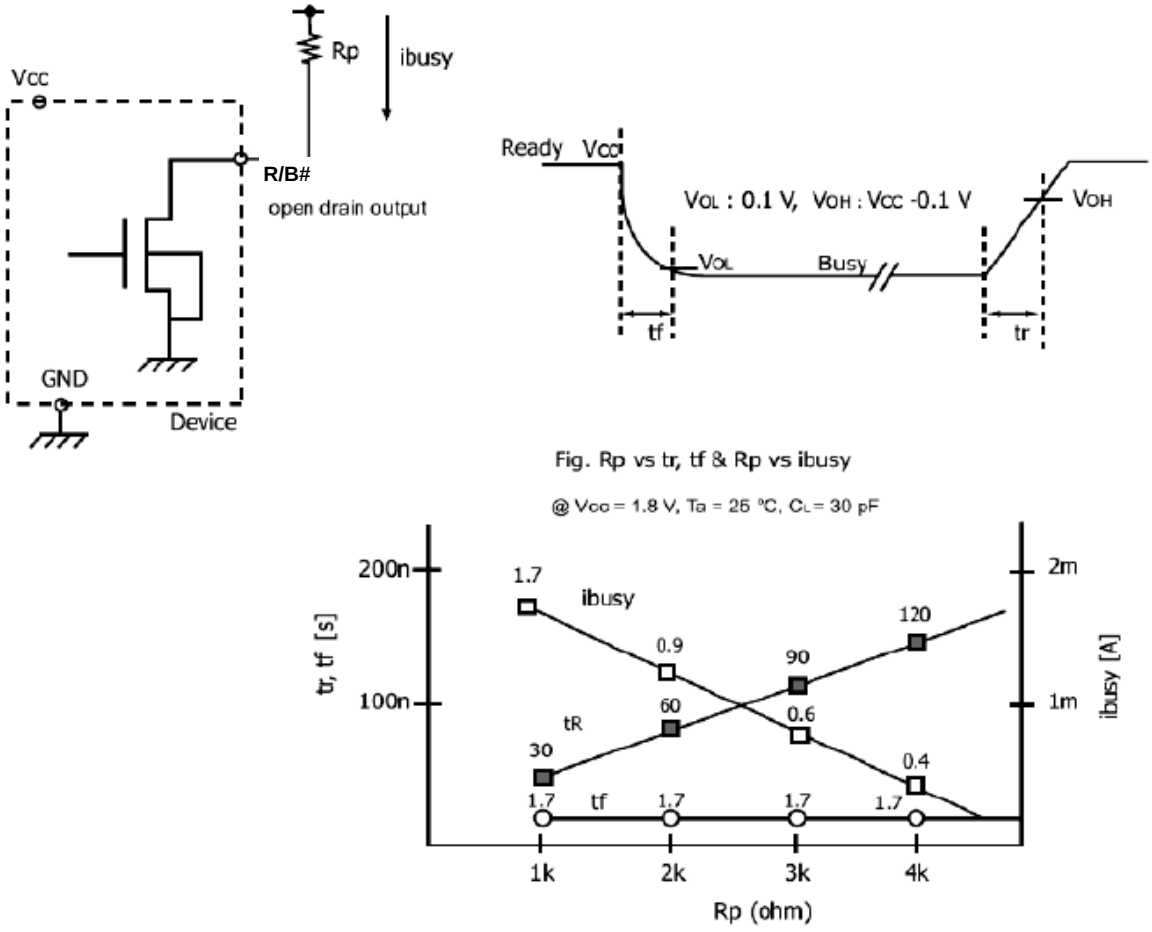


Fig. Rp vs tr, tf & Rp vs ibusy

@ Vcc = 1.8 V, Ta = 25 °C, CL = 30 pF

R_P value guidance

$$\text{Rp (min)} = \frac{V_{CC}(\text{Max.}) - V_{OL}(\text{Max.})}{I_{OL} + \Sigma I_L} = \frac{1.85V}{3\ mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/ B# pin.
R_P (max) is determined by maximum permissible limit of tr

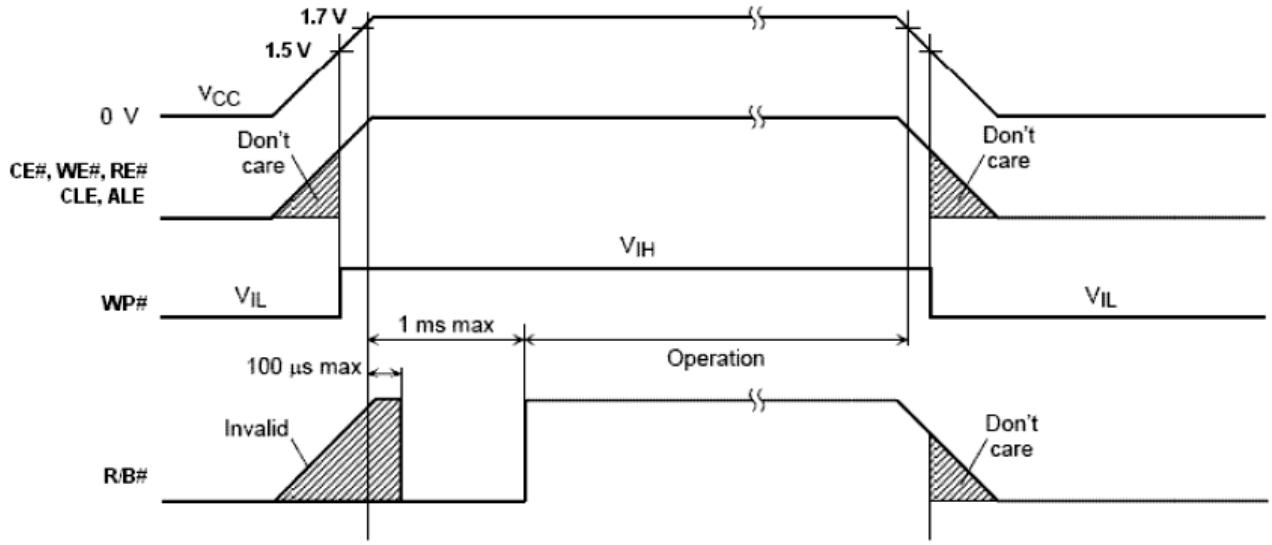
Data Protection & Power-up sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device R/B# signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are 70h.

The WP# signal is useful for protecting against data corruption at power on/off.

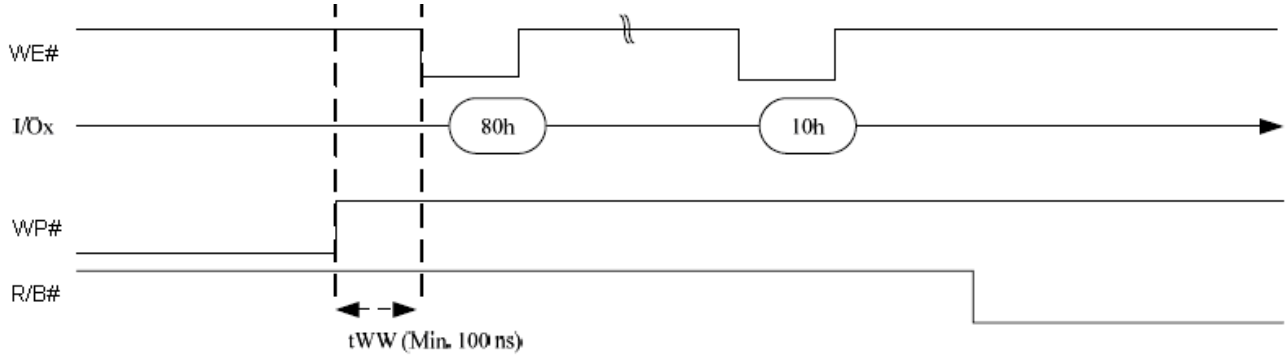
AC Waveforms for Power Transition



Write Protect Operation

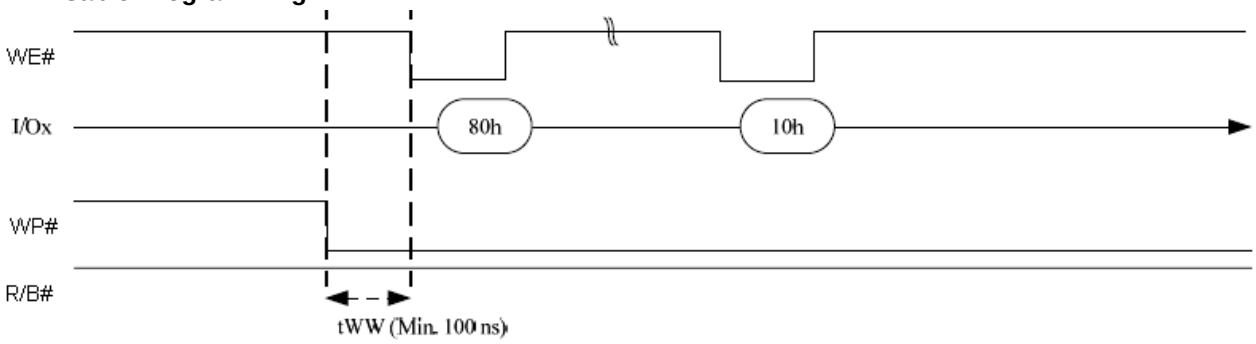
Enabling WP# during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

Enable Programming:

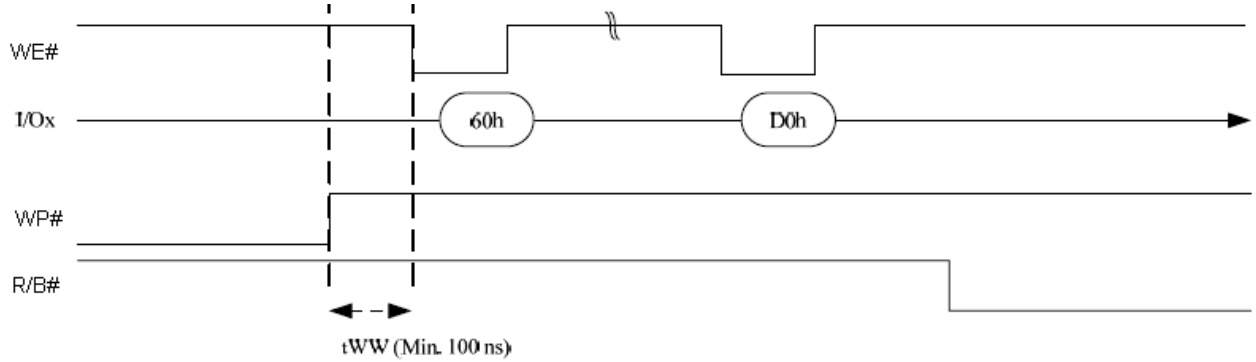


NOTE: WP# keeps "High" until programming finish.

Disable Programming:

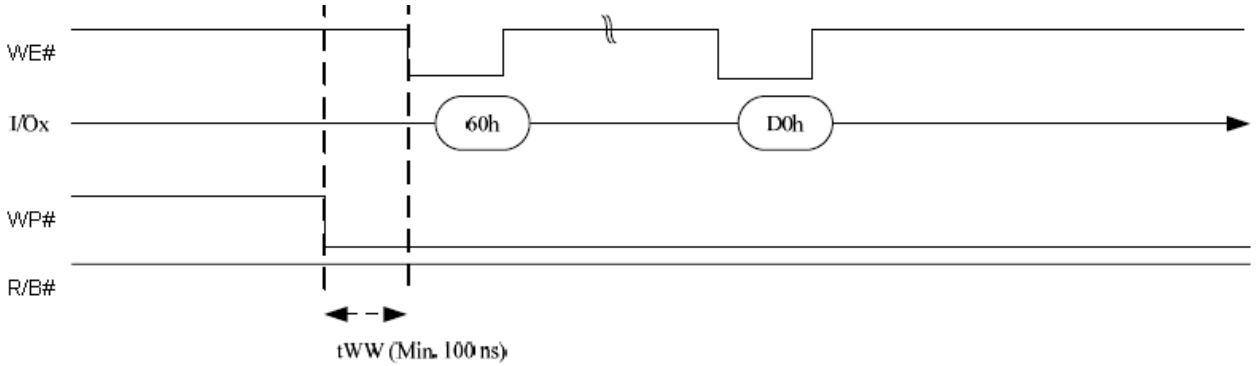


Enable Erasing:



NOTE: WP keeps “High” until erasing finish.

Disable Erasing:



One-Time Programmable (OTP) Operations

This flash device offers one-time programmable memory area. Thirty full pages of OTP data are available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands.

The OTP area leaves the factory in an unwritten state. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area.

The OTP area is only accessible while in OTP operation mode. To set the device to OTP operation mode, issue the Set Feature (EFh-90h-01h) command. When the device is in OTP operation mode, subsequent Read and/or Page Program are applied to the OTP area. When you want to come back to normal operation, you need to use EFh-90h-00h for OTP mode release. Otherwise, device will stay in OTP mode.

To program an OTP page, issue the Serial Data Input (80h) command followed by 4 address cycles. The first two address cycles are column address. For the third cycle, select a page in the range of 00h through 1Dh. The fourth cycle is fixed at 00h. Next, up to 2,112 bytes of data can be loaded into data register. The bytes other than those to be programmed do not need to be loaded. This device supports Random Data Input (85h) command, which can be operated multiple times in a page. The column address for the next data to be entered may be changed to the address follows the Random Data Input command. The Page Program confirm (10h) command initiates the programming process. The internal control logic automatically executes the programming algorithm, timing and verification. Please note that no partial-page program is allowed in the OTP area. In addition, the OTP pages must be programmed in the ascending order. A programmed OTP page will be automatically protected.

Similarly, to read data from an OTP page, set the device to OTP operation mode and then issue the Read (00h-30h) command. The device may output random data (not in sequential order) in a page by writing Random Data Output (05h-E0h) command, which can be operated multiple times in a page. The column address for the next data to be output may be changed to the address follows the Random Data Output command.

All pages in the OTP area will be protected simultaneously by issuing the Set Feature (EFh-90h-03h) command to set the device to OTP protection mode. After the OTP area is protected, no page in the area is programmable and the whole area cannot be unprotected.

The Read Status (70h) command is the only valid command for reading status in OTP operation mode.

OTP Modes and Commands

	Set feature		Command
OTP Operation mode	Read	EFh-90h-01h	00h-30h
	Page Program	EFh-90h-01h	80h-10h
OTP Protection mode	Program Protect	EFh-90h-03h	80h-10h
OTP Release mode	Leave OTP mode	EFh-90h-00h	

OTP Area Details

Description	Value
Number of OTP pages	30
OTP page address	01h – 1Eh
Number of partial page programs for each page in the OTP area	1

Mobile DDR SDRAM Memory Operations

Electrical Specifications

- All voltages are referenced to VSS (GND).
- After power-up, wait more than 200 µs and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 ~ 2.3	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.5 ~ 2.3	V
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.5 ~ 2.3	V
Short circuit output current	I_{OS}	50	mA
Power dissipation	P_D	1.0	W
Operating ambient temperature	T_A	-25 ~ +85	°C
Storage temperature (plastic)	T_{STG}	-55 ~ +125	°C

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions

Recommended operating conditions unless otherwise noted, V_{DD} / V_{DDQ} = 1.7~1.95V

Parameter	Pins	Symbol	Min	Typ.	Max	Unit	Note
Supply voltage		V_{DD} / V_{DDQ}	1.7	1.8	1.95	V	1
		V_{SS} / V_{SSQ}	0	0	0	V	
Input high voltage	All other input pins	V_{IH}	0.8 x V_{DDQ}	-	V_{DDQ} + 0.3	V	
Input low voltage		V_{IL}	-0.3	-	0.2 x V_{DDQ}	V	
DC input voltage	CLK, CLK#	V_{IN}	-0.3	-	V_{DDQ} + 0.3	V	
DC input differential voltage		V_{ID} (DC)	0.4 x V_{DDQ}		V_{DDQ} + 0.6	V	5
AC input differential voltage		V_{ID} (AC)	0.6 x V_{DDQ}		V_{DDQ} + 0.6	V	5
AC input differential cross point voltage		V_{IX} (AC)	0.4 x V_{DDQ}	0.5 x V_{DDQ}	0.6 x V_{DDQ}	V	6
DC input high voltage	DQ, DM, DQS	V_{IHD} (DC)	0.7 x V_{DDQ}		V_{DDQ} + 0.3	V	
DC input low voltage		V_{ILD} (DC)	-0.3		0.3 x V_{DDQ}	V	
AC input high voltage		V_{IHD} (AC)	0.8 x V_{DDQ}		V_{DDQ} + 0.3	V	
AC input low voltage		V_{ILD} (AC)	-0.3		0.2 x V_{DDQ}	V	

Note:
1. VDDQ must be equal to VDD.
2. VIH (max.) = 2.3V (pulse width ≤ 5ns).
3. VIL (min.) = -0.5V (pulse width ≤ 5ns).
4. All voltage referred to VSS and VSSQ must be same potential.
5. VID (DC) and VID (AC) are the magnitude of the difference between the input level on CLK and the input level on CLK#.
6. The value of VIX is expected to be 0.5 x VDDQ and must track variations in the DC level of the same.

DC Characteristics 1

Recommended operating conditions unless otherwise noted, V_{DD} / V_{DDQ} = 1.7~1.95

Parameter	Symbol	Max.	Unit	Test Condition	Note
Operating Current (ACT-PRE)	I_{DD0}	85	mA	One bank active-prechange, t_{RC}= t_{RC} (min); t_{CK} = t_{CK} (min); CKE = HIGH; CS# = HIGH between valid commands; address inputs are SWITCHING; data input signals are STABLE	
Standby Current in power-down mode	I_{DD2P}	0.8	mA	All banks idle, CKE = LOW; CS# = HIGH, t_{CK} = t_{CK} (min); address & control inputs are SWITCHING; data input signals are STABLE	
Standby Current in power-down mode	I_{DD2PS}	0.6	mA	All banks idle, CKE = LOW; CS# = HIGH, CLK = LOW, CLK# = HIGH; address & control inputs are SWITCHING; data input signals are STABLE	
Standby Current in non power-down mode	I_{DD2N}	7	mA	All banks idle, CKE = HIGH; CS# = HIGH, t_{CK} = t_{CK} (min); address & control inputs are SWITCHING; data input signals are STABLE	
	I_{DD2NS}	2	mA	All banks idle, CKE = HIGH; CS# = HIGH, CLK = LOW, CLK# = HIGH; address & control inputs are SWITCHING; data input signals are STABLE	
Active Standby Current in power-down mode	I_{DD3P}	3	mA	One bank active, CKE = LOW; CS# = HIGH, t_{CK} = t_{CK} (min); address & control inputs are SWITCHING; data input signals are STABLE	
Active Standby Current in power-down mode with clock stop	I_{DD3PS}	2	mA	One bank active, CKE = LOW; CS# = HIGH, CLK = LOW, CLK# = HIGH; address & control inputs are SWITCHING; data input signals are STABLE	
Active Standby Current in non power-down mode	I_{DD3N}	10	mA	One bank active, CKE = HIGH, CS# = HIGH, t_{CK} = t_{CK} (min); address & control inputs are SWITCHING; data input signals are STABLE	
Active Standby Current in non power-down mode with clock stop	I_{DD3NS}	7	mA	One bank active, CKE = HIGH; CS# = HIGH, CLK= LOW, CLK# = HIGH; address & control inputs are SWITCHING; data input signals are STABLE	
Operating Current (Burst Mode)	I_{DD4}	135	mA	One bank active; BL=4; CL=3; t_{CK} = t_{CK} (min); continuous read bursts; I_{OUT} = 0 mA; address inputs are SWITCHING; 50% data changing each burst	
Auto Refresh Current	I_{DD5}	80	mA	CKE = HIGH; t_{CK} = t_{CK} (min); t_{RFC} = t_{RFC} (min); address and control inputs are SWITCHING; data input signals are STABLE	
Deep Power-down Current	I_{DD8}	10	uA	Address and control pins are disable; data input signals are STABLE	

Advanced Data Retention current (V_{DD}/V_{DDQ}=1.70~1.95V)

Parameter (Self Refresh Current)	Symbol	Max.	Unit	Condition	Note
PASR="000" (full)	I_{DD6}	250	uA	-25 C ° ~ +40 C° CKE=L	
PASR="001" (2BK)		220	uA		
PASR="010" (1BK)		200	uA		
PASR="000" (full)	I_{DD6}	480	uA	+40 C ° ~+70 C° CKE=L	
PASR="001" (2BK)		350	uA		
PASR="010" (1BK)		280	uA		
PASR="000" (full)	I_{DD6}	600	uA	+70 C ° ~ +85 C° CKE=L	
PASR="001" (2BK)		400	uA		
PASR="010" (1BK)		300	uA		

Note: 1. I_{DD} specifications are tested after the device is properly initialized.
2. Input slew rate is specified by Test Conditions.
3. Definitions for I_{DD}:
LOW is defined as V IN ≤ 0.1 * V $_{DDQ}$;
HIGH is defined as V IN ≥ 0.9 * V $_{DDQ}$;
STABLE is defined as inputs stable at a HIGH or LOW level;
SWITCHING is defined as:
Address and command: inputs changing between HIGH and LOW once per two clock cycles;
Data bus inputs: DQ changing between HIGH and LOW once per clock cycle; DM and DQS are STABLE.

DC Characteristics 2

Recommended operating conditions unless otherwise noted, V_{DD} / V_{DDQ} = 1.7~1.95

Parameter	Symbol	Min	Max.	Unit	Pins	Note
Input leakage current	I_{LI}	-2	2	uA	$0 \le V_{IN} \le V_{DDQ}$	
Output leakage current	I_{LO}	-1.5	1.5	uA	$0 \le V_{OUT} \le V_{DDQ}$ DQ = disable	
Output high voltage	V_{OH}	0.9 x V_{DDQ}		V	I_{OH} = -0.1mA	
Output low voltage	V_{OL}	-	0.1 x V_{DDQ}	V	I_{OL} = 0.1mA	

Pin Capacitance

Parameter	Pins	Symbol	MIN	MAX	Unit	Notes
Input capacitance:	CLK, CLK#	C_{I1}	1.5	3.5	pF	1
	All other input-only pins	C_{I2}	1.5	3.0	pF	1
Delta Input capacitance	CLK, CLK#	C_{DI1}	-	0.25	pF	1
	All other input-only pins	C_{DI2}	-	0.5	pF	1
Data Input/output capacitance	DQs, DQS, DM	C_{IO}	2.0	4.5	pF	1, 2
Delta Input/output capacitance:	DQs, DQS, DM	C_{DIO}	-	0.5	pF	1

Note:
1. These parameters are measured on conditions: f = 100MHz, V_{OUT} = V_{DDQ}/2, ΔV_{OUT} = 0.2V, TA = +25°C.
2. D_{OUT} circuits are disabled.

AC Characteristics (Reference)

Recommended operating condition unless otherwise noted, V_{DD}/V_{DDQ} = 1.7~1.95V, T_A = -25 to 85°C

Parameter	Symbol	200MHz		Unit	Note
		min	max		
Clock cycle time	t_{CK}	5.0		ns	
CLK high-level width	t_{CH}	0.45	0.55	t_{CK}	
CLK low-level width	t_{CL}	0.45	0.55	t_{CK}	
CLK half period	T_{HP}	Min (t_{CH}, t_{CL})	-	t_{CK}	
DQ output access time from CLK, CLK#	t_{AC}	2.0	5.0	ns	2, 8
DQS-in cycle time	t_{DSC}	0.9	1.1	t_{CK}	
DQS output access time from CLK, CLK#	t_{DQSCK}	2.0	5.0	ns	2, 8
DQ-out high-impedance from CLK, CLK#	t_{HZ}	-	5.0	ns	5, 8
DQ-out low-impedance from CLK, CLK#	t_{LZ}	1.0	-	ns	6, 8
DQS to DQ skew	t_{DQSQ}	-	0.4	ns	3
DQ/DQS output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	-	ns	4
Data hold skew factor	t_{QHS}	-	0.5	ns	
DQ and DM input setup time	t_{DS}	0.5	-	ns	3
DQ and DM input hold time	t_{DH}	0.5	-	ns	3
DQ and DM input pulse width	t_{DIPW}	1.6	-	ns	
Read Preamble	t_{RPRE}	0.9	1.1	t_{CK}	
Read Postamble	t_{RPST}	0.4	0.6	t_{CK}	
Write preamble setup time	t_{WPRES}	0	-	ns	
Write preamble	t_{WPRE}	0.25	-	t_{CK}	
Write postamble	t_{WPST}	0.4	0.6	t_{CK}	7
Write command to first DQS latching transition	t_{DQSS}	0.75	1.25	t_{CK}	
DQS falling edge to CLK setup time	t_{DSS}	0.2	-	t_{CK}	
DQS falling edge hold time from CLK	t_{DSH}	0.2	-	t_{CK}	
DQS input high pulse width	t_{DQSH}	0.4	-	t_{CK}	
DQS input low pulse width	t_{DQSL}	0.4	-	t_{CK}	
Address and control input setup time	t_{IS}	0.9	-	ns	3
Address and control input hold time	t_{IH}	0.9	-	ns	3
Address and control input pulse width	t_{IPW}	2.3	-	ns	3
Mode register set command cycle time	t_{MRD}	2	-	t_{CK}	
Active to precharge command period	t_{RAS}	40	120000	ns	
Active to Active/Auto-refresh command period	t_{RC}	55	-	ns	
Auto-refresh to Active/ Auto-refresh command period	t_{RFC}	96	-	ns	
Active to Read/Write delay	t_{RCD}	15	-	ns	

Parameter	Symbol	200MHz		Unit	Note
		min	max		
Precharge to Active command period	t_{RP}	15	-	ns	
Column address to column address delay	t_{CCD}	1	-	t_{CK}	
Active to Active command period	t_{RRD}	10	-	ns	
WRITE recovery time	t_{WR}	15		ns	
Auto precharge write recovery and precharge time	t_{DAL}	-	-		9
Self-Refresh exit period	t_{SREX}	120	-	ns	
Power-down entry	t_{PDEN}	2	-	t_{CK}	
Power-down exit to command input	t_{PDEX}	1	-	t_{CK}	
Internal Write to READ command delay	t_{WTR}	2	-	t_{CK}	
Refresh period	t_{REF}	-	64	ms	
Average periodic refresh interval	t_{REFI}		7.8	us	
CKE minimum pulse width	t_{CKE}	2	-	t_{CK}	
Write to pre-charge command delay (same bank)	t_{WPD}	4+BL/2	-	t_{CK}	
Read to pre-charge command delay (same bank)	t_{RPD}	BL/2	-	t_{CK}	
Write to read command delay (to input all data)	t_{WRD}	3+BL/2	-	t_{CK}	
Burst stop command to write command delay (CL=3)	t_{BSTW}	3	-	t_{CK}	
Burst stop command to DQ high-Z (CL=3)	t_{BSTZ}	3	-	t_{CK}	
Read command to write command delay (to output all data) (CL=3)	t_{WRD}	3+BL/2	-	t_{CK}	
Precharge command to high-Z (CL=3)	t_{HZP}	3	-	t_{CK}	
Mode register set command cycle time	t_{MRD}	2	-	t_{CK}	

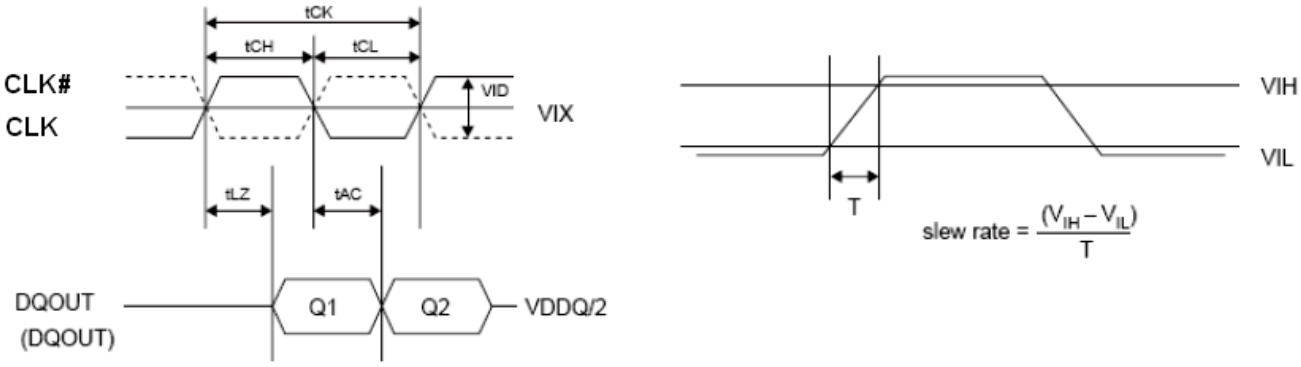
Note:

1. On all AC measurements, we assume the test conditions shown in “Test conditions” and full driver strength is assumed for the output load, that is both A6 and A5 of EMRS is set to be “L”.
2. This parameter defines the signal transition delay from the cross point of CK and CK#. The signal transition is defined to occur when the signal level crossing $V_{DDQ}/2$.
3. The timing reference level is $V_{DDQ}/2$.
4. Output valid window is defined to be the period between two successive transition of data out signals. The signal transition is defined to occur when the signal level crossing $V_{DDQ}/2$.
5. t_{HZ} is defined as D_{OUT} transition delay from low-Z to high-Z at the end of read burst operation. The timing reference is cross point of CK and CK#. This parameter is not referred to a specific D_{OUT} voltage level, but specify when the device output stops driving.
6. t_{LZ} is defined as D_{OUT} transition delay from high-Z to low-Z at the beginning of read operation. This parameter is not referred to a specific D_{OUT} voltage level, but specify when the device output begins driving.
7. The transition from low-Z to high-Z is defined to occur when the device output stops driving. A specific reference voltage to judge this transition is not given.
8. t_{AC}, t_{DQSCK}, t_{HZ} and t_{LZ} are specified with 15pF bus loading condition.
9. Minimum 3 clocks of t_{DAL} (= t_{WR} + t_{RP}) is required because it need minimum 2 clocks for t_{WR} and minimum 1 clock for t_{RP}. t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK}): for each of the terms above, if not already an integer, round to the next higher integer.

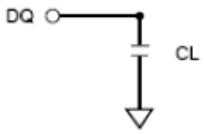
Test Conditions

Parameter	Symbol	Value	Unit	Note
Input high voltage	VIH (AC)	0.8 x V_{DDQ}	V	1
Input low voltage	VIL (AC)	0.2 x V_{DDQ}	V	1
Input differential voltage, CLK and CLK# inputs	VID (AC)	1.4	V	1
Input differential cross point voltage, CLK and CLK# inputs	VIX (AC)	$V_{DDQ/2}$ with V_{DD}=V_{DDQ}	V	
Input signal skew rate	SLEW	1	V/ ns	1
Output load	CL	15	pF	

Note:
1. V_{DD}=$V_{DDQ.}$

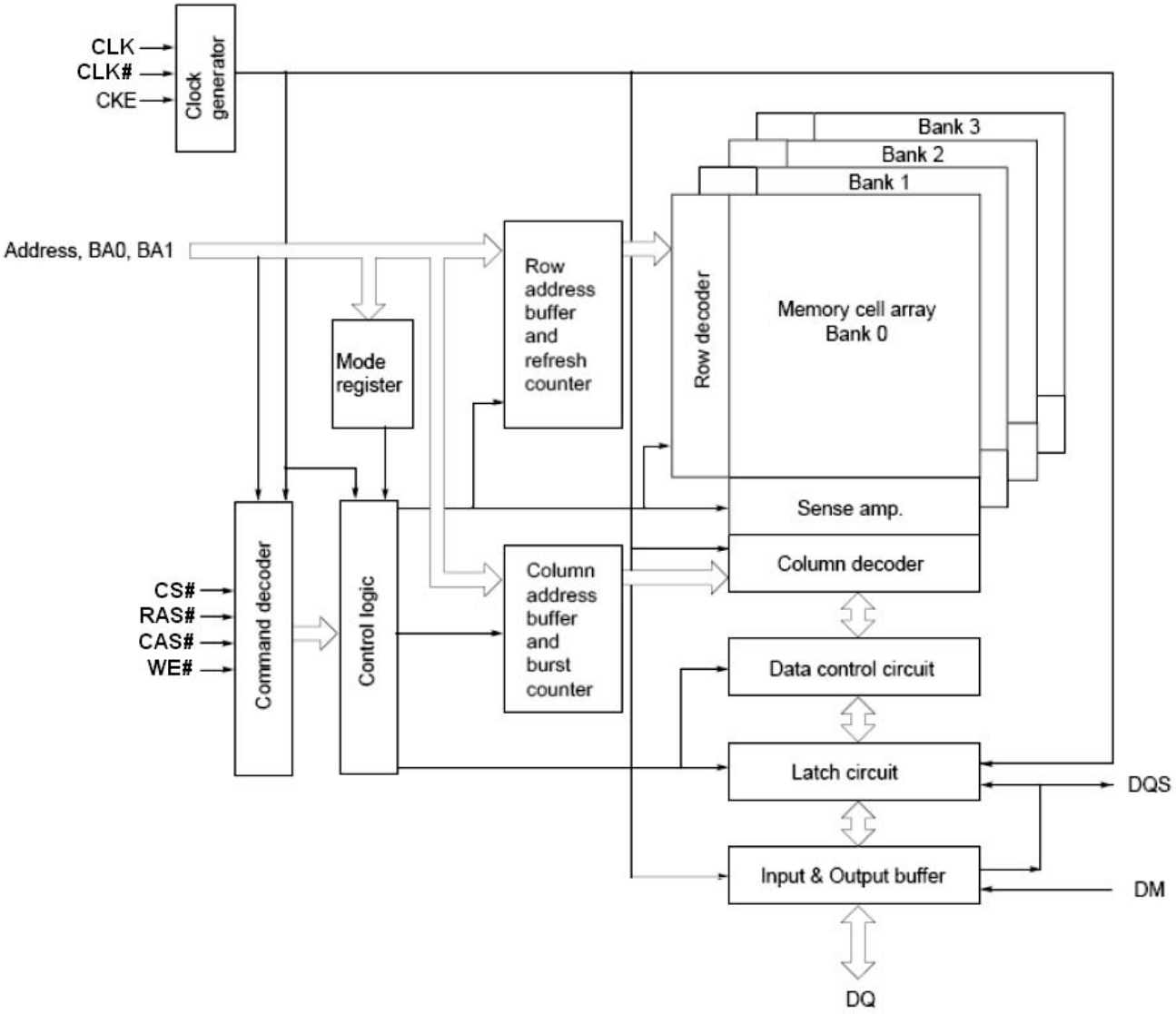


Test Condition (Wave form and Timing Reference)



Output Load

Block Diagram



PIN FUNCTION

CLK, CLK# (input pins)

The CLK and the CLK# are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CLK rising edge and the CK# falling edge. When a read operation, DQSs and DQs are referred to the cross point of the CLK and the CLK#. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VDDQ/2 level. DQSs for write operation are referred to the cross point of the CLK and the CLK#. The other input signals are referred at CLK rising edge.

CS# (input pins)

When CS# is low, commands and data can be input. When CS# is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

RAS#, CAS#, and WE# (input pins)

These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A12 (input pins)

Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CK rising edge and the CK# falling edge in a bank active command cycle. Column address is loaded at the cross point of the CK rising edge and the CK# falling edge in a read or a write command cycle (See “Address Pins Table”). This column address becomes the starting address of a burst operation

Address Pins Table

Page size	Organization	Row address	Column address
2KB	x 16 bits	AX0 to AX12	AY0 to AY9

A10 (AP) (input pin)

A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = high when a precharge command is issued, all banks are precharged. If A10 = low when a precharge command is issued, only the bank that is selected by BA1/BA0 is precharged. If A10 = high when read or write command, auto precharge function is enabled.

BA0 and BA1 (input pins)

BA0 and BA1 are bank select signals (BA). The memory array is divided into bank 0, bank 1, bank 2 and bank 3. (See Bank Select Signal Table)

Bank Select Signal Table

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

Remark: H: V_{IH} and L:V_{IL}

CKE (input pin)

CKE controls power-down mode, self-refresh function and deep power-down function with other command inputs. The CKE level must be kept for 2 clocks at least, that is, if CKE changes at the cross point of the CLK rising edge and the CLK# falling edge with proper setup time t_{IS}, by the next CLK rising edge CKE level must be kept with proper hold time t_{IH}.

DQ0 to DQ15 (input/Output pins)

Data are input to and output from these pins.

UDQS and LDQS (input and output pins)

DQS provides the read data strobes (as output) and the write data strobes (as input). Each DQS pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

UDM and LDM (input pins)

DM is the reference signals of the data input mask function. DM is sampled at the cross point of DQS and $V_{DDQ/2}$. When DM = high, the data input at the same timing are masked while the internal burst counter will be counting up. Each DM pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

DQS and DM Correspondence Table

Organization	DQS	Data mask	DQs
X16 bits	LDQS	LDM	DQ0 to DQ7
	UDQS	UDM	DQ8 to DQ15

V_{DD}, V_{SS}, V_{DDQ} and V_{SSQ} (power supply)

V_{DD} and V_{SS} are power supply pins for internal circuits. V_{DDQ} and V_{SSQ} are power supply pins for the output buffers. V_{DD} must be equal to V_{DDQ}.

COMMAND OPERATIONS

Command Truth Table

Name (Function)	Symbol	CKE		CS#	RAS#	CAS#	WE#	BA1	BA0	AP	ADDR
		n-1	n								
Ignore command	DESL	H	H	H	X	X	X	X	X	X	X
No operation	NOP	H	H	L	H	H	H	X	X	X	X
Burst stop command	BST	H	H	L	H	H	L	X	X	X	X
Column address and read command	READ	H	H	L	H	L	H	V	V	L	V
Read with auto precharge	READA	H	H	L	H	L	H	V	V	H	V
Column address and write command	WRIT	H	H	L	H	L	L	V	V	L	V
Write with auto precharge	WRITA	H	H	L	H	L	L	V	V	H	V
Row address strobe and bank active	ACT	H	H	L	L	H	H	V	V	V	V
Precharge selected bank	PRE	H	H	L	L	H	L	V	V	L	X
Precharge all banks	PALL	H	H	L	L	H	L	X	X	H	X
Refresh	REF	H	H	L	L	L	H	X	X	X	X
	SELF	H	L	L	L	L	H	X	X	X	X
Mode register set	MRS	H	H	L	L	L	L	L	L	L	V
	EMRS	H	H	L	L	L	L	H	L	L	V

Remark: H: V_{IH}, L: V_{IL}, X: Don't care, and V: Valid address input

Notes:
1. The CKE level must be kept for 1 CK cycle at least.

Ignore command [DESL]

When CS# is high at the cross point of the CLK rising edge and the CLK# falling edge, all input signals are neglected and internal state is held.

No operation [NOP]

As long as this command is input at the cross point of the CLK rising edge and the CLK# falling edge, address and data input are neglected and internal state is held.

Burst stop command [BST]

This command stops a current burst operation.

Column address strobe and read command [READ]

This command starts a read operation. The start address of the burst read is determined by the column address (See "Address Pins Table" in Pin Function) and the bank select address. After the completion of the read operation, all output buffers become high-Z.

Read with auto precharge [READA]

This command starts a read operation. After completion of the read operation, precharge is automatically executed.

Column address strobe and write command [WRIT]

This command starts a write operation. The start address of the burst write is determined by the column address (See “Address Pins Table” in Pin Function) and the bank select address.

Write with auto precharge [WRITA]

This command starts a write operation. After completion of the write operation, precharge is automatically executed.

Row address strobe and bank activate [ACT]

This command activates the bank that is selected by BA0 and BA1 (See Bank Select Signal Table) and determines the row address (Address Pins Table in “Pin Function”).

Precharge selected bank [PRE]

This command starts precharge operation for the bank selected by BA0 and BA1. (See Bank Select Signal Table)

Precharge all banks [PALL]

This command starts a precharge operation for all banks.

Refresh [REF/SELF]

This command starts a refresh operation. There are two types of refresh operation, one is auto-refresh, and another is self-refresh. For details, refer to the CKE truth table section.

Mode register set/Extended mode register set [MRS/EMRS]

The DDR Mobile RAM has the two mode registers, the mode register and the extended mode register, to define how it works. The both mode registers are set through the address pins in the mode register set cycle. For details, refer to "Mode register and extended mode register set"

Function Truth Table

The following tables show the operations that are performed when each command is issued in each state of the DDR Mobile RAM.

Current state	CS#	RAS#	CAS#	WE#	Address	Command	Operation
Precharging *1	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	ILLEGAL *11
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL *11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL *11
	L	L	H	H	BA, RA	ACT	ILLEGAL *11
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	X	X		ILLEGAL
Idle *2	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL *11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL *11
	L	L	H	H	BA, RA	ACT	Activating
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	X	REF, SELF	Refresh/Self-refresh *12
	L	L	L	L	MODE	MRS	Mode register set *12
Refresh (auto-refresh) *3	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	H	H	H	L	X	BST	ILLEGAL
	L	H	L	X	X		ILLEGAL
	L	L	X	X	X		ILLEGAL
Activating *4	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	ILLEGAL *11
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL *11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL *11
	L	L	H	H	BA, RA	ACT	ILLEGAL *11
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL *11
	L	L	L	X	X		ILLEGAL
Active *5	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READA	Start read operation
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Start write operation
	L	L	H	H	BA, RA	ACT	ILLEGAL *11
	L	L	H	L	BA, A10	PRE, PALL	PRECHARGE
	L	L	L	X	X		ILLEGAL
Read *6	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	Burst stop
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst read operation to start new read
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL *13
	L	L	H	H	BA, RA	ACT	ILLEGAL *11
	L	L	H	L	BA, A10	PRE, PALL	Interrupting burst read operation to precharge
	L	L	L	X	X		ILLEGAL

Current state	CS#	RAS#	CAS#	WE#	Address	Command	Operation
Read with auto-precharge *7	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL *11
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL *11
	L	L	L	X	X		ILLEGAL
Write *8	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	Burst stop
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst write operation to start read operation
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Interrupting burst write operation to start new write operation
	L	L	H	H	BA, RA	ACT	ILLEGAL *11
	L	L	H	L	BA, A10	PRE, PALL	Interrupting write operation to precharge
	L	L	L	X	X		ILLEGAL
Write recovering *9	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting new write operation
	L	L	H	H	BA, RA	ACT	ILLEGAL *11
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL *11
	L	L	L	X	X		ILLEGAL
Write with auto-precharge *10	H	X	X	X	X	DESL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL *11
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL *11
	L	L	L	X	X		ILLEGAL

Remark: H: V_{IH}, L: V_{IL}, and X: Don't care

Notes:

1. The DDR Mobile RAM is in "Precharging" state for tRP after precharge command is issued.
2. The DDR Mobile RAM reaches "IDLE" state t_{RP} after precharge command is issued.
3. The DDR Mobile RAM is in "Refresh" state for t_{RFC} after auto-refresh command is issued.
4. The DDR Mobile RAM is in "Activating" state for t_{RCD} after ACT command is issued.
5. The DDR Mobile RAM is in "Active" state after "Activating" is completed.
6. The DDR Mobile RAM is in "READ" state until burst data have been output and DQ output circuits are turned off.
7. The DDR Mobile RAM is in "READ with auto precharge" from READA command until burst data has been output and DQ output circuits are turned off.
8. The DDR Mobile RAM is in "WRITE" state from WRIT command to the last burst data are input.
9. The DDR Mobile RAM is in "Write recovering" for t_{WR} after the last data are input.
10. The DDR Mobile RAM is in "Write with auto precharge" until t_{WR} after the last data has been input.
11. This command may be issued for other banks, depending on the state of the banks.
12. Not bank-specific; requires that all banks are idle and no bursts are in progress.

13. Before executing a write command to stop the preceding burst read operation, BST command must be issued. All states and sequences not shown are reserved and/or illegal.

CKE Truth Table

Current state	Command	CKE		CS#	RAS#	CAS#	WE#	Address	Notes
		n-1	n						
Idle	Auto-refresh command (REF)	H	H	L	L	L	H	X	2
Idle	Self-refresh entry (SELF)	H	L	L	L	L	H	X	2
Active/Idle	Power-down entry (PDEN)	H	L	L	H	H	H	X	2
		H	L	H	X	X	X	X	
Idle Self-refresh	Deep power-down entry (DPDEN)	H	L	L	H	H	L	X	
		L	H	L	H	H	H	X	
	Self-refresh exit (SELFX)	L	H	H	X	X	X	X	
Power-down	Power-down exit (PDEX)	L	H	L	H	H	H	X	
		L	H	H	X	X	X	X	
Deep power-down	Power-down exit (DPDEX)	L	H	X	X	X	X	X	

Notes:
1. H: V_{IH}. L: V_{IL}. X: Don't care.
2. All the banks must be in IDLE and no bursts in progress before executing this command.
3. The CKE level must be kept for 1 clock cycle at least.

Auto-refresh command [REF]

This command executes auto-refresh. The bank and the ROW addresses to be refreshed are internally determined by the internal refresh controller. The output buffer becomes high-Z after auto-refresh start. Precharge has been completed automatically after the auto-refresh. The ACT or MRS command can be issued t_{RFC} after the last auto-refresh command. The average refresh interval is 7.8us. To allow for improved efficiency in scheduling, some flexibility in the absolute refresh interval is provided. A maximum of eight auto-refresh commands can be posted to the DDR Mobile RAM or the maximum absolute interval between any auto-refresh command and the next auto-refresh command is 8 x tREFI.

Self-refresh entry [SELF]

This command starts self-refresh. The self-refresh operation continues as long as CKE is held low. During the self-refresh operation, all ROW addresses are repeated refreshing by the internal refresh controller. A self-refresh is terminated by a self-refresh exit command.

Power-down mode entry [PDEN]

tPDEN (= 2 clocks) after the cycle when [PDEN] is issued, the DDR Mobile RAM enters into power-down mode. In power-down mode, power consumption is suppressed by deactivating the input initial circuit. Power-down mode continues while CKE is held low. No internal refresh operation occurs during the power-down mode.

Deep power-down mode entry [DPDEN]

After the command execution, deep power-down mode continues while CKE remains low. Before executing deep power-down, all banks must be precharged or in idle state.

Self-refresh exit [SELFX]

This command is executed to exit from self-refresh mode. tSREX after [SELFX], the device will be into idle state.

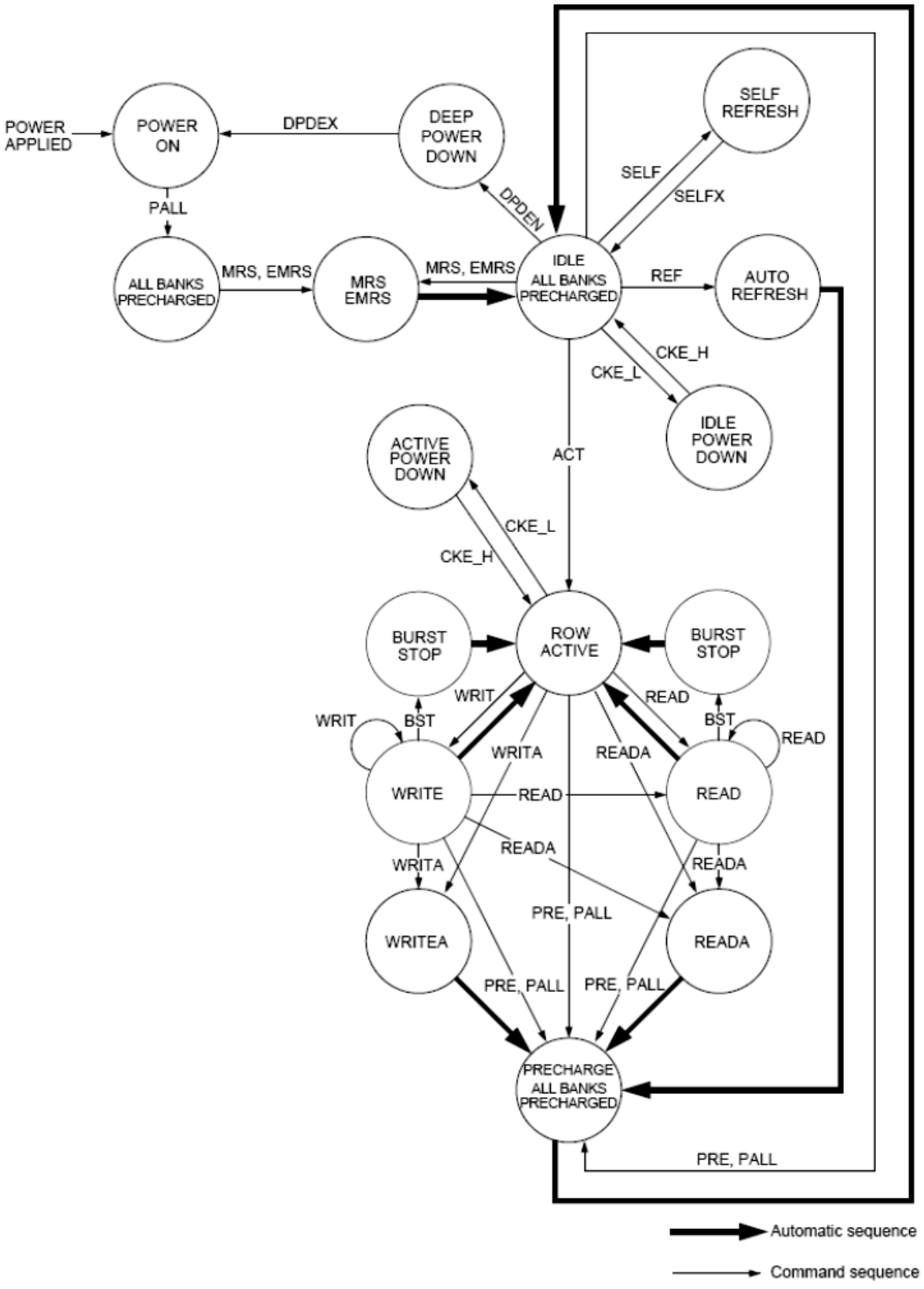
Power-down mode exit [PDEX]

The DDR Mobile RAM can exit from power-down mode tPDEX (1 cycle min.) after the cycle when [PDEX] is issued.

Deep power-down mode exit [DPDEX]

As CKE goes high in the deep power-down mode, the DDR Mobile RAM exits from the deep power-down mode through deep power-down exiting sequence.

SIMPLIFIED STATE DIAGRAM



Operation of the DDR Mobile RAM

Initialization

The DDR Mobile RAM is initialized in the power-on sequence according to the following.

1. Provide power, the device core power (V_{DD}) and the device I/O power (V_{DDQ}) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that VDD and V_{DDQ} are from the same power source. Also assert and hold Clock Enable (CKE) to a LV-CMOS logic high level.
2. Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock.
3. There must be at least 200μs of valid clocks before any command may be given to the DRAM. During this time NOP or deselect (DESL) commands must be issued on the command bus.
4. Issue a precharge all command.
5. Provide NOPs or DESL commands for at least tRP time.
6. Issue an auto-refresh command followed by NOPs or DESL command for at least t_{RFC} time. Issue the second auto-refresh command followed by NOPs or DESL command for at least t_{RFC} time. Note as part of the initialization sequence there must be two auto-refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.
7. Using the MRS command, load the base mode register. Set the desired operating modes.
8. Provide NOPs or DESL commands for at least t_{MRD} time.
9. Using the MRS command, program the extended mode register for the desired operating modes.
10. Provide NOP or DESL commands for at least t_{MRD} time.
11. The DRAM has been properly initialized and is ready for any valid command.

Mode Register and Extended Mode Register Set

There are two mode registers, the mode register and the extended mode register so as to define the operating mode. Parameters are set to both through the A0 to the A12 and BA0 and BA1 pins by the mode register set command [MRS] or the extended mode register set command [EMRS]. The mode register and the extended mode register are set by inputting signal via the A0 to the A12 and BA0 and BA1 pins during mode register set cycles. BA0 and BA1 determine which one of the mode register or the extended mode register are set. Prior to a read or a write operation, the mode register must be set.

Mode register

The mode register has four fields;

Reserved : A12 through A7 CAS# latency : A6 through A4 Wrap type : A3 Burst length : A2 through A0

Following mode register programming, no command can be issued before at least 2 clocks have elapsed.

CAS# Latency

CAS# latency must be set to 3

Burst length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become high-Z. The burst length is programmable as 2, 4, 8 and 16.

Wrap type (Burst sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either ”Sequential” or “Interleave”. “Burst Operation” shows the addressing sequence for each burst length for each wrap type.

Extended mode register

The extended mode register has three fields;

Reserved : A12 through A7, A4, A3 Driver Strength : A6 through A5 Partial Array Self-Refresh : A2 through A0

Following extended mode register programming, no command can be issued before at least 2 clocks have elapsed.

Driver strength

By setting specific parameter on A6 and A5, driving capability of data output drivers is selected.

Auto Temperature Compensated Self-Refresh (ATCSR)

The DDR Mobile RAM automatically changes the self-refresh cycle by on die temperature sensor. No extended mode register program is required. Manual TCSR (Temperature Compensated Self-Refresh) is not implemented.

Partial Array Self-Refresh

Memory array size to be refreshed during self-refresh operation is programmable in order to reduce power. Data outside the defined area will not be retained during self-refresh.

Deep Power-Down Exit Sequence

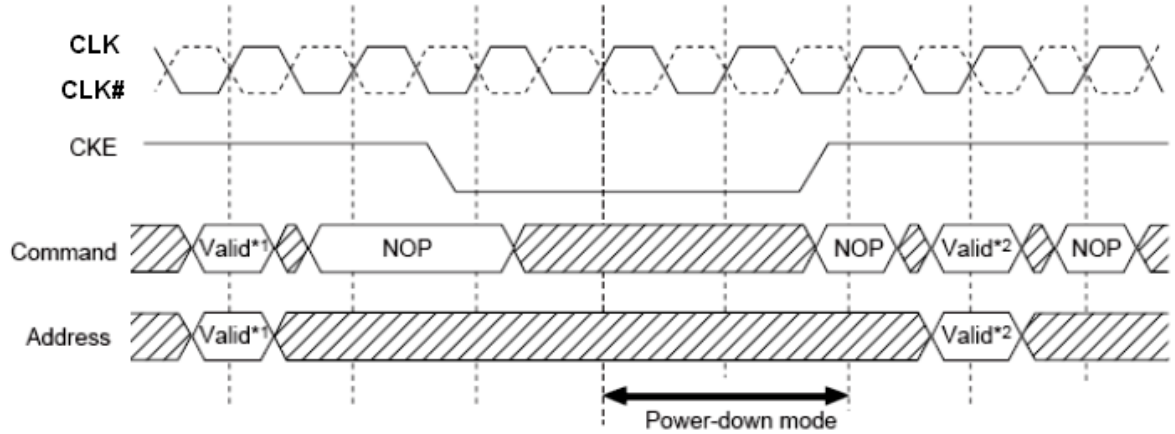
In order to exit from the deep power-down mode and enter into the idle mode, the following sequence is needed, which is similar to the power-on sequence.

(1) A 200µs or longer pause must precede any command other than ignore command (DESL).
(2) After the pause, all banks must be precharged using the precharge command (the precharge all banks command is convenient).
(3) Once the precharge is completed and the minimum t_{RP} is satisfied, two or more Auto-refresh must be performed.
(4) Both the mode register and the extended mode register must be programmed. After the mode register set cycle or the extended mode register set cycle, t_{MRD} (2 clocks minimum) pause must be satisfied.

Remarks:
1. The sequence of Auto-refresh, mode register programming and extended mode register programming above may be transposed.
2. CKE must be held high.

Power-Down Mode and CKE Control

DDR Mobile RAM will be into power-down mode at the second CLK rising edge after CKE to be low level with NOP or DESL command at first CLK rising edge after CKE signal to be low.

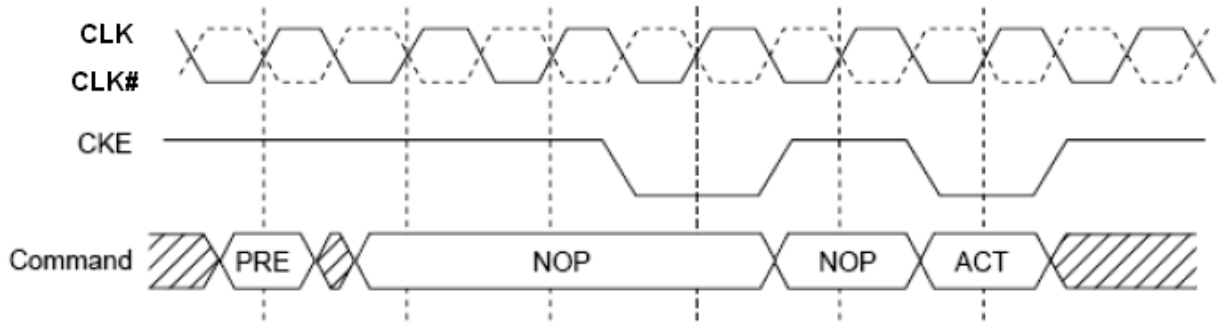


Notes:
1. Valid*1 can be either Activate command or Precharge command, When Valid*1 is Activate command, power-down mode will be active power-down mode, while it will be precharge power down mode, if Valid*1 will be Precharge command.

2. Valid*2 can be any command as long as all of specified AC parameters are satisfied.

Power-Down Entry and Exit

However, if the CKE has one clock cycle high and on clock cycle low just as below, even DDR Mobile RAM will not enter power-down.



Note: Assume PRE and ACT command is closing and activating same bank.

CKE Control

Mode Register Definition

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	0	0	0	0	LTMODE			WT	BL			Mode Register Set

	Bits6-4	/CAS latency
Latency mode	000	R
	001	R
	010	R
	011	3
	100	R
	101	R
	110	R
	111	R

	Bits2-0	WT = 0	WT = 1
Burst length	000	R	R
	001	2	2
	010	4	4
	011	8	8
	100	16	16
	101	R	R
	110	R	R
	111	R	R

Wrap type	0	Sequential
	1	Interleave

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
1	0	0	0	0	0	0	0	DS		0	0	PASR			Extended Mode Register Set

	Bits6-5	Strength
Driver Strength	00	Normal
	01	1/2 strength
	10	1/4 strength
	11	1/8 strength

	Bits2-0	Refresh Array
Partial Array Self Refresh	000	All banks
	001	Bank A & Bank B (BA1=0)
	010	Bank A (BA0=BA1=0)
	011	R
	100	R
	101	R
	110	R
	111	R

Remark: R: Reserved

Burst Operation

The burst type (BT) and the first three bits of the column address determine the order of a data out.

Burst Length	Starting Column Address (A3, A2,A1,A0)	Burst type = Sequential A3 = 0	Burst type = Interleaved A3 = 1
2	0000	0,1	0,1
	0001	1,0	1,0
4	0000	0,1,2,3	0,1,2,3
	0001	1,2,3,0	1,0,3,2
	0010	2,3,0,1	2,3,0,1
	0011	3,0,1,2	3,2,1,0
8	0000	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
	0001	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
	0010	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
	0011	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
	0100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
	0101	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
	0110	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
	0111	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0
16	0000	0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F	0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F
	0001	1,2,3,4,5,6,7,8,9,A,B,C,D,E,F,0	1,0,3,2,5,4,7,6,9,8,B,A,D,C,F,E
	0010	2,3,4,5,6,7,8,9,A,B,C,D,E,F,0,1	2,3,0,1,6,7,4,5,A,B,8,9,E,F,C,D
	0011	3,4,5,6,7,8,9,A,B,C,D,E,F,0,1,2	3,2,1,0,7,6,5,4,B,A,9,8,F,E,D,C
	0100	4,5,6,7,8,9,A,B,C,D,E,F,0,1,2,3	4,5,6,7,0,1,2,3,C,D,E,F,8,9,A,B
	0101	5,6,7,8,9,A,B,C,D,E,F,0,1,2,3,4	5,4,7,6,1,0,3,2,D,C,F,E,9,8,B,A
	0110	6,7,8,9,A,B,C,D,E,F,0,1,2,3,4,5	6,7,4,5,2,3,0,1,E,F,C,D,A,B,8,9
	0111	7,8,9,A,B,C,D,E,F,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0,F,E,D,C,B,A,9,8
	1000	8,9,A,B,C,D,E,F,0,1,2,3,4,5,6,7	8,9,A,B,C,D,E,F,0,1,2,3,4,5,6,7
	1001	9,A,B,C,D,E,F,0,1,2,3,4,5,6,7,8	9,8,B,A,D,C,F,E,1,0,3,2,5,4,7,6
	1010	A,B,C,D,E,F,0,1,2,3,4,5,6,7,8,9	A,B,8,9,E,F,C,D,2,3,0,1,6,7,4,5
	1011	B,C,D,E,F,0,1,2,3,4,5,6,7,8,9,A	B,A,9,8,F,E,D,C,3,2,1,0,7,6,5,4
	1100	C,D,E,F,0,1,2,3,4,5,6,7,8,9,A,B	C,D,E,F,8,9,A,B,4,5,6,7,0,1,2,3
	1101	D,E,F,0,1,2,3,4,5,6,7,8,9,A,B,C	D,C,F,E,,9,8,B,A,5,4,7,6,1,0,3,2
	1110	E,F,0,1,2,3,4,5,6,7,8,9,A,B,C,D	E,F,C,D,A,B,8,9,6,7,4,5,2,3,0,1
	1111	F,0,1,2,3,4,5,6,7,8,9,A,B,C,D,E	F,E,D,C,B,A,9,8,7,6,5,4,3,2,1,0

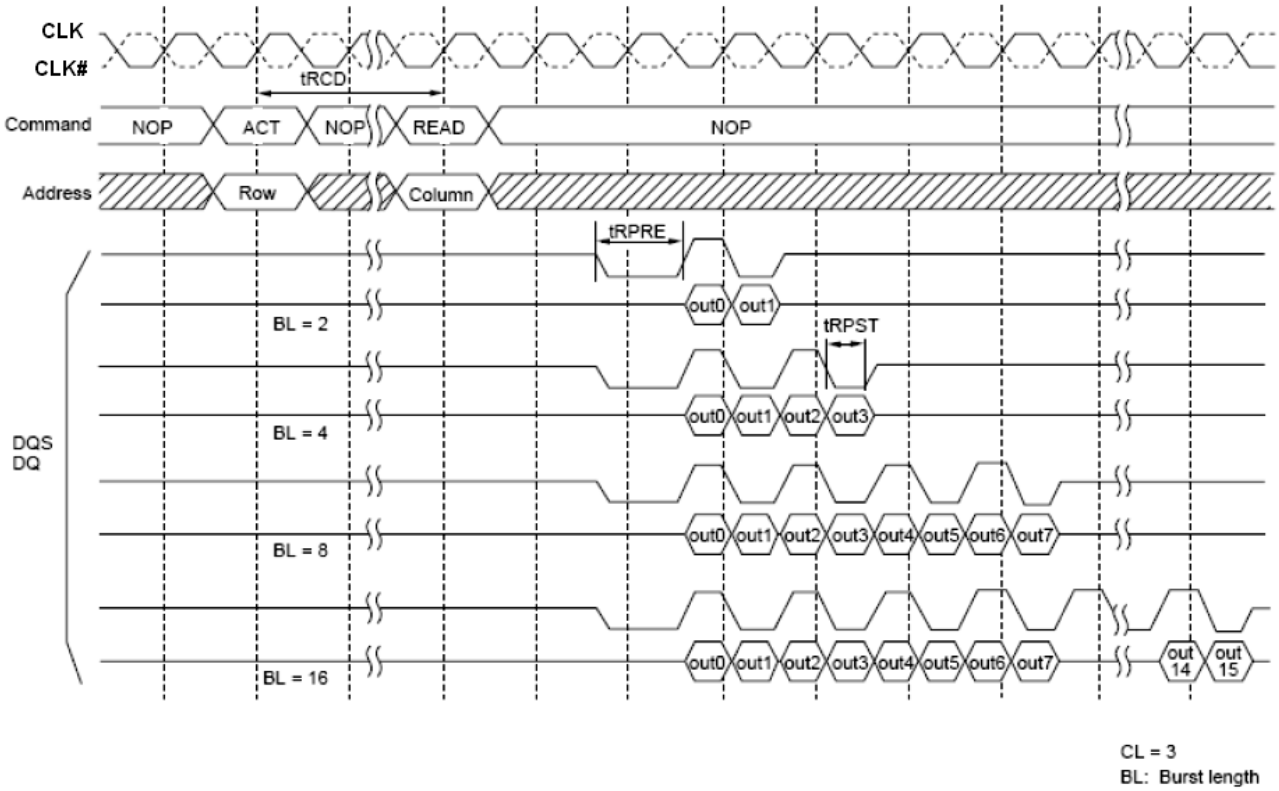
Read/Write Operations

Bank Active

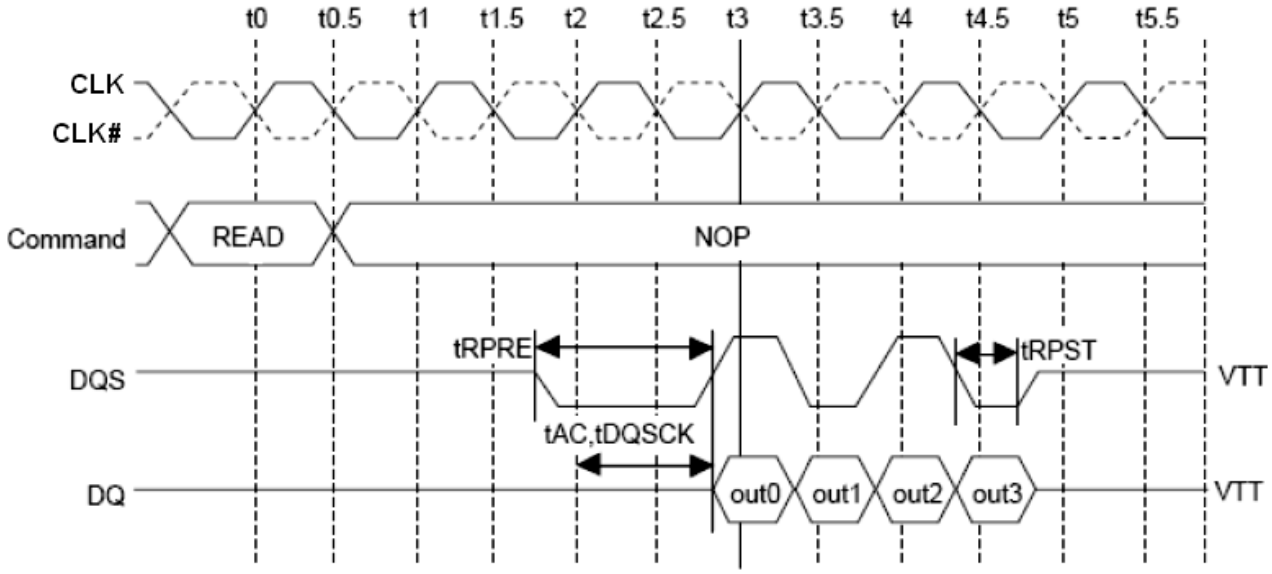
A read or a write operation begins with the bank active command [ACT]. The bank active command determines a bank address and a row address. For the bank and the row, a read or a write command can be issued t_{RCD} after the ACT is issued.

Read operation

The burst length (BL), the /CAS latency (CL) and the burst type (BT) of the mode register are referred when a read command is issued. The burst length (BL) determines the length of a sequential output data by the read command that can be set to 2, 4, 8 or 16. The starting address of the burst read is defined by the column address, the bank select address (See “Pin Function”) in the cycle when the read command is issued. The data output timing is characterized by CL and t_{AC}. The read burst start (CL-1) × t_{CK} + t_{AC} (ns) after the clock rising edge where the read command is latched. The DDR Mobile RAM outputs the data strobe through DQS pins simultaneously with data. t_{RPRE} prior to the first rising edge of the data strobe, the DQS pins are driven low from high-Z state. This low period of DQS is referred as read preamble. The burst data are output coincidentally at both the rising and falling edge of the data strobe. The DQ pins become high-Z in the next cycle after the burst read operation completed. t_{RPST} from the last falling edge of the data strobe, the DQS pins become high-Z. This low period of DQS is referred as read postamble.



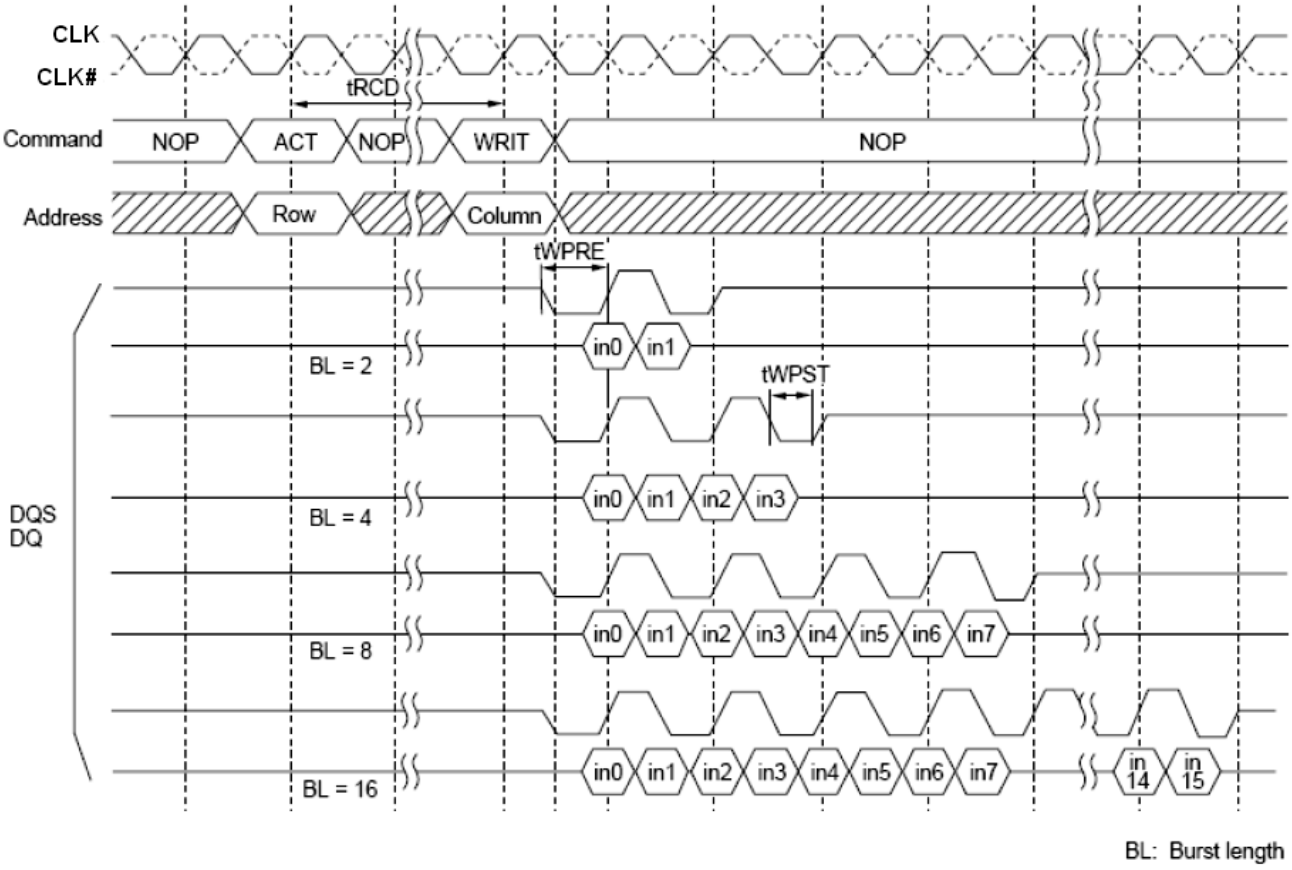
Read Operation (Burst Length)



Read Operation (CAS# Latency)

Write Operation

The burst length (BL) and the burst type (BT) of the mode register are referred when a write command is issued. The burst length (BL) determines the length of a sequential data input by the write command that can be set to 2, 4, 8 or 16. The latency from write command to data input is fixed to 1. The starting address of the burst write is defined by the column address, the bank select address (See “Pin Function”) in the cycle when the write command is issued. DQS should be input as the strobe for the input-data and DM as well during burst operation. t_{WPRE} prior to the first rising edge of DQS, DQS must be set to low. t_{WPST} after the last falling edge of DQS, the DQS pins can be changed to high-Z. The leading low period of DQS is referred as write preamble. The last low period of DQS is referred as write postamble.

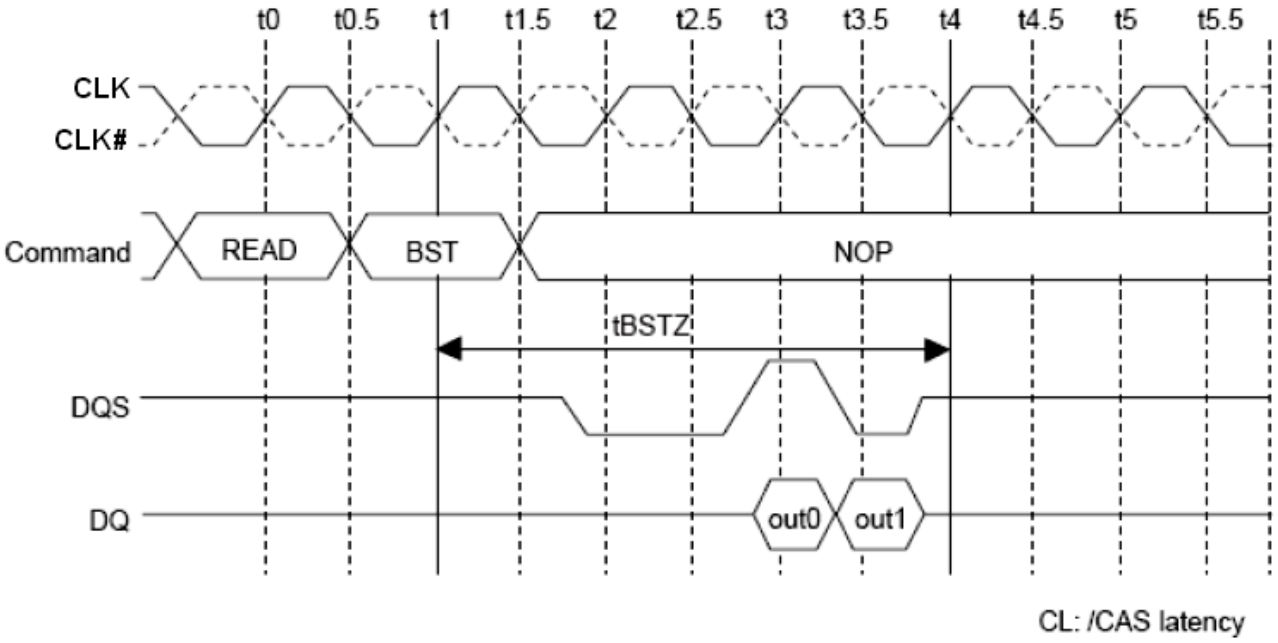


Write Operation

Burst Stop

Burst stop command during burst operation

The burst stop (BST) command stops the burst read and sets all output buffers to high-Z. t_{BSTZ} (= CL) cycles after a BST command issued, all DQ and DQS pins become high-Z. The BST command is also supported for the burst write operation. No data will be written in subsequent cycles. Note that bank address is not referred when this command is executed.

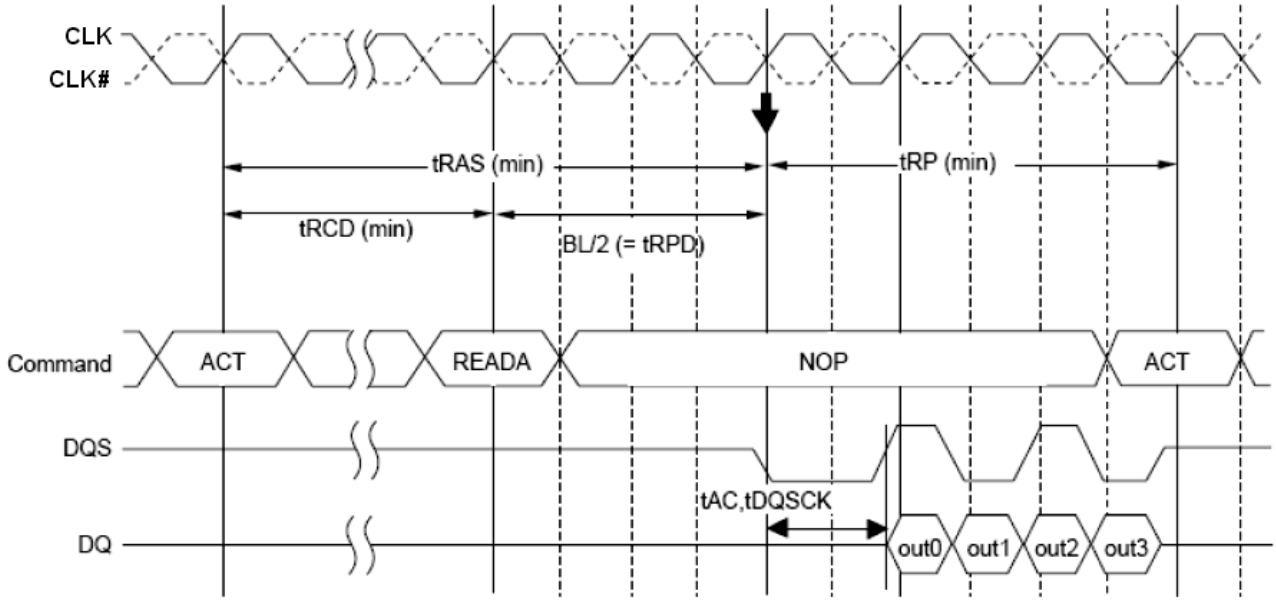


Burst Stop during a Read Operation

Auto Precharge

Read with auto precharge

The precharge is automatically performed after completing a read operation. The precharge starts BL/2 (= t_{RPD}) clocks after READA command input. t_{RAS} lock out mechanism for READA allows a read command with auto precharge to be issued to a bank that has been activated (opened) but has not yet satisfied the t_{RAS} (min) specification. A column command to the other active bank can be issued the next cycle after the last data output. Read with auto precharge command does not limit row commands execution for other bank.

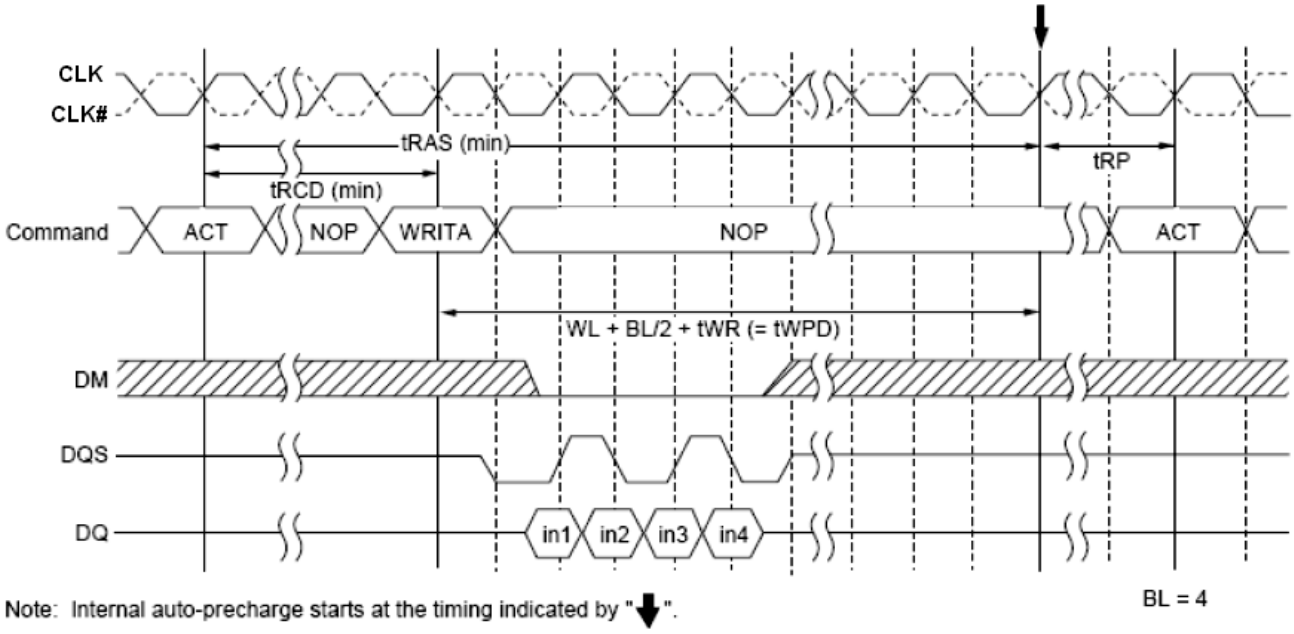


Note: Internal auto-precharge starts at the timing indicated by "↓".

Read with auto precharge

Write with auto precharge

The precharge is automatically performed after completing a burst write operation. The precharge operation is started Write latency (WL) + BL/2 + t_{WR} (= t_{WPD}) clocks after WRITA command issued. A column command to the other banks can be issued the next cycle after the internal precharge.



Burst Write (BL=4)

The Concurrent Auto Precharge

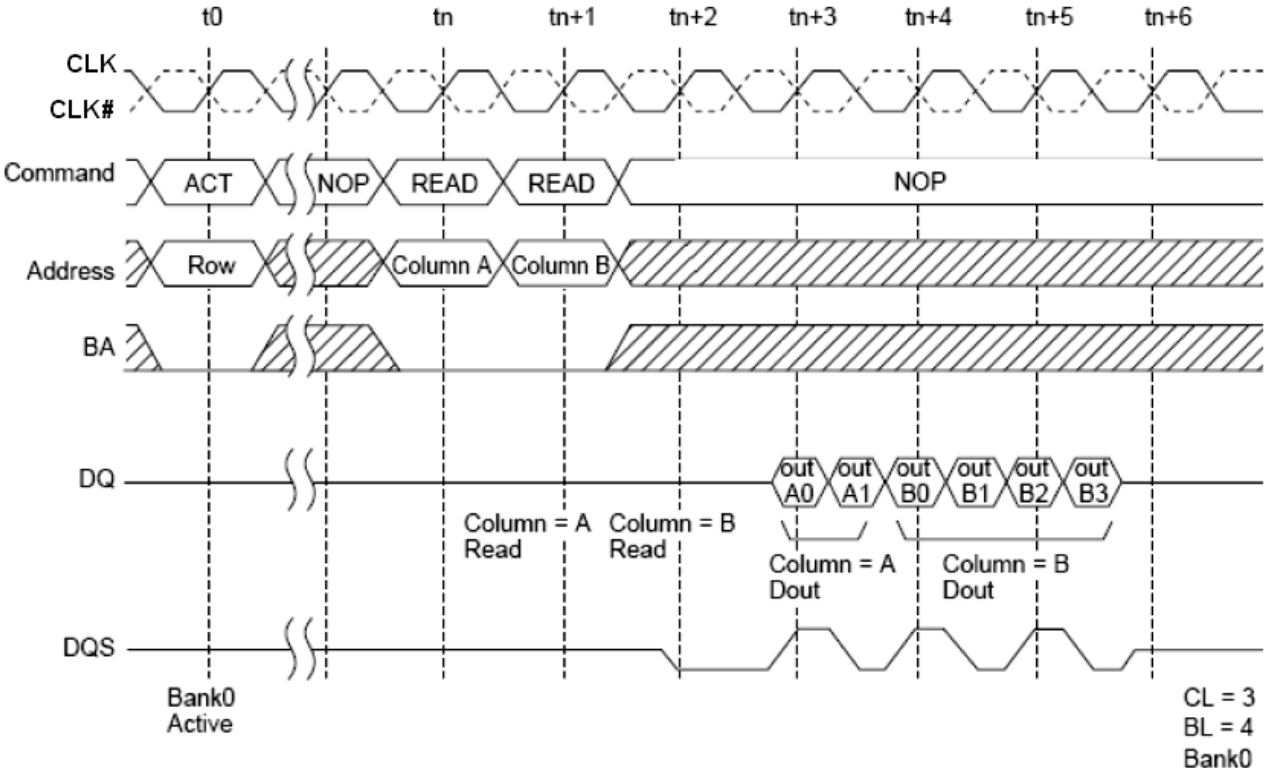
The DDR Mobile RAM supports the concurrent auto precharge feature, a read with auto precharge or a write with auto precharge, can be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided.) The minimum delay from a read or write command with auto precharge, to a command to a different bank, is summarized below.

From command	To command (different bank, non-interrupting command)	Minimum delay (Concurrent AP supported)	Units
Read w/ AP	Read or Read w/ AP	BL/2	t_{CK}
	Write or Write w/ AP	CL (round up) + (BL/2)	t_{CK}
	Precharge or Activate	1	t_{CK}
Write w/ AP	Read or Read w/ AP	1 + (BL/2) + t_{WTR}	t_{CK}
	Write or Write w/ AP	BL/2	t_{CK}
	Precharge or Activate	1	t_{CK}

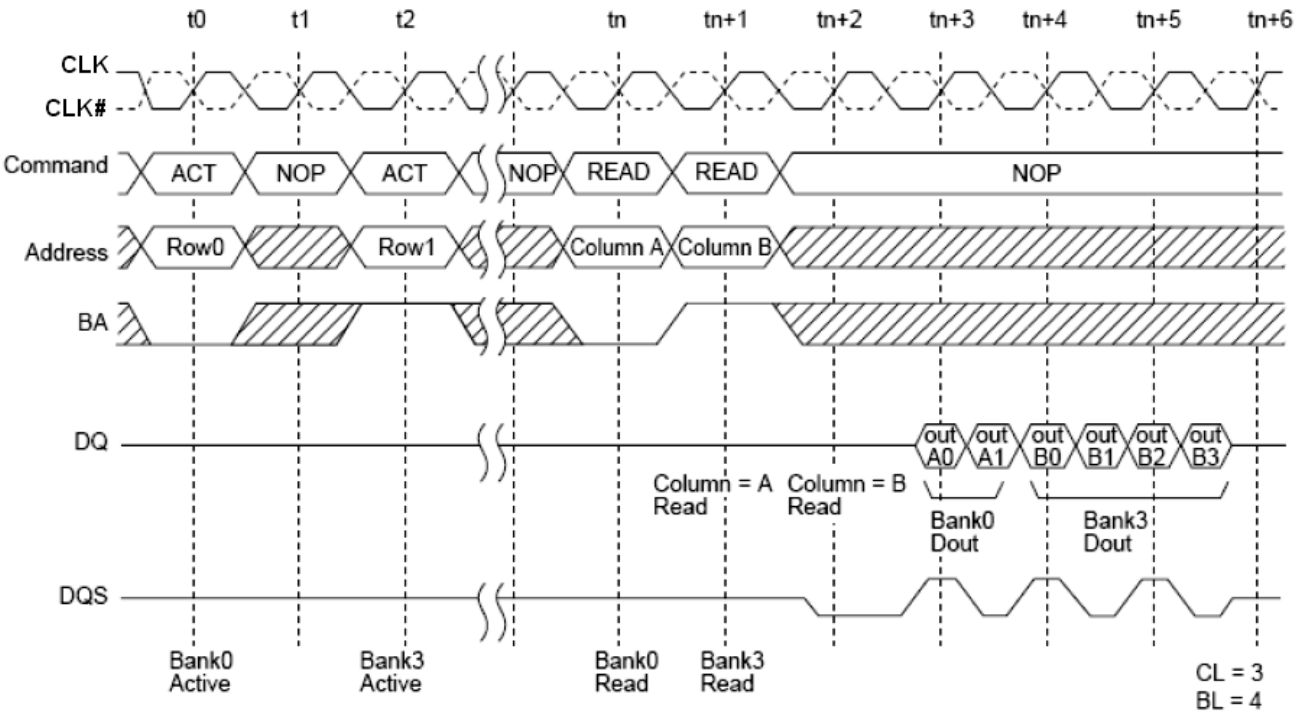
Command Intervals A Read command to the consecutive Read command interval

Destination row of the consecutive read command

	Bank address	Row Address	Status	Operation
1	Same	Same	ACTIVE	The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
2	Same	Different	-	Precharge the bank to interrupt the preceding read operation. t_{RP} after the precharge command, issue the ACT command. t_{RCD} after the ACT command, the consecutive read command can be issued. See 'A read command to the consecutive precharge interval' section.
3	Different	Any	ACTIVE	The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
			IDLE	Precharge the bank without interrupting the preceding read operation. t_{RP} after the precharge command, issue the ACT command. t_{RCD} after the ACT command, the consecutive read command can be issued.



Read to Read command interval (same ROW address in the same bank)

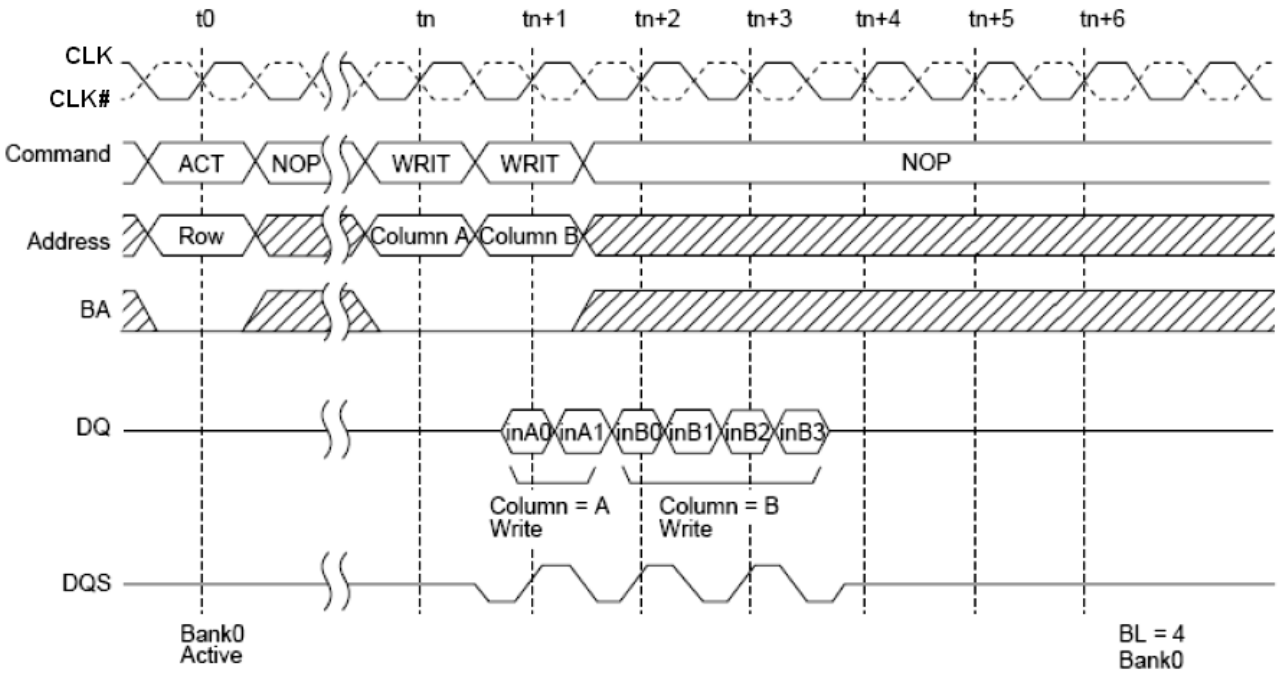


Read to Read command interval (different bank)

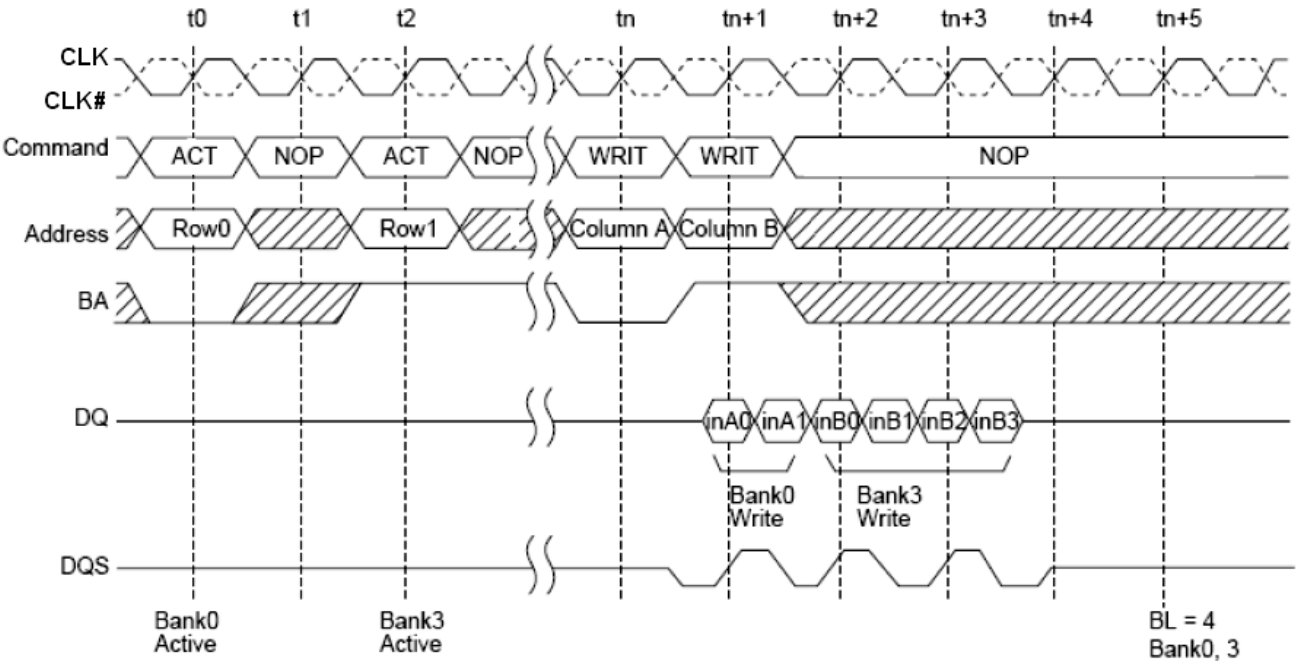
A Write command to the consecutive Write command interval

Destination row of the consecutive write command

	Bank address	Row Address	Status	Operation
1	Same	Same	ACTIVE	The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation.
2	Same	Different	-	Precharge the bank to interrupt the preceding write operation. t_{RP} after the precharge command, issue the ACT command. t_{RCD} after the ACT command, the consecutive write command can be issued. See 'A write command to the consecutive precharge interval' section.
3	Different	Any	ACTIVE	The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation.
			IDLE	Precharge the bank without interrupting the preceding write operation. t_{RP} after the precharge command, issue the ACT command. t_{RCD} after the ACT command, the consecutive write command can be issued.



Write to Write command interval (same ROW address in the same bank)

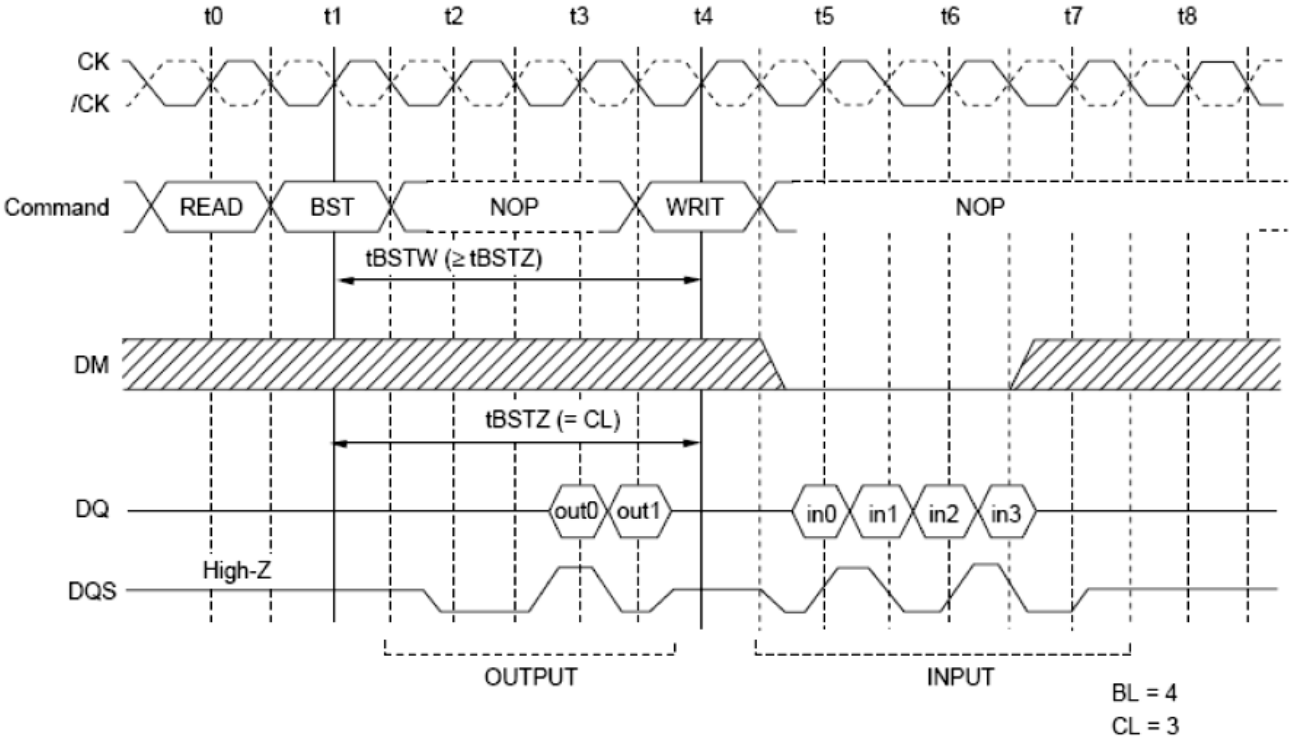


Write to Write command interval (different bank)

A Read command to the consecutive Write command interval with the BST command

Destination row of the consecutive writ command

	Bank address	Row Address	Status	Operation
1	Same	Same	ACTIVE	Issue the BST command. t_{BSTW} (≥ t_{BSTZ}) after the BST command, the consecutive write command can be issued.
2	Same	Different	-	Precharge the bank to interrupt the preceding read operation. t_{RP} after the precharge command, issue the ACT command. t_{RCD} after the ACT command, the consecutive write command can be issued. See 'A read command to the consecutive precharge interval' section.
3	Different	Any	ACTIVE	Issue the BST command. t_{BSTW} (≥ t_{BSTZ}) after the BST command, the consecutive write command can be issued.
			IDLE	Precharge the bank independently of the preceding read operation. t_{RP} after the precharge command, issue the ACT command. t_{RCD} after the ACT command, the consecutive write command can be issued.

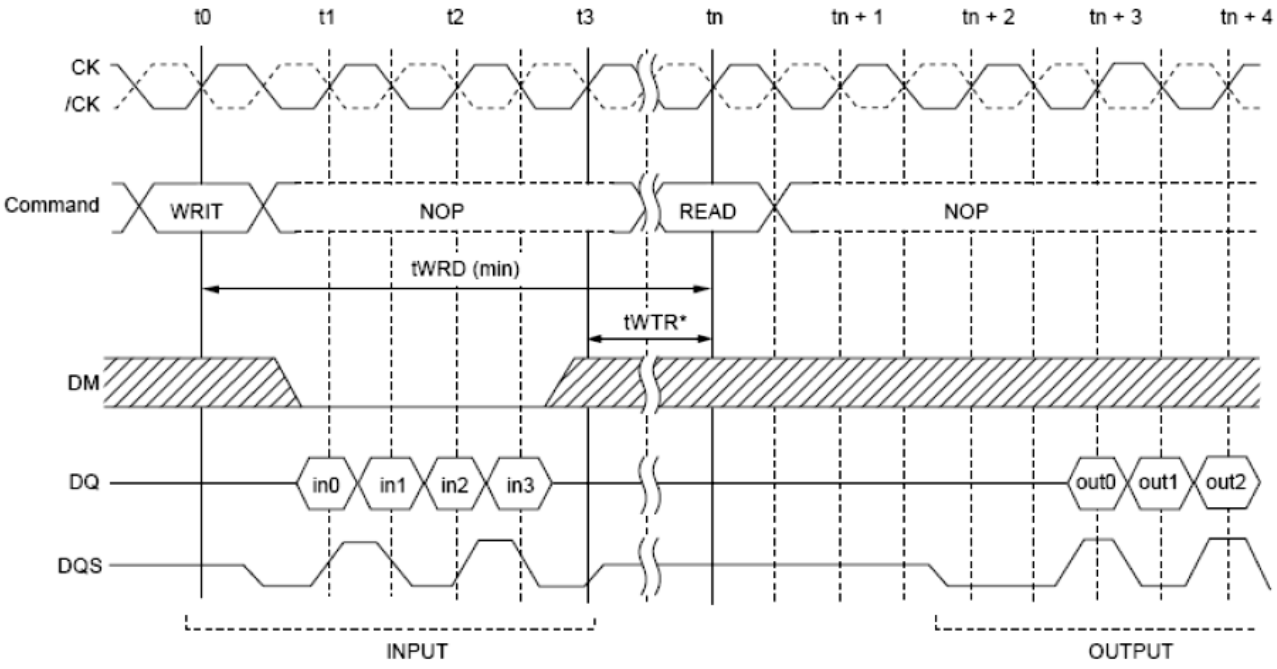


Read to Write command interval

A Write command to the consecutive Read command interval: to complete the burst operation

Destination row of the consecutive read command

	Bank address	Row Address	Status	Operation
1	Same	Same	ACTIVE	To complete the burst operation, the consecutive read command should be performed t_{WRD} after the write command.
2	Same	Different	-	Precharge the bank t_{WPD} after the preceding write command. t_{RP} after the precharge command, issue the ACT command. t_{RCD} after the ACT command, the consecutive read command can be issued. See 'A read command to the consecutive precharge interval' section.
3	Different	Any	ACTIVE	To complete a burst operation, the consecutive read command should be performed t_{WRD} after the write command.
			IDLE	Precharge the bank independently of the preceding write operation. t_{RP} after the precharge command, issue the ACT command. t_{RCD} after the ACT command, the consecutive read command can be issued.



Note: tWTR is referenced from the first positive CK edge after the last desired data in pair tWTR.

BL = 4
CL = 3

Write to Read command interval

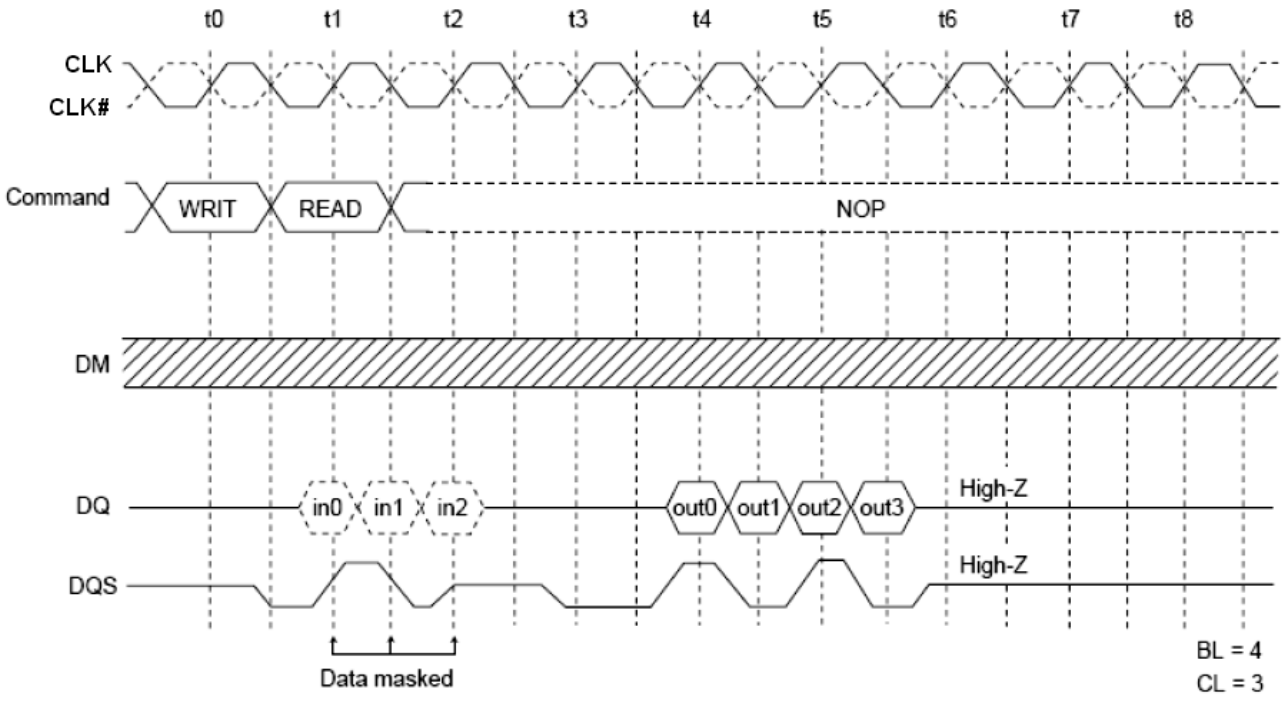
A Write command to the consecutive Read command interval: to interrupt the write operation

Destination row of the consecutive read command

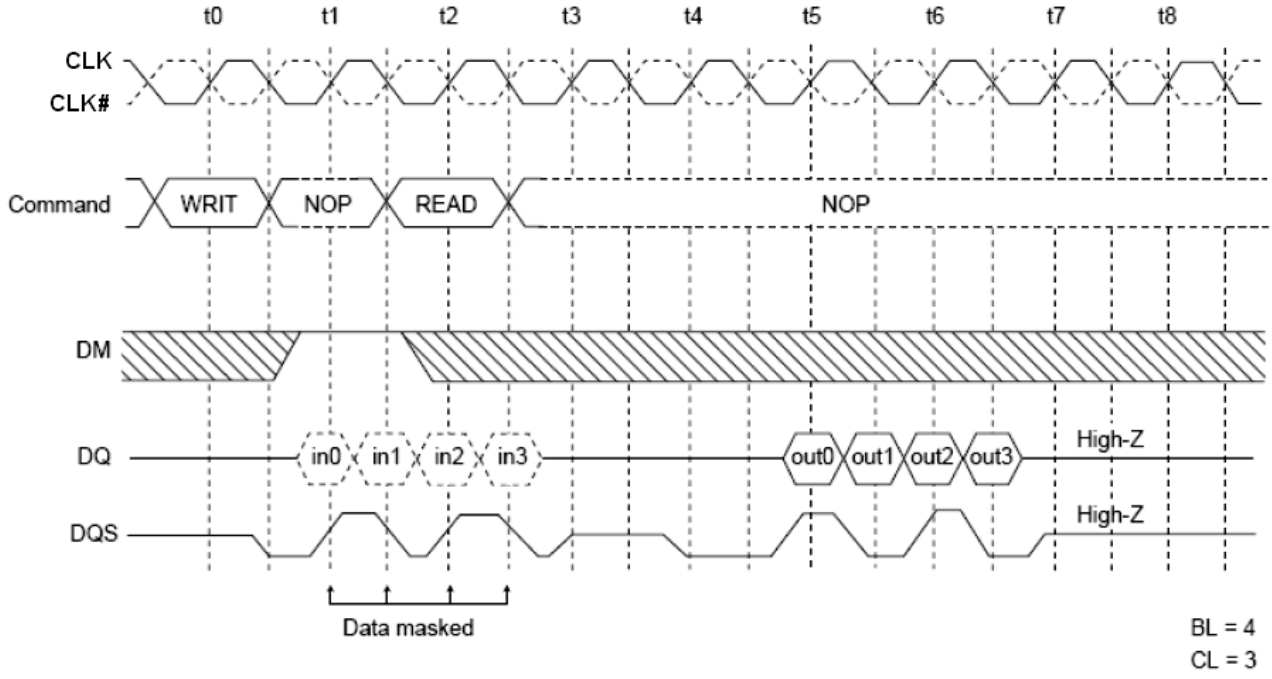
	Bank address	Row Address	Status	Operation
1	Same	Same	ACTIVE	DM must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM is not necessary.
2	Same	Different	-	-*1
3	Different	Any	ACTIVE	DM must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM is not necessary.
			IDLE	*1

Note:
1. Precharge must be preceded to read command. Therefore read command can not interrupt the write operation in this case.

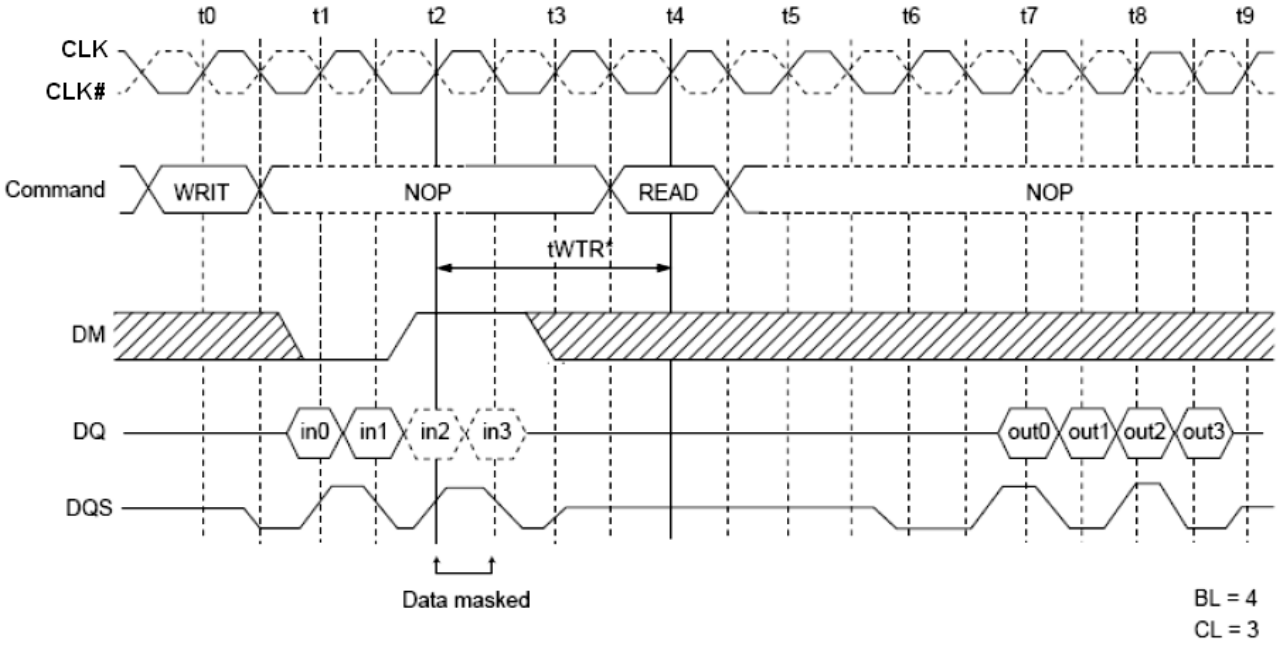
Write to Read Command Interval (same bank, same ROW address)



[Write to Read delay = 1 clock cycle]



[Write to Read delay = 2 clock cycle]

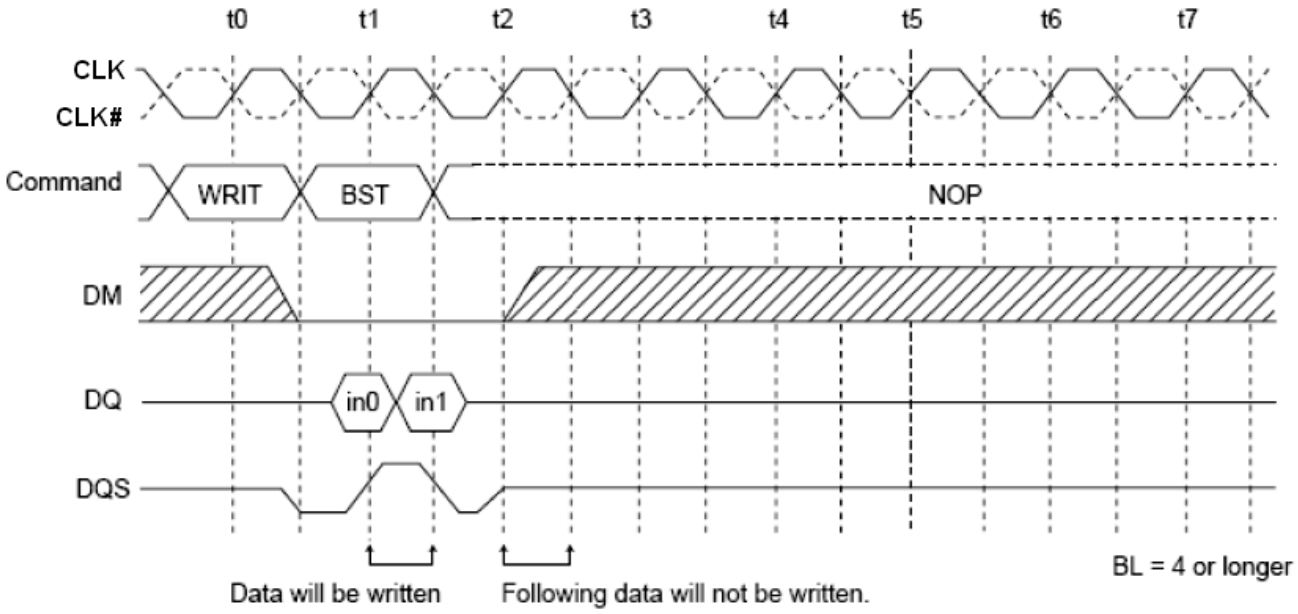


Note: t_{WTR} is referenced from the first positive CK edge after the last desired data in pair t_{WTR}.

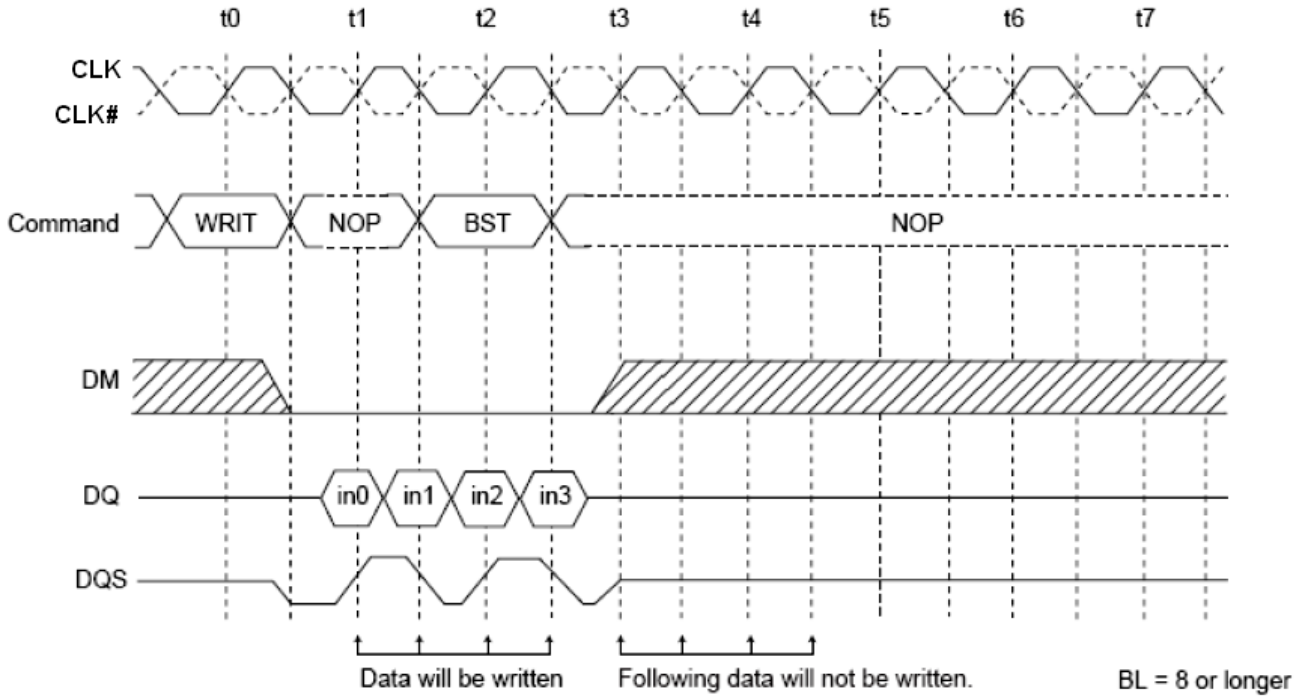
[Write to Read delay = 4 clock cycle]

A Write command to the Bust stop command interval: To interrupt the write operation

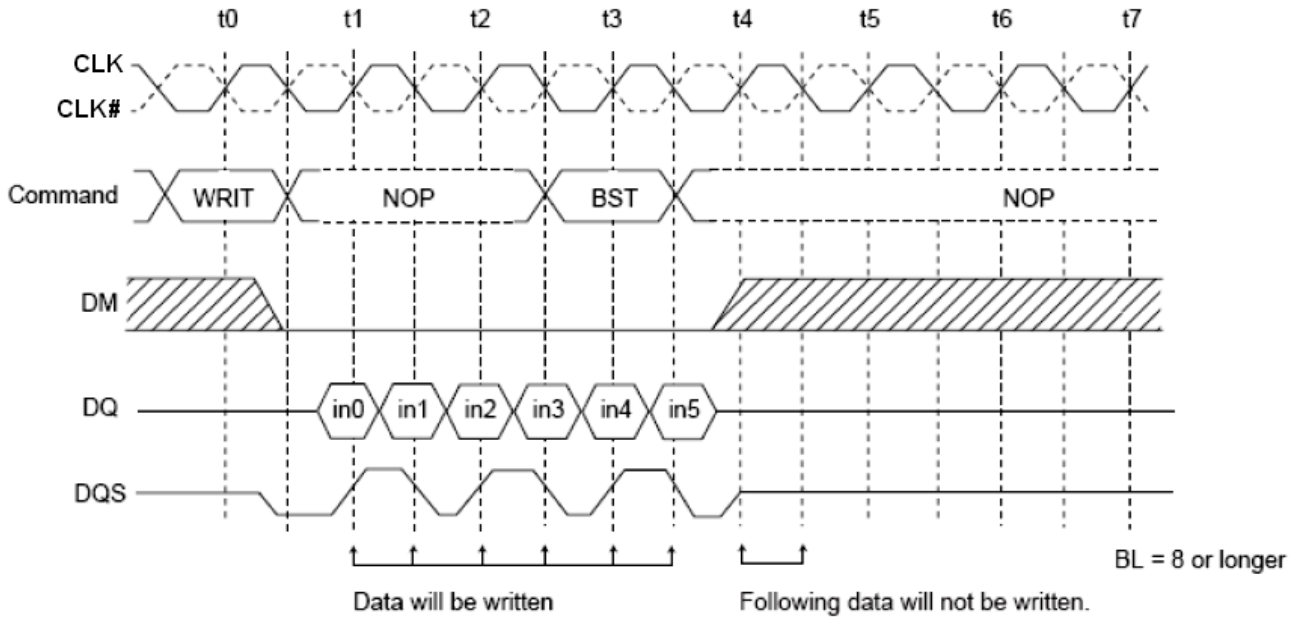
WRITE to BST Command Interval (Same bank, same ROW address)



[Write to BST delay = 1 clock cycle]



[Write to BST delay = 2 clock cycle]



[Write to BST delay = 3 clock cycle]

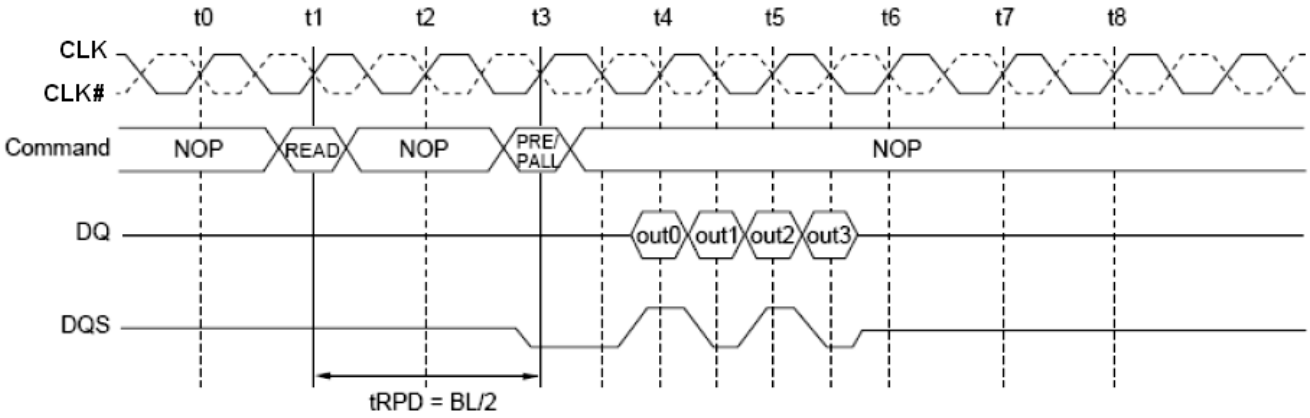
A Read command to the consecutive Precharge command interval

Operation by each case of destination bank of the consecutive Precharge command.

	Bank address	Operation
1	Same	The PRE and PALL command can interrupt a read operation. To complete a burst read operation, t_{RPD} is required between the read and the precharge command. Please refer to the following timing chart.
2	Different	The PRE command does not interrupt a read command. No interval timing is required between the read and the precharge command.

READ to PRECHARGE Command Interval (same bank): To output all data

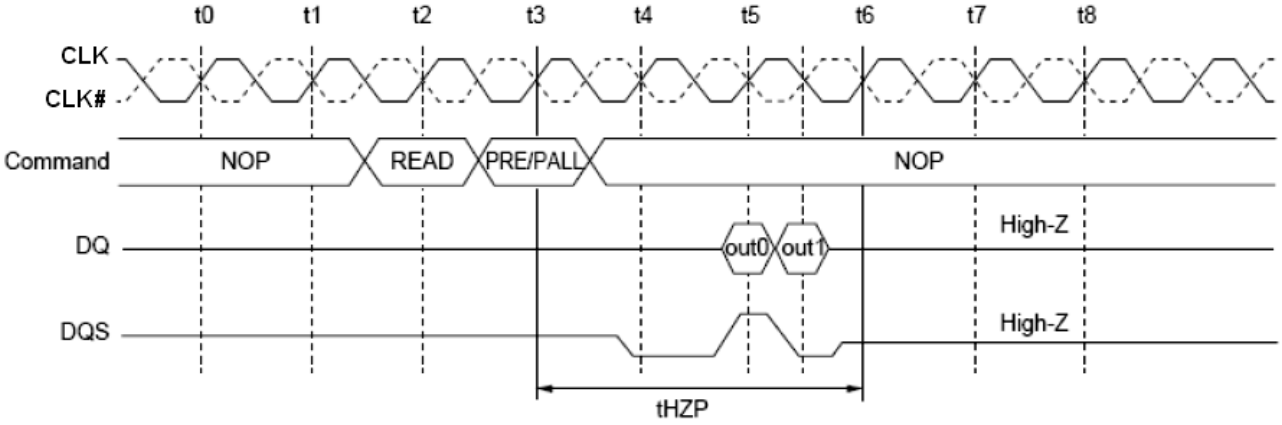
To complete a burst read operation and get a burst length of data, the consecutive precharge command must be issued t_{RPD} (= BL/ 2 cycles) after the read command is issued.



READ to PRECHARGE Command Interval (same bank): To output all data (CL=3, BL=4)

READ to PRECHARGE Command Interval (same bank): To stop output data

A burst data output can be interrupted with a precharge command. All DQ pins and DQS pins become high-Z t_{HZP} (= CL) after the precharge command.



READ to PRECHARGE Command Interval (same bank): To stop output data (CL=3, BL=4, 8)

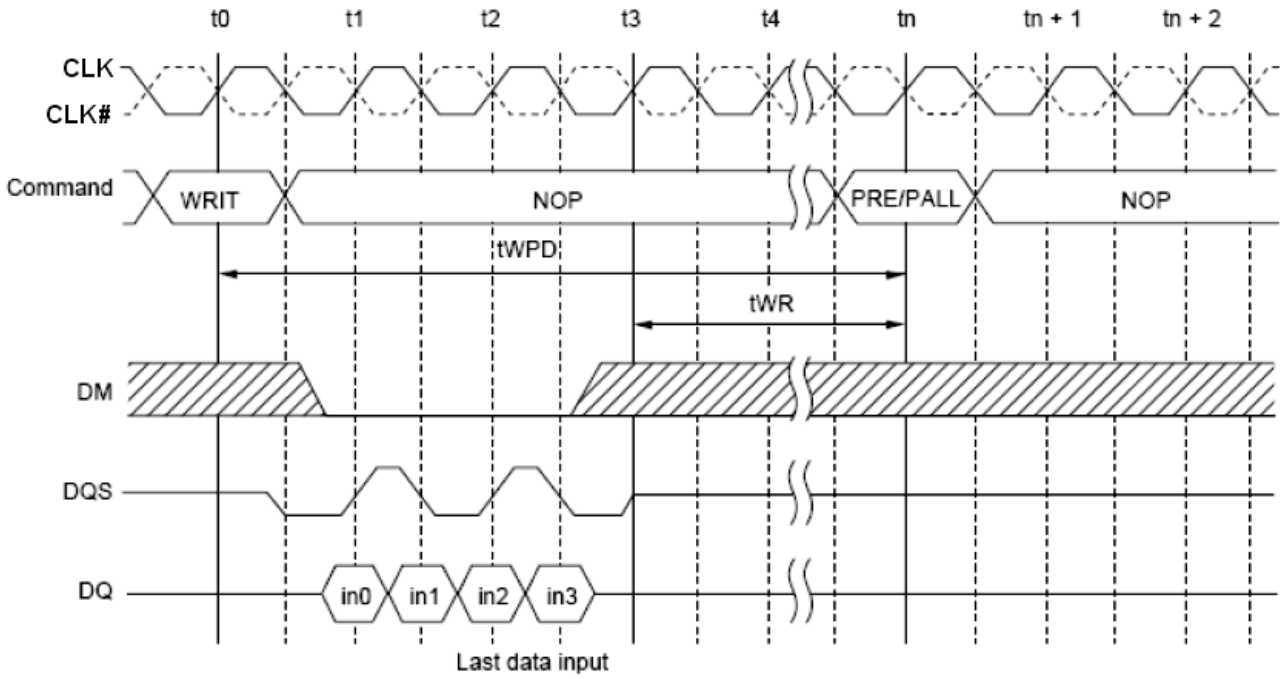
A Write command to the consecutive Precharge command interval (same bank)

Operation by each case of destination bank of the consecutive Precharge command.

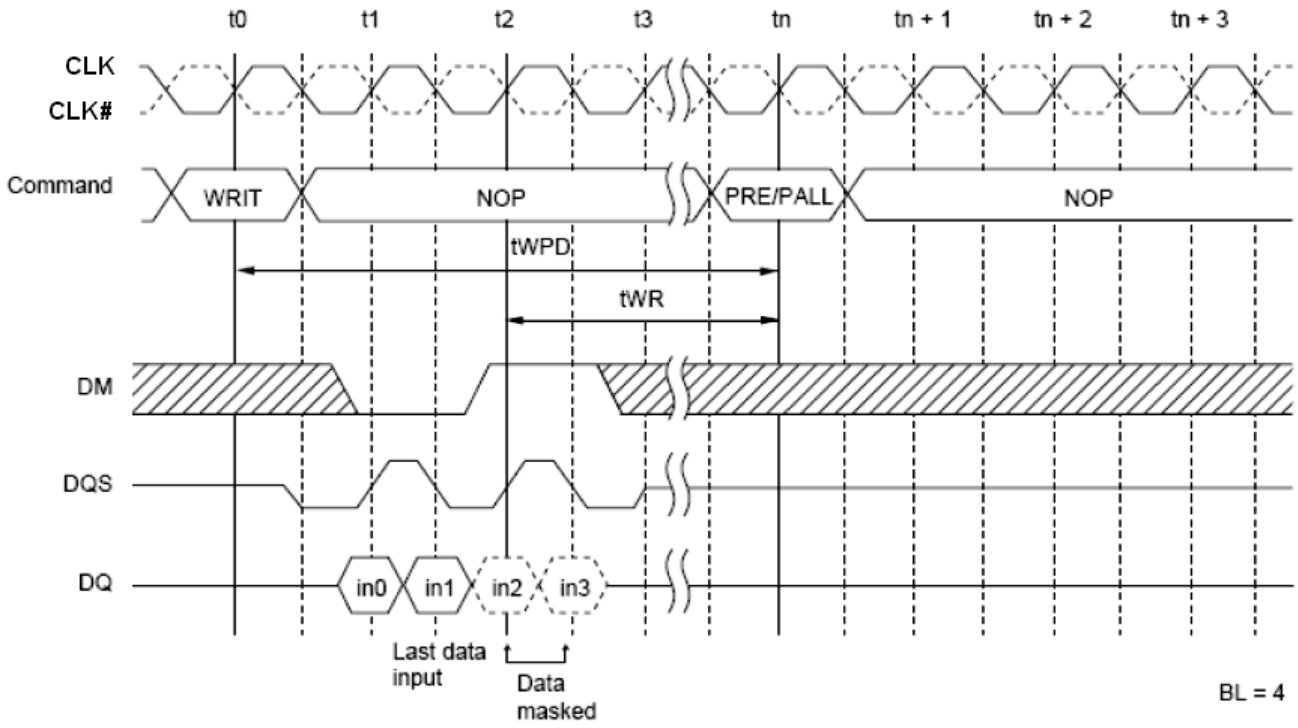
	Bank address	Operation
1	Same	The PRE and PALL command can interrupt a write operation. To complete a burst write operation, t_{WPD} is required between the write and the precharge command. Please refer to the following timing chart.
2	Different	The PRE command does not interrupt a write command. No interval timing is required between the write and the precharge command.

Write to Precharge command interval (same bank)

The minimum interval t_{WPD} is necessary between the write command and the precharge command.



Write to Precharge command interval (same bank) (BL=4)

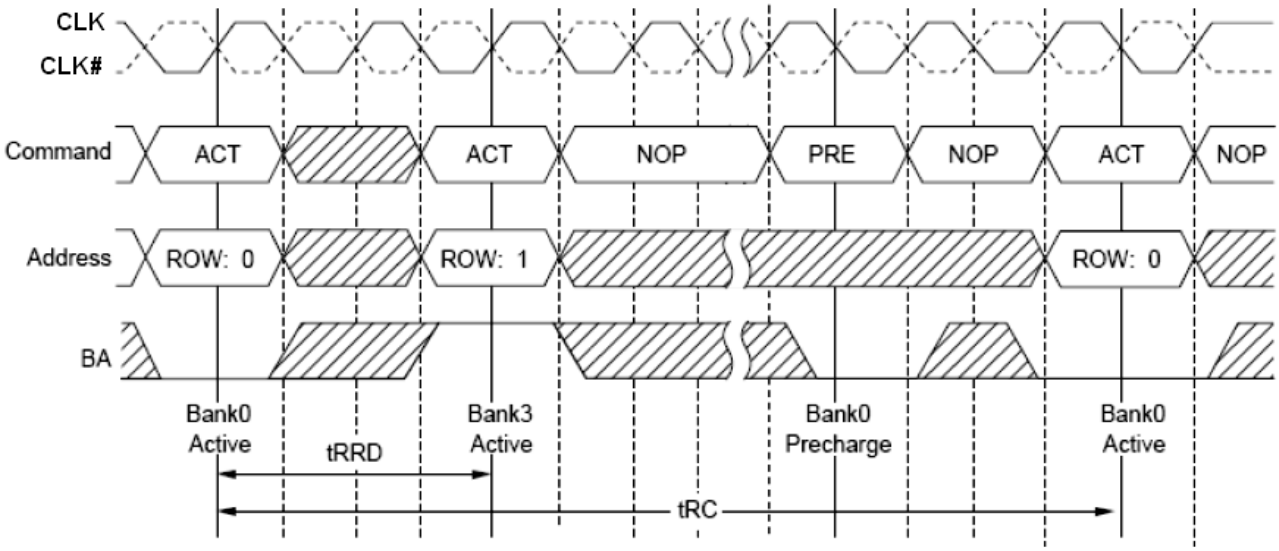


Write to Precharge command interval (same bank) (BL=4, DM to mask data)

Bank active command interval

Destination row of the consecutive ACT command

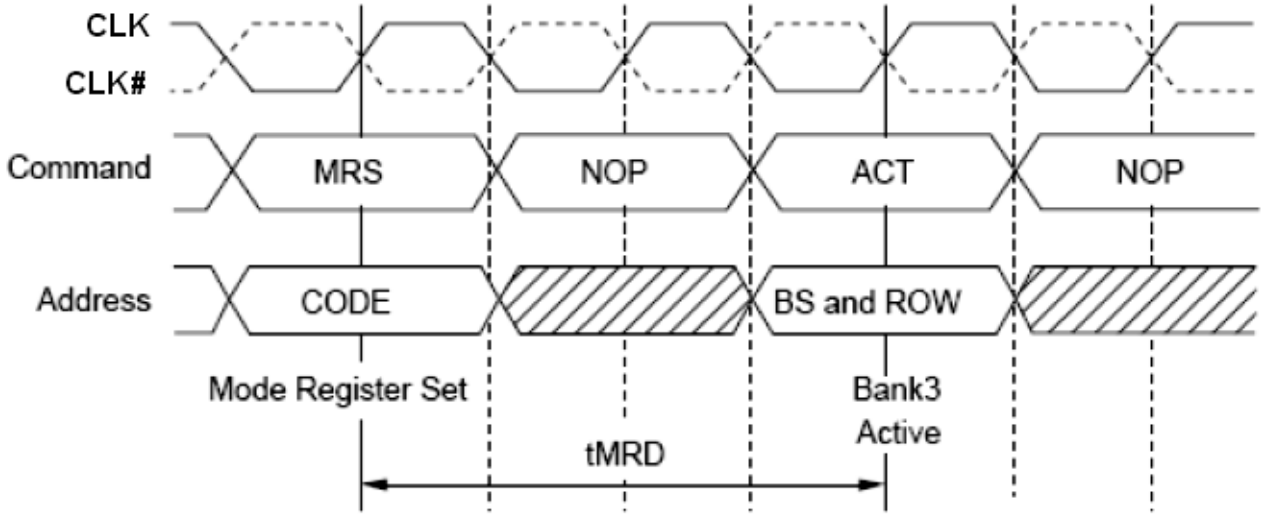
	Bank address	Row Address	Status	Operation
1	Same	Any	ACTIVE	Two successive ACT commands can be issued at t_{RC} interval. In between two successive ACT operations, precharge command should be executed.
2	Different	Any	ACTIVE	Precharge the bank. t_{RP} after the precharge command, the consecutive ACT command can be issued.
			IDLE	t_{RRD} after an ACT command, the next ACT command can be issued.



Bank Active to Bank Active

Mode register set to Bank-active command interval

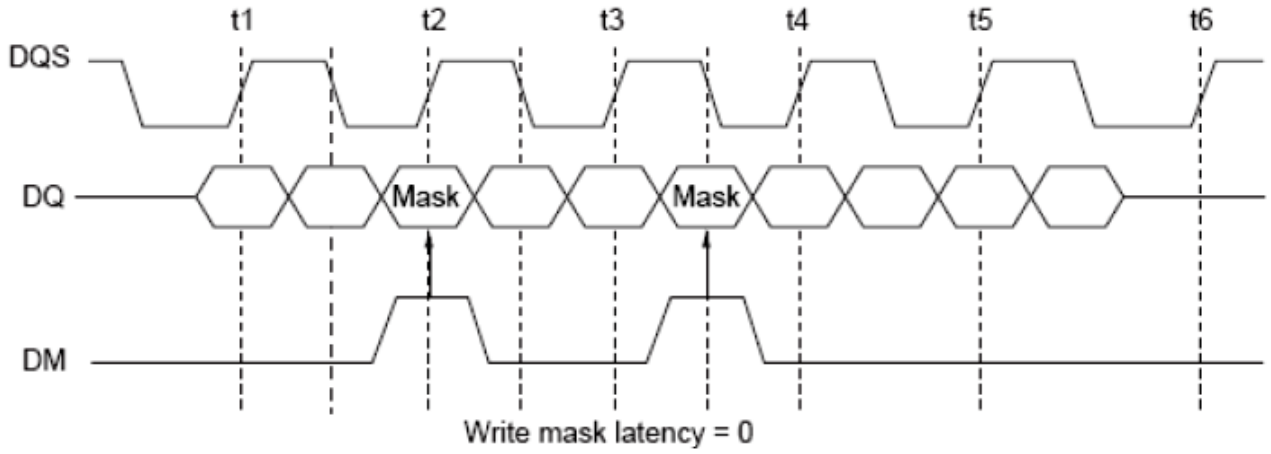
The interval between setting the mode register and executing a bank-active command must be no less than t_{MRD}.



Mode Register Set to Bank Active

DM Control

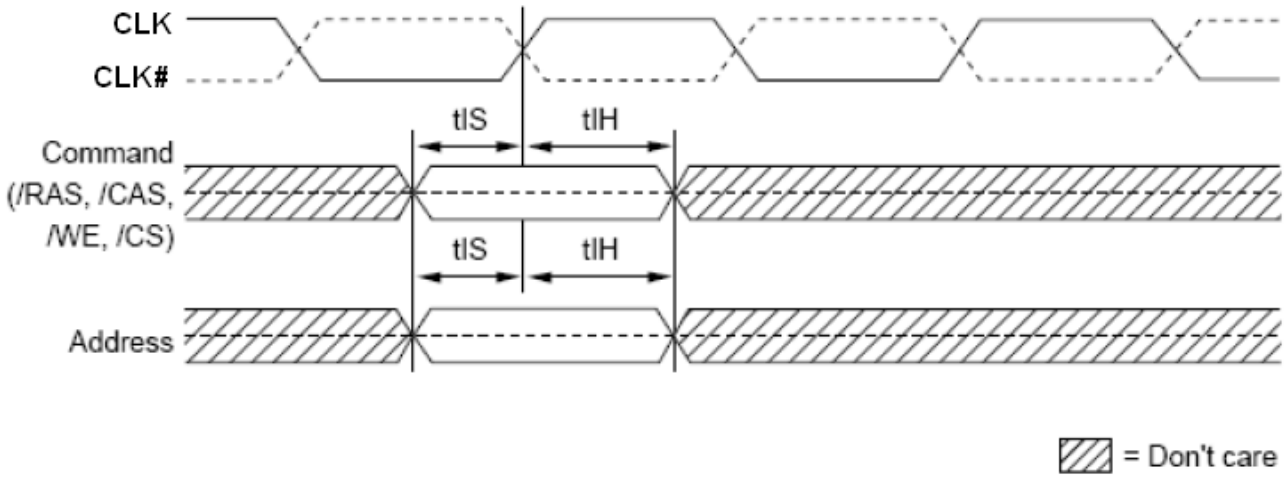
DM can mask input data. By setting DM to low, data can be written. UDM and LDM can mask the upper and lower byte of input data, respectively. When DM is set to high, the corresponding data is not written, and the previous data is held. The latency between DM



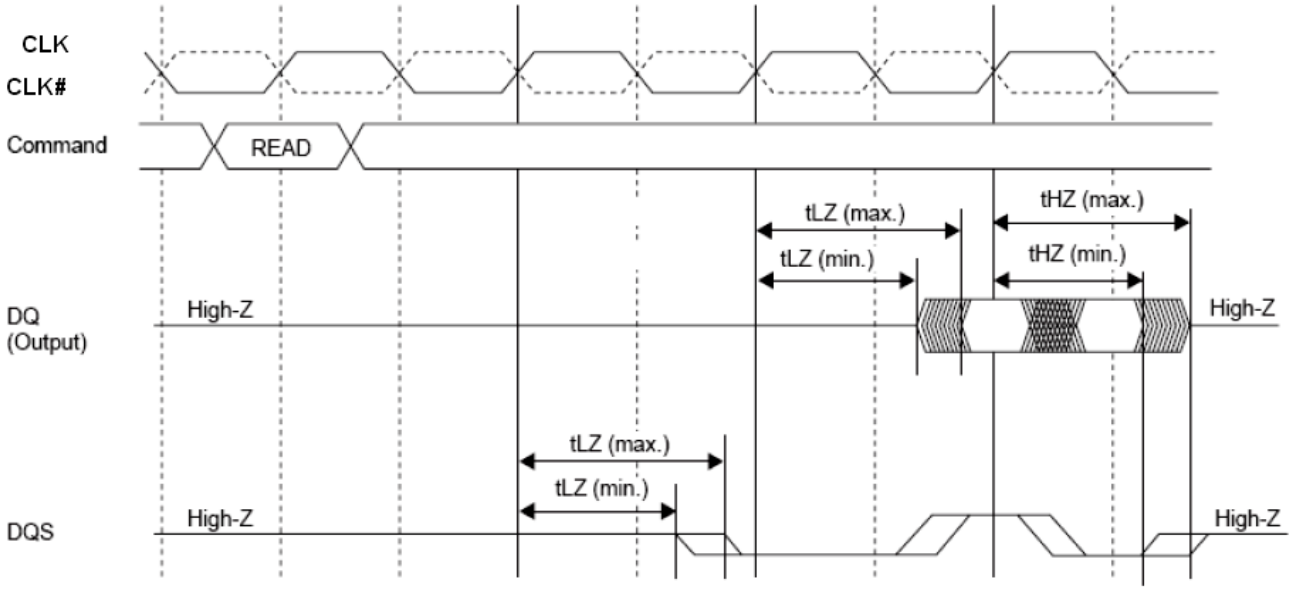
DM Control

Timing Waveforms

Command and Addresses Input Timing Definition

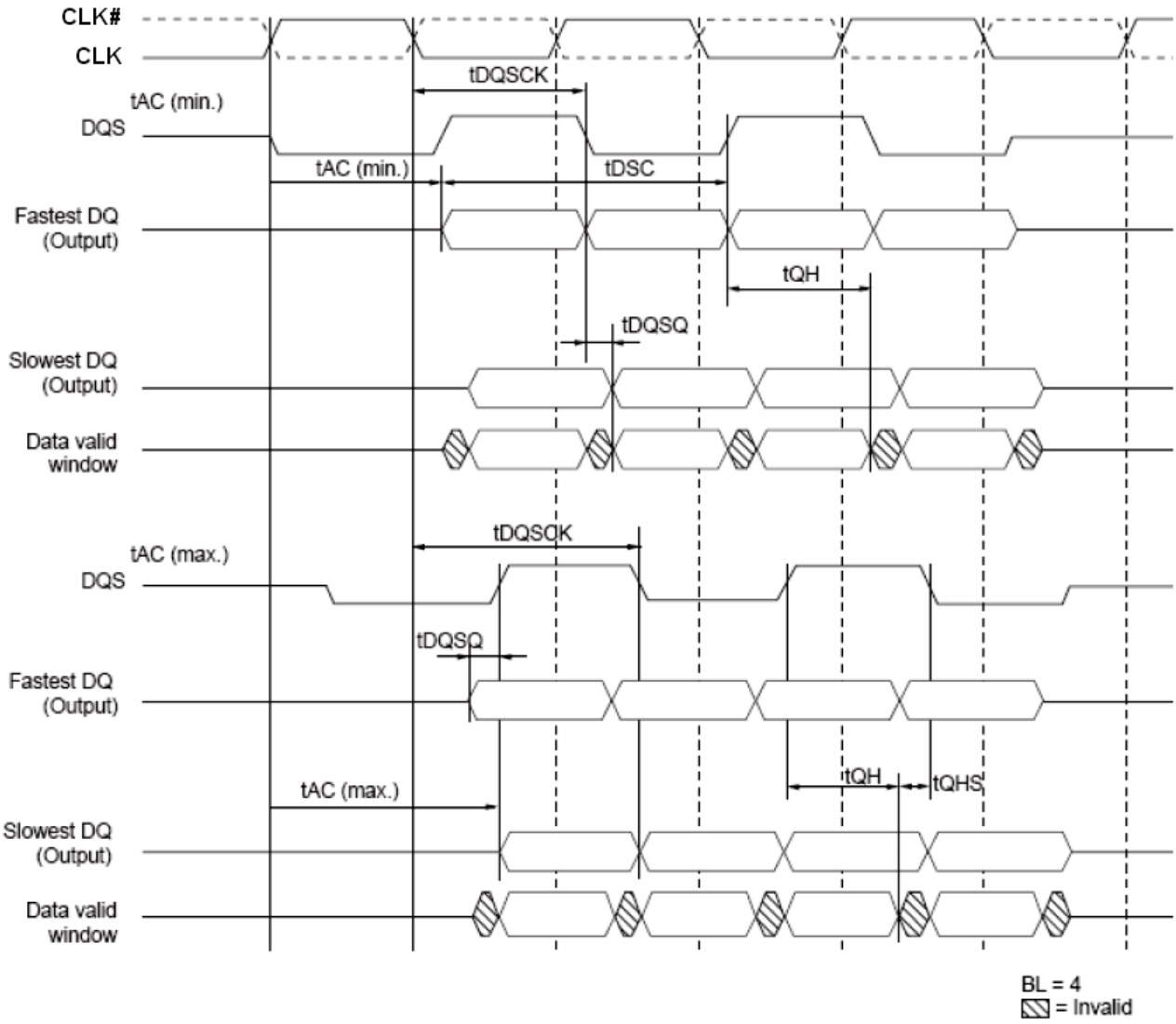


Read Timing Definition (1)

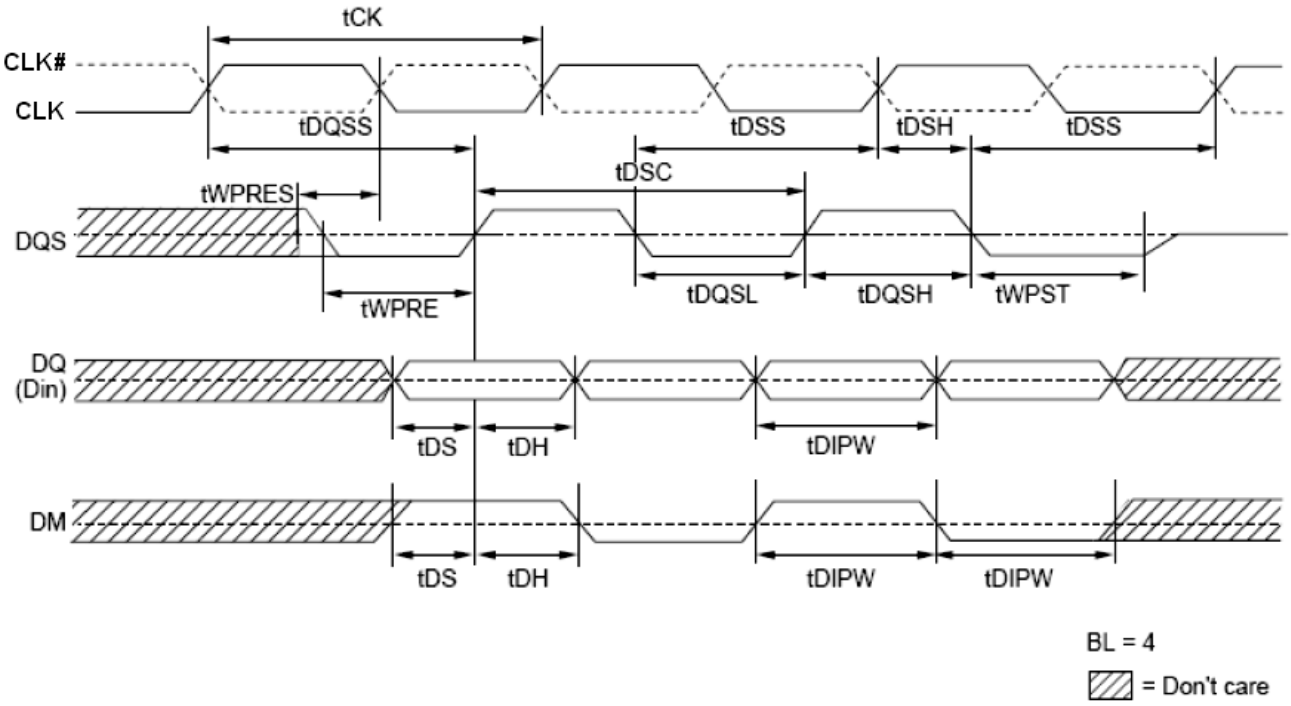


CL = 3
BL = 2

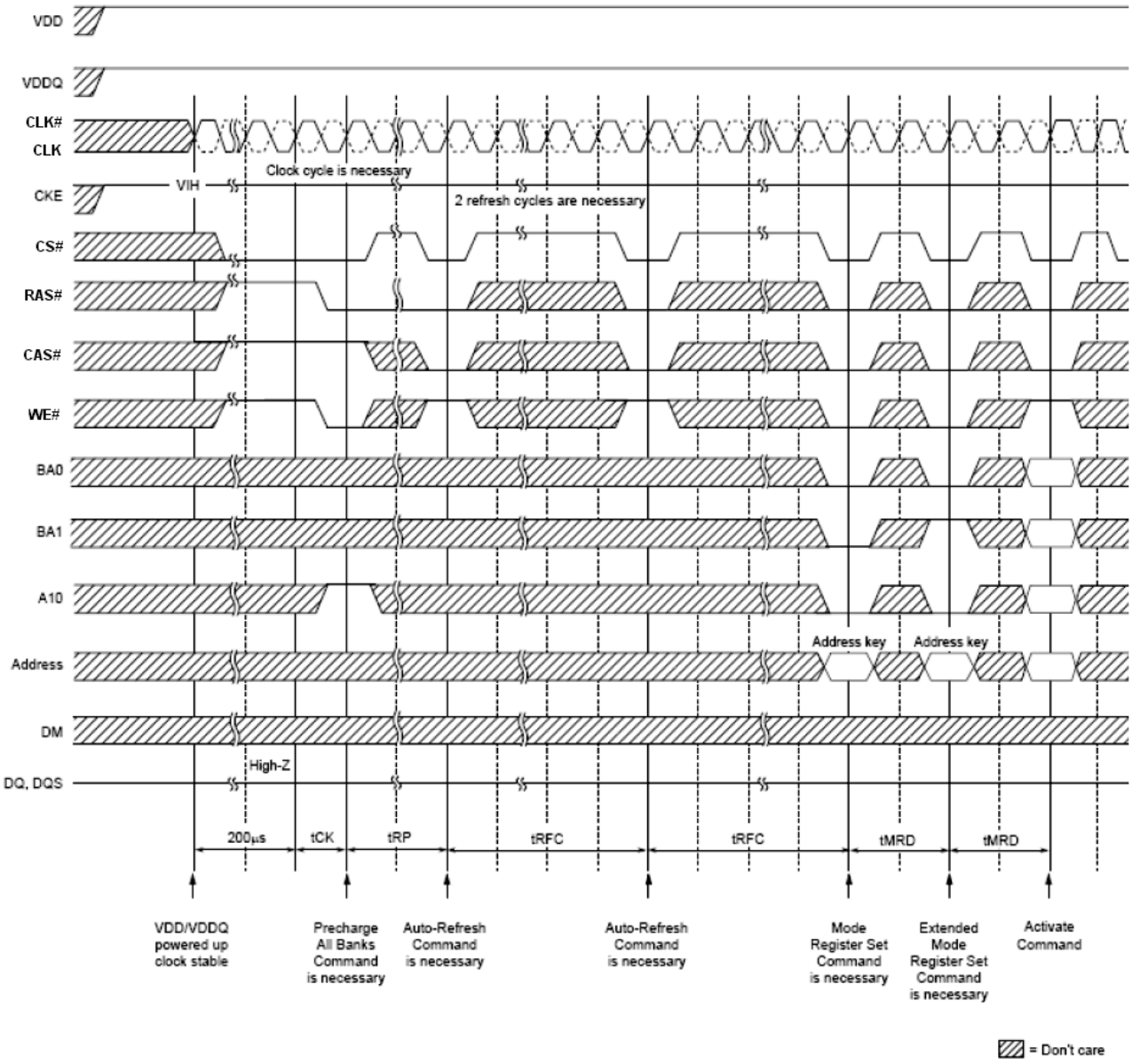
Read Timing Definition (2)



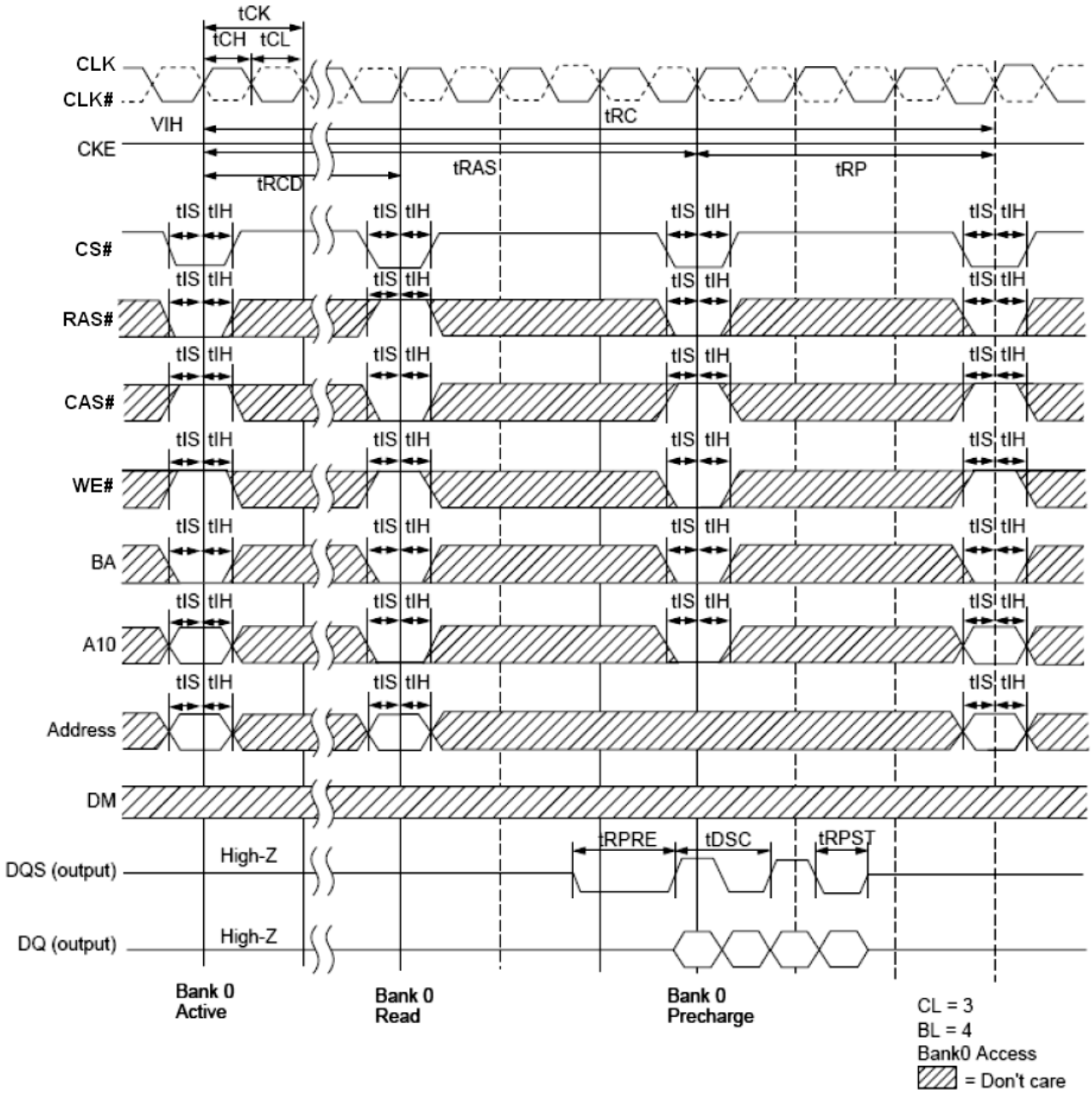
Write Timing Definition



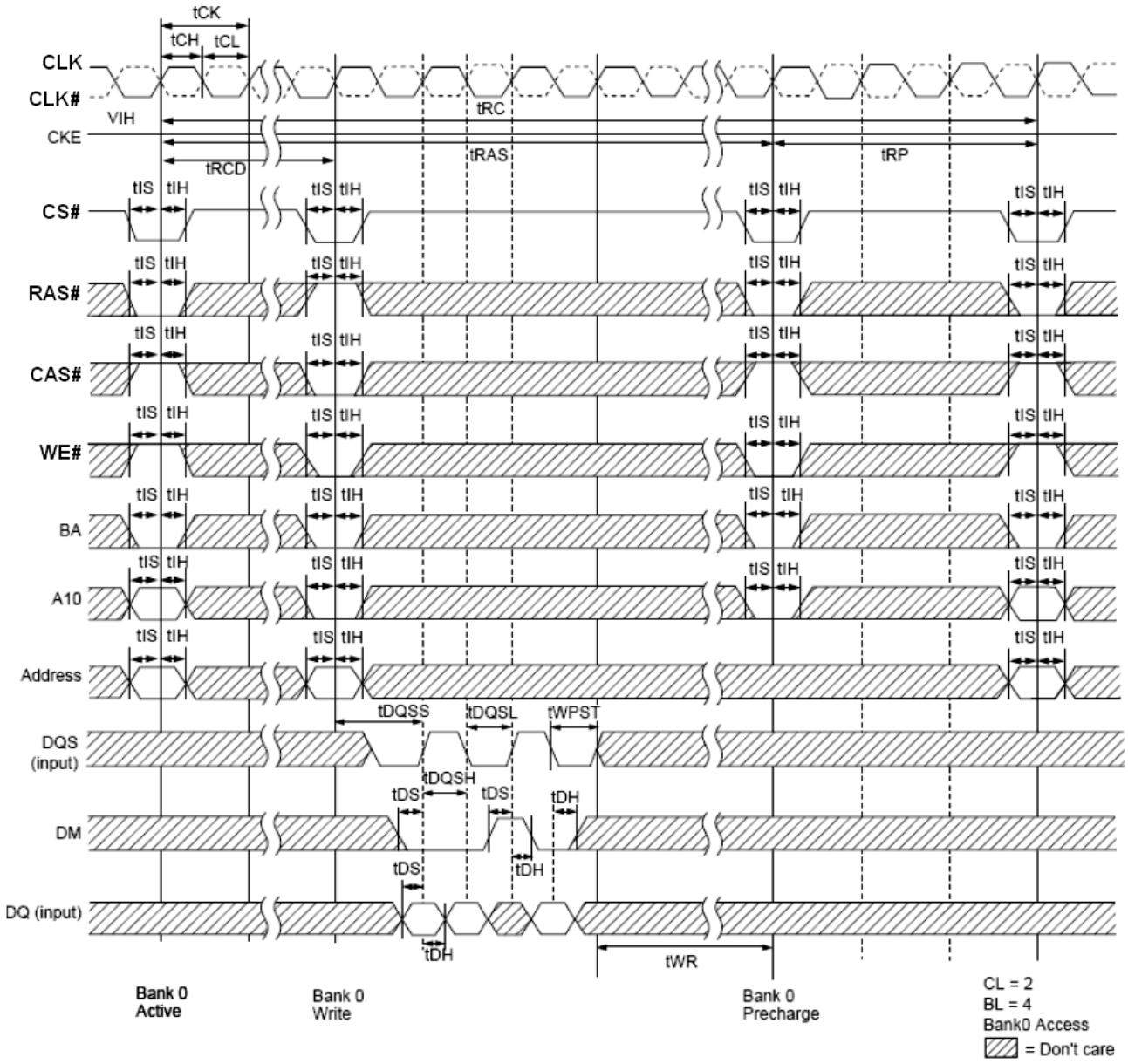
Initialization Sequence



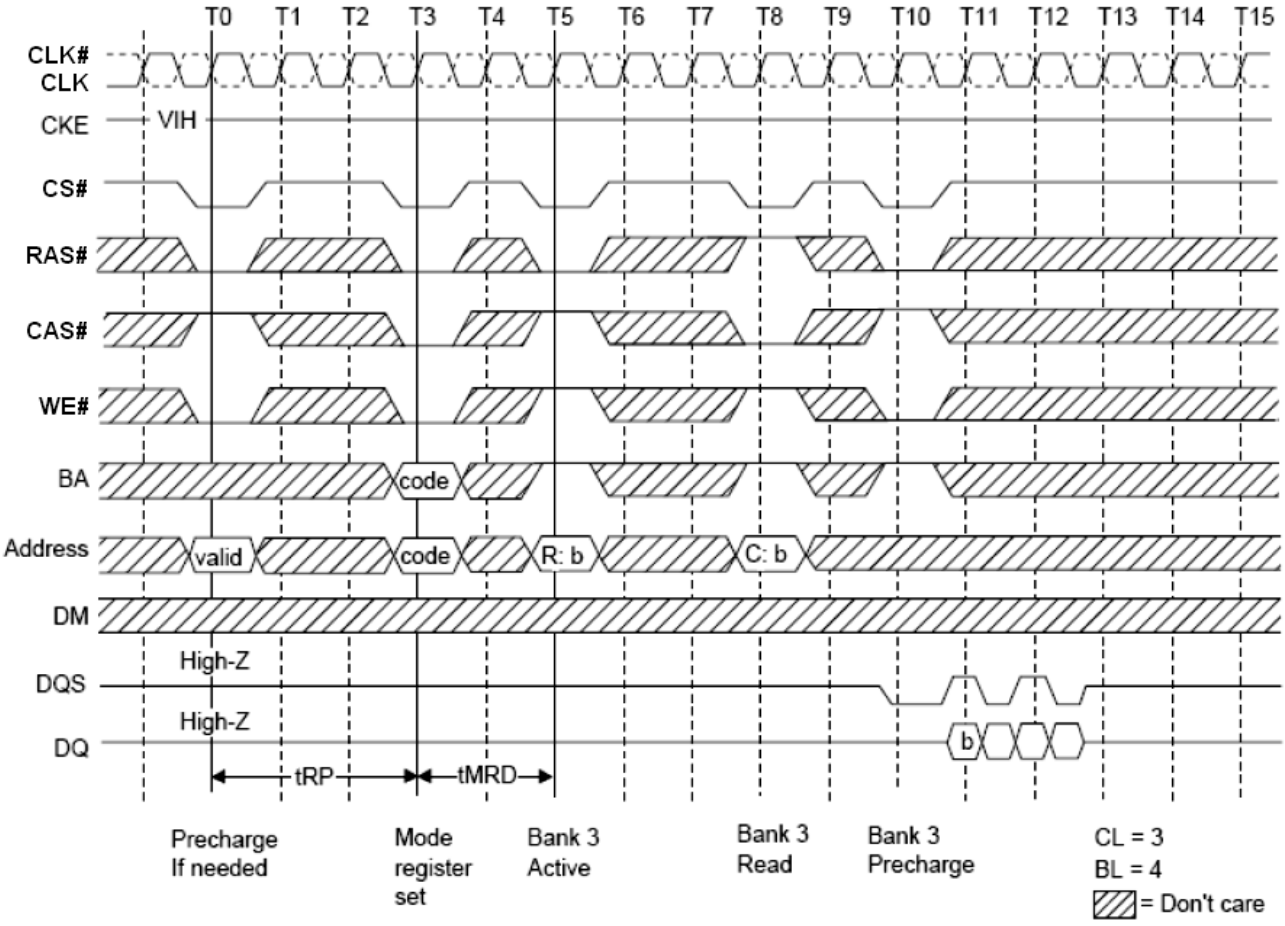
Read Cycle



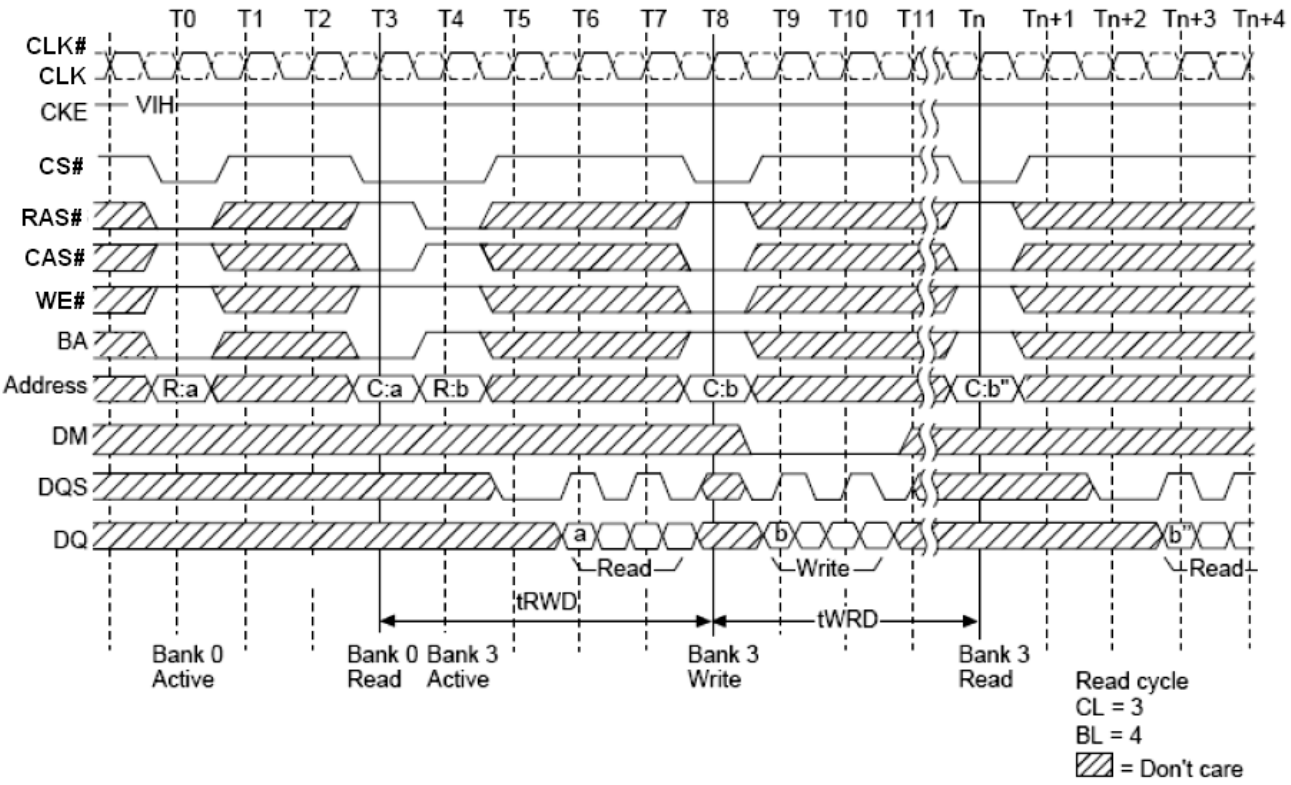
Write Cycle



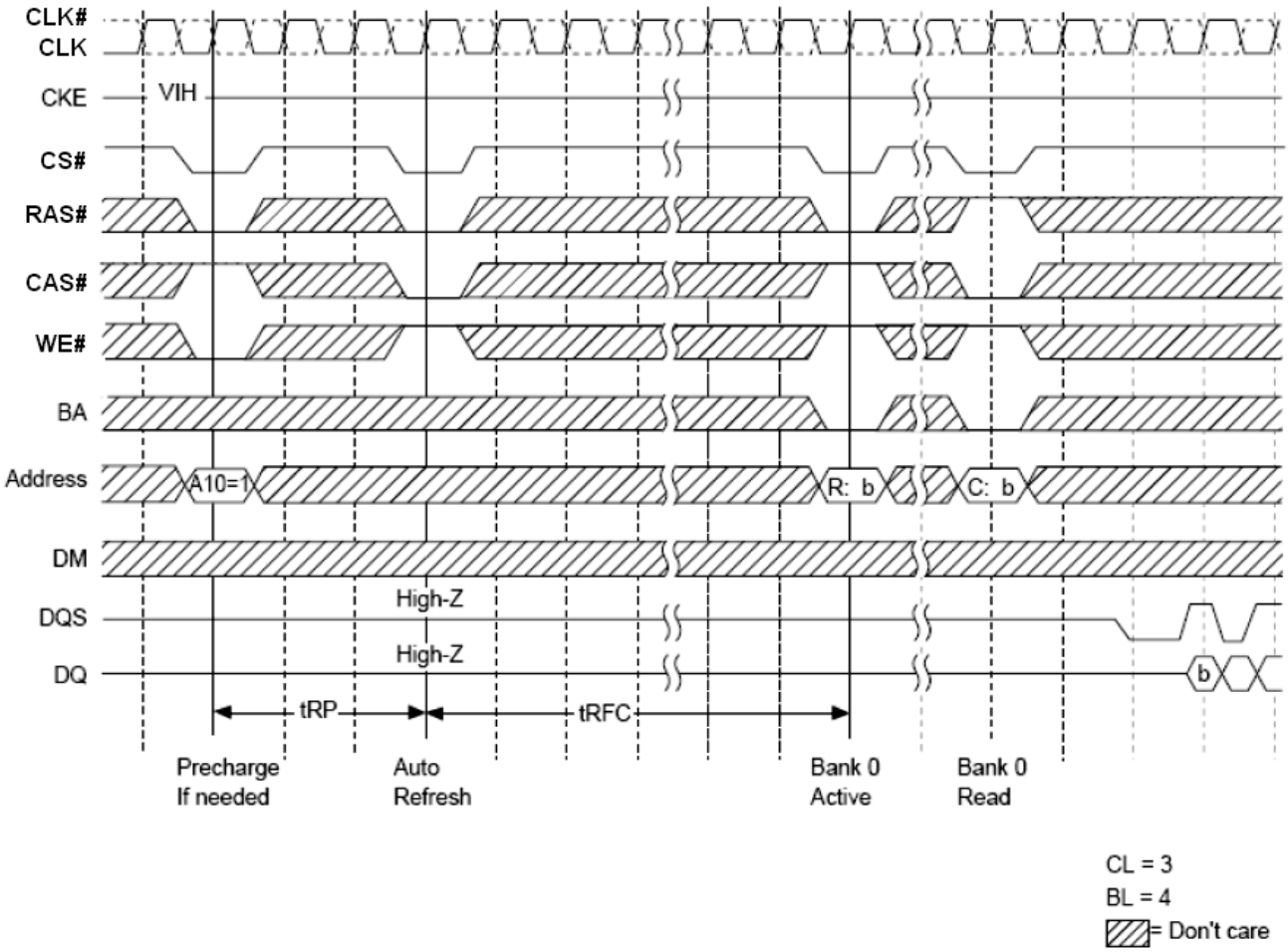
Mode Register Set Cycle



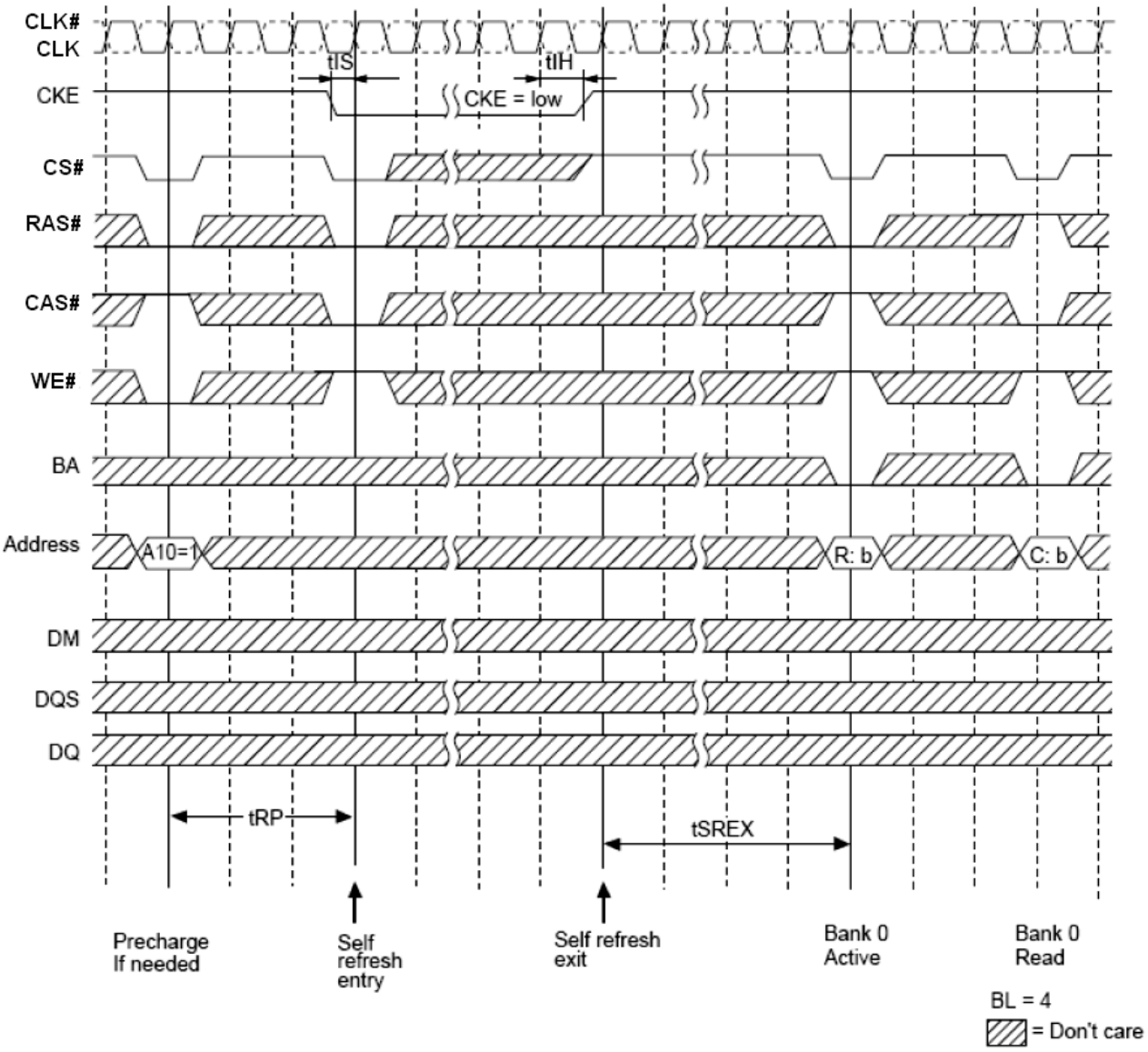
Read/Write Cycle



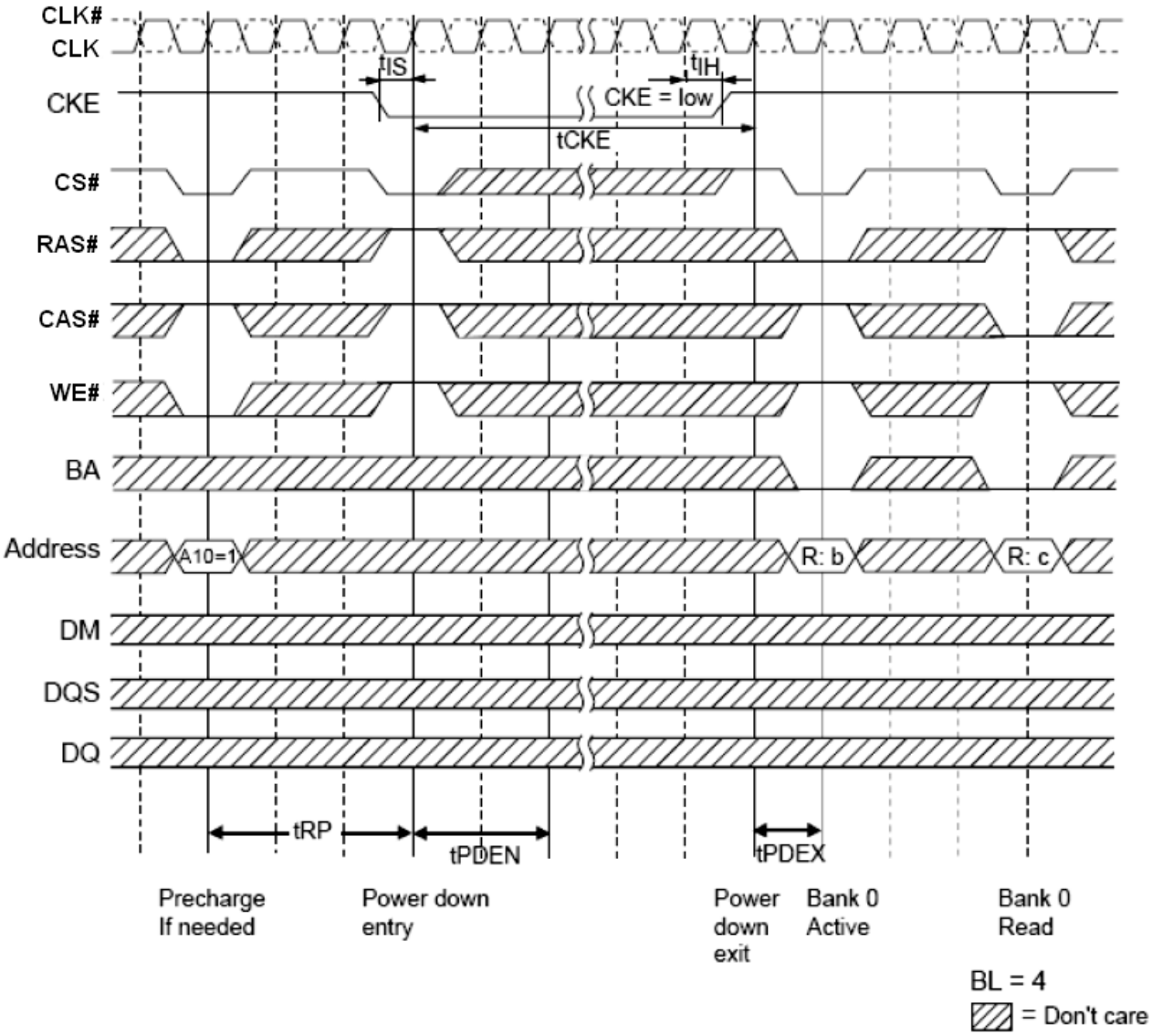
Auto-Refresh Cycle



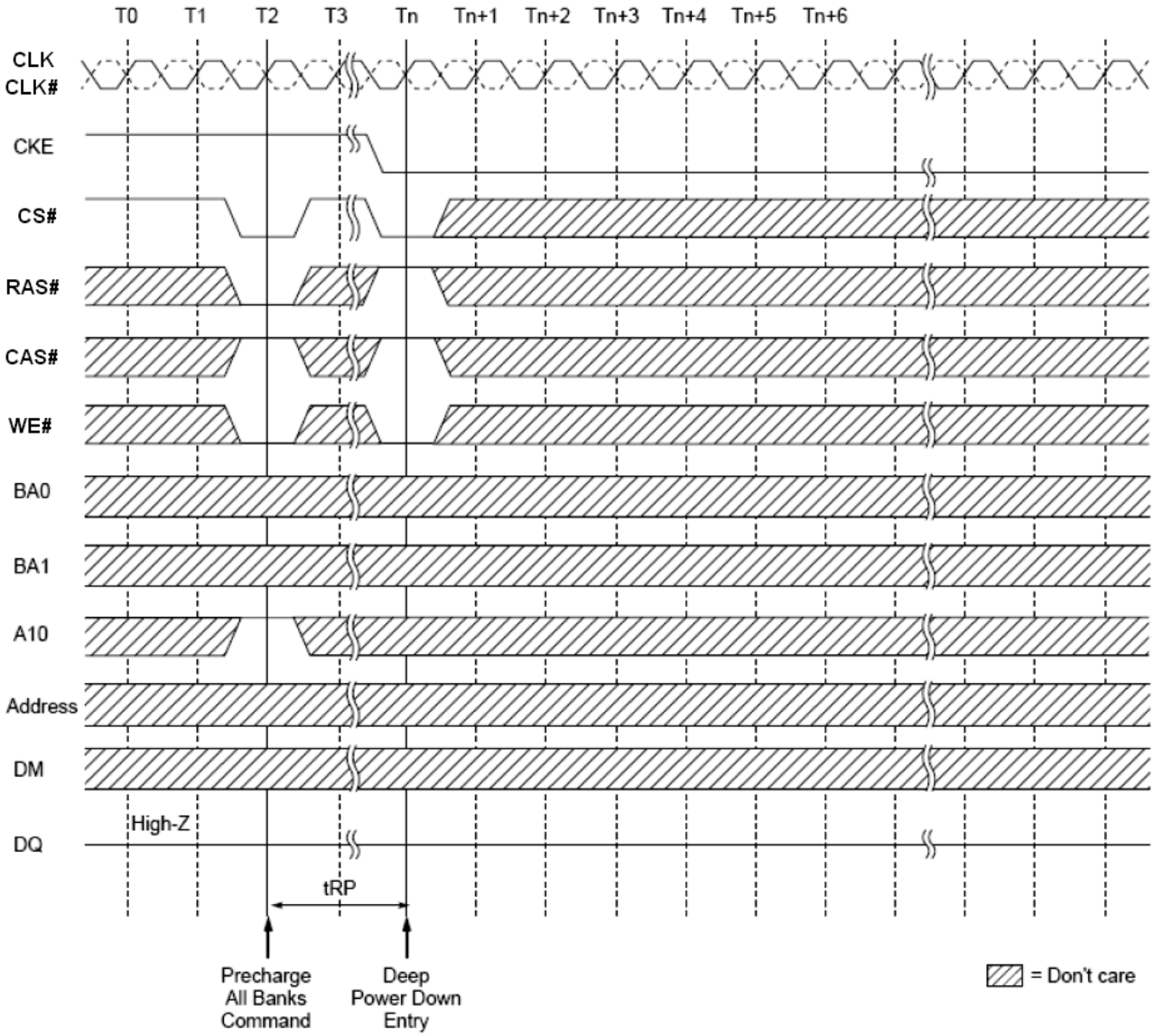
Self-Refresh Cycle



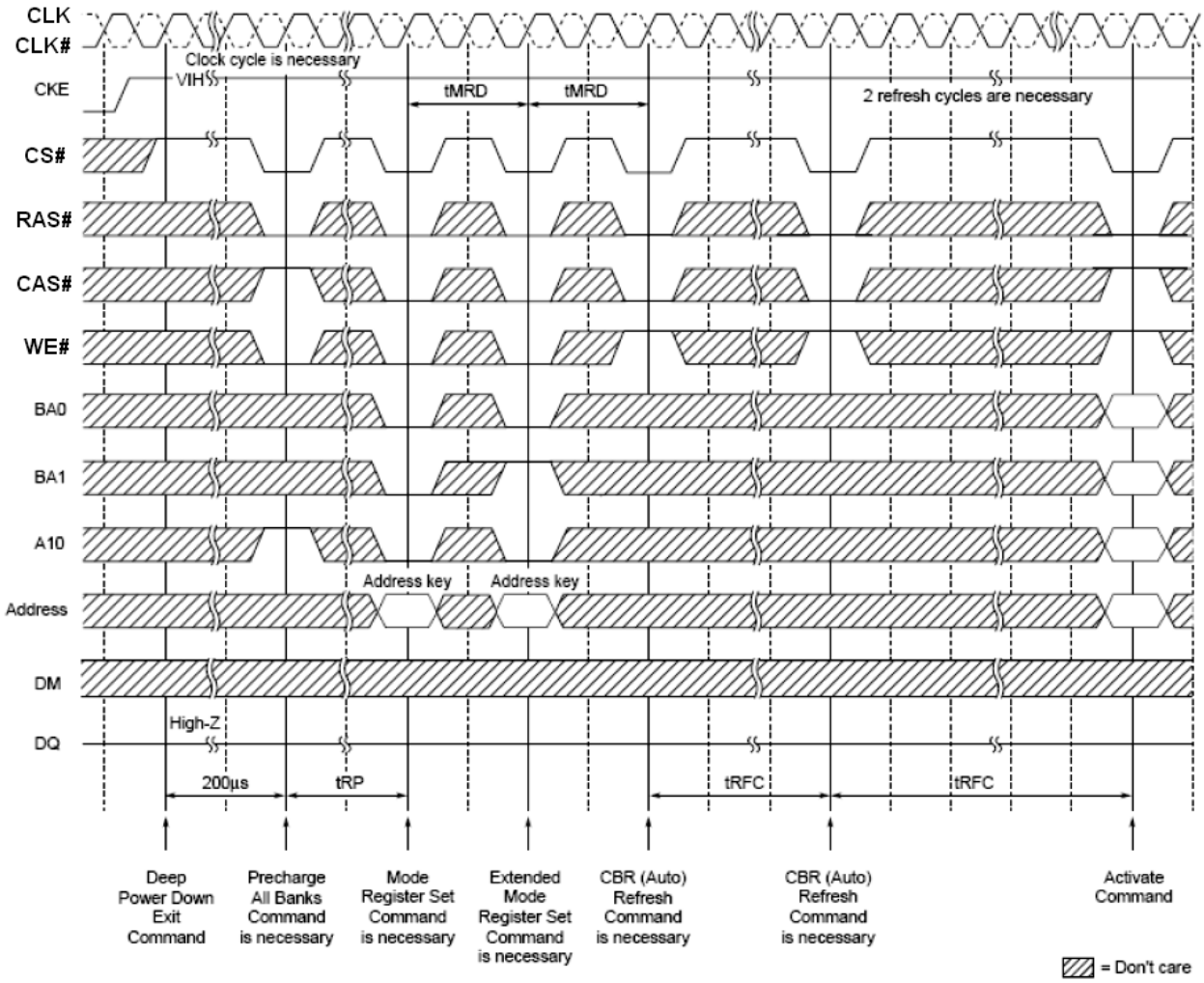
Power-Down Entry and Exit



Deep Power-Down Entry



Deep Power-Down Exit



Note:
The sequence of auto-refresh, mode register programming and extended mode register programming above may be transposed.

Revisions List

Revision No	Description	Date
Preliminary 0.0	Initial Release	2012/10/25
A	Update datasheet version from Preliminary 0.0 to A.	2012/12/07