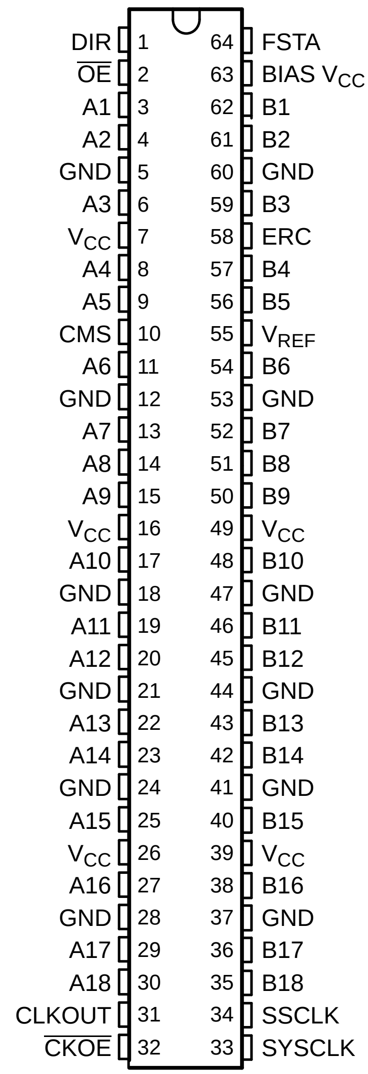
SN74GTLPH1627
18-BIT LVTTL-TO-GTLP BUS TRANSCEIVER WITH SOURCE-SYNCHRONOUS CLOCK OUTPUTS

SCES356C–JUNE 2001–REVISED DECEMBER 2005

FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **TI-OPC™ Circuitry Limits Ringing on Unevenly Loaded Backplanes**
- **OEC™ Circuitry Improves Signal Integrity and Reduces Electromagnetic Interference**
- **Bidirectional Interface Between GTLP Signal Levels and LVTTL Logic Levels**
- **GTLP Buffered SYSCLK Signal (SSCLK) for Source-Synchronous Applications**
- **LVTTL Interfaces Are 5-V Tolerant**
- **High-Drive GTLP Outputs (100 mA)**
- **LVTTL Outputs (–24 mA/24 mA)**
- **GTLP Rise and Fall Times Designed for Optimal Data-Transfer Rate and Signal Integrity in Distributed Loads**
- **I_{off}, Power-Up 3-State, and BIAS V_{CC} Support Live Insertion**
- **Bus Hold on A-Port Data Inputs**
- **Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**
  - **– 1000-V Charged-Device Model (C101)**

DGG PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74GTLPH1627DGGR	GTLPH1627

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74GTLPH1627 is a high-drive, 18-bit bus transceiver that provides LVTTL-to-GTLP and GTLP-to-LVTTL signal-level translation. The device allows for transparent and latched modes of data transfer. Additionally, with the use of the clock-mode select (CMS) input, the device can be used in source-synchronous and clock-synchronous applications. Source-synchronous applications require the skew between the clock output and data output to be minimized for optimum maximum-frequency system performance. In order to reduce this skew, a flexible setup time adjustment (FSTA) feature is incorporated into the device that sets a predetermined delay between the clock and data. The CMS and direction (DIR) inputs control the mode of the device. The system clock (SYSCLK) and CLKOUT pins are LVTTL compatible, while the source synchronous I/O is GTLP compatible. The benefits include compensation for output-to-output skew coming from the driver itself, and compensation for process skew if more than one driver is used. The device provides a high-speed interface between cards operating at LVTTL logic levels and a backplane operating at GTLP signal levels. High-speed (about three times faster than standard TTL or LVTTL) backplane operation is a direct result of GTLP's reduced output swing (<1 V), reduced input threshold levels, improved differential input, OEC™ circuitry, and TI-OPC™ circuitry. Improved GTLP OEC and TI-OPC circuits minimize bus-settling time and have been designed and tested using several backplane models. The high drive allows incident-wave switching in heavily loaded backplanes, with equivalent load impedance down to 11 Ω.

GTLP is the Texas Instruments derivative of the Gunning Transceiver Logic (GTL) JEDEC standard JESD 8-3. The ac specification for the SN74GTLPH1627 is given only at the preferred higher noise-margin GTLP, but the user has the flexibility of using this device at either GTL (V_{TT} = 1.2 V and V_{REF} = 0.8 V) or GTLP (V_{TT} = 1.5 V and V_{REF} = 1 V) signal levels. For information on using GTLP devices in FB+/BTL applications, refer to TI application reports, *Texas Instruments GTLP Frequently Asked Questions*, literature number SCEA019, and *GTLP in BTL Applications*, literature number SCEA017.

Normally, the B port operates at GTLP signal levels. The A-port and control inputs operate at LVTTL logic levels, but are 5-V tolerant and are compatible with TTL and 5-V CMOS inputs. V_{REF} is the B-port differential input reference voltage.

This device is fully specified for live-insertion applications using I_{off}, power-up 3-state, and BIAS V_{CC}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict. The BIAS V_{CC} circuitry precharges and preconditions the B-port input/output connections, preventing disturbance of active data on the backplane during card insertion or removal, and permits true live-insertion capability.

This GTLP device features TI-OPC circuitry, which actively limits the overshoot caused by improperly terminated backplanes, unevenly distributed cards, or empty slots during low-to-high signal transitions. This improves signal integrity, which allows adequate noise margin to be maintained at higher frequencies.

High-drive GTLP backplane interface devices feature adjustable edge-rate control (ERC). Changing the ERC input voltage between low and high adjusts the B-port output rise and fall times. This allows the designer to optimize system data-transfer rate and signal integrity to the backplane load.

Active bus-hold circuitry holds unused or undriven LVTTL data inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTIONAL DESCRIPTION

The SN74GTLPH1627 is a high-drive (100 mA), 18-bit bus transceiver containing D-type latches and D-type flip-flops for data-path operation in transparent or latched modes and can replace any of the functions shown in Table 1. Data polarity is noninverting.

Table 1. SN74GTLPH1627 Bus Transceiver Replacement Functions

FUNCTION	8 BIT	9 BIT	10 BIT	16 BIT	18 BIT
Transceiver	'245, '623, '645	'863	'861	'16245, '16623	'16863
Buffer/driver	'241, '244, '541		'827	'16241, '16244, '16541	'16825
Latched transceiver	'543			'16543	'16472
Latch	'373, '573	'843	'841	'16373	'16843
SN74GTLPH1627 bus transceiver replaces all above functions.					

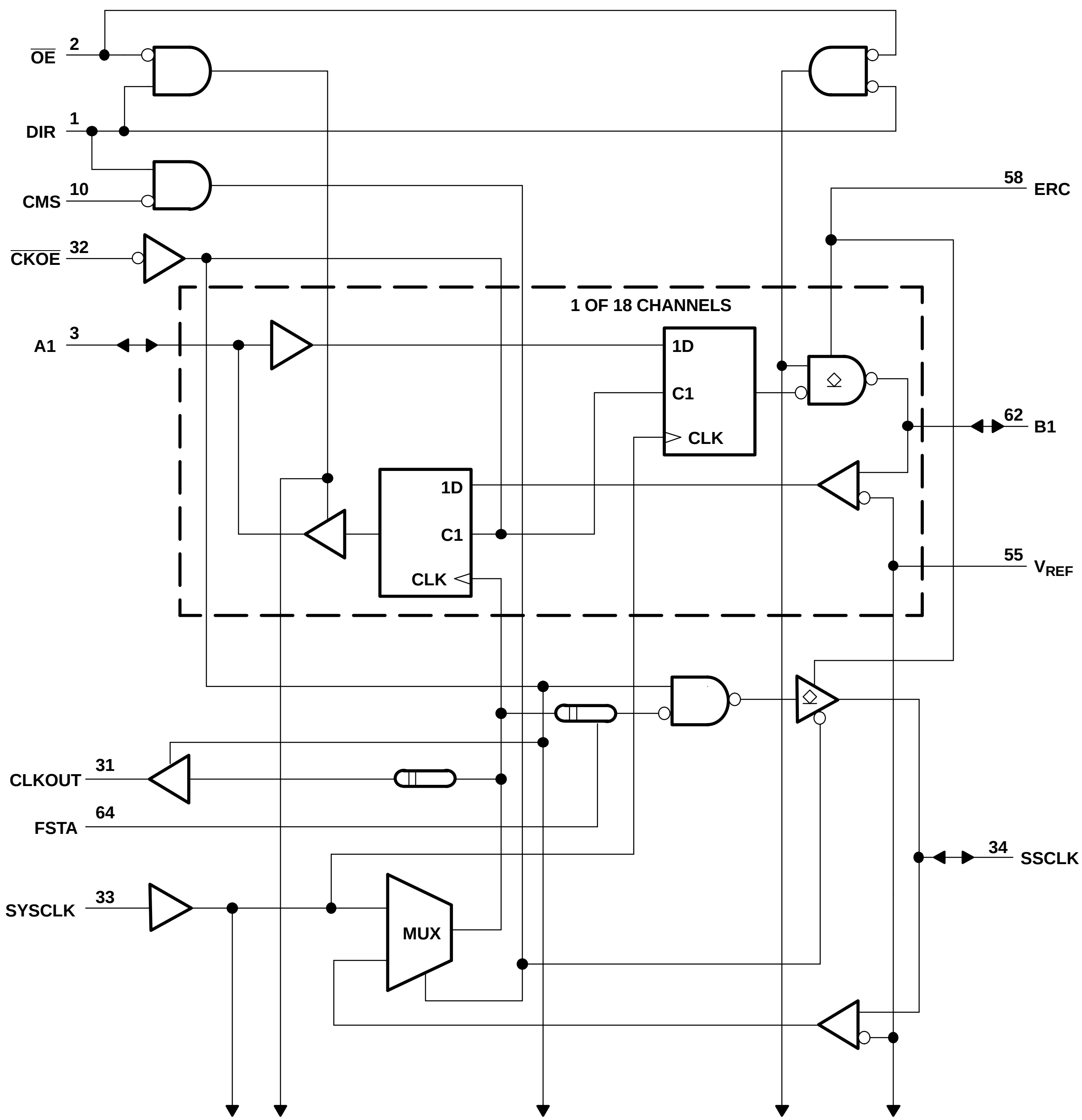
Additionally, the device allows for conversion of the system clock (SYSCLK) to GTLP signal levels (SSCLK) and LVTTL signal levels (CLKOUT). It also provides conversion of a GTLP source-synchronous clock to LVTTL signal levels (CLKOUT).

The device allows for conversion of the LVTTL system clock (SYSCLK) to GTLP (SSCLK) and LVTTL (CLKOUT) signal levels when used as the transmitter, and GTLP source-synchronous clock (SSCLK) to LVTTL (CLKOUT) signal levels when used as the receiver in source-synchronous applications. Source-synchronous operation removes time-of-flight restrictions and allows for increased data throughput. CMS is used to switch between system-synchronous mode and clock-synchronous mode. The clock output-enable ($\overline{\text{CKOE}}$) input is used to switch between latched and transparent mode.

Data flow in each direction is controlled by $\overline{\text{CKOE}}$, clock (SYSCLK or SSCLK), direction (DIR), and $\overline{\text{OE}}$. $\overline{\text{OE}}$ controls the 18 bits of data. The CLKOUT/SSCLK buffered clock path for the A-to-B and B-to-A directions is controlled by $\overline{\text{CKOE}}$. In the data isolation mode ($\overline{\text{OE}}$ high, $\overline{\text{CKOE}}$ low), A data may be stored in one register and/or B data may be stored in the other register.

TEXAS INSTRUMENTS
www.ti.com

LOGIC DIAGRAM (POSITIVE LOGIC)



FUNCTION TABLES

A-TO-B DIRECTION

INPUTS						OUTPUTS			MODE	
$\overline{CKOE}$	$\overline{OE}$	CMS	DIR	SYSCLK	A	SSCLK	CLKOUT	B		
L	L	X	L	H or L	X	SYSCLK	SYSCLK	B_0	Latched storage of A	Source synchronous
L	L	X	L	↑	L	SYSCLK	SYSCLK	L	Clocked storage of A	
L	L	X	L	↑	H	SYSCLK	SYSCLK	H		
L	H	X	L	X	X	SYSCLK	SYSCLK	Z	Data isolation	
H	L	X	L	X	L	Z	Z	L	Transparent transmission of A	
H	L	X	L	X	H	Z	Z	H		
H	H	X	X	X	X	Z	Z	Z	Isolation	
L	H	H	X	↑	X	SYSCLK	SYSCLK	Z	Transmit SYSCLK	
L	H	H	X	H or L	X	SYSCLK	SYSCLK	Z		

B-TO-A DIRECTION

INPUTS							OUTPUTS			MODE	
$\overline{CKOE}$	$\overline{OE}$	CMS	DIR	SYSCLK	SSCLK	B	SSCLK	CLKOUT	A		
L	L	L	H	X	H or L	X	Input	SSCLK	A_0	Latched storage of B	Source synchronous
L	L	L	H	X	↑	L	Input	SSCLK	L	Clocked storage of B	
L	L	L	H	X	↑	H	Input	SSCLK	H		
L	H	L	H	X	X	X	Input	SSCLK	Z	Data isolation	
L	L	H	H	H or L	Output	X	SYSCLK	SYSCLK	A_0	Latched storage of B	Clock synchronous
L	L	H	H	↑	Output	L	SYSCLK	SYSCLK	L	Clocked storage of B	
L	L	H	H	↑	Output	H	SYSCLK	SYSCLK	H		
L	H	H	H	X	Output	X	SYSCLK	SYSCLK	Z	Data isolation	
H	L	X	H	X	Output	L	Z	Z	L	Transparent transmission of B	
H	L	X	H	X	Output	H	Z	Z	H		
H	H	X	X	X	Output	X	Z	Z	Z	Isolation	
L	H	L	X	X	↑	X	Input	SSCLK	Z	Receive SSCLK	
L	H	L	X	X	H or L	X	Input	SSCLK	Z		

OUTPUT EDGE-RATE CONTROL (ERC)

INPUT ERC LOGIC LEVEL	OUTPUT B-PORT EDGE RATE
H	Slow
L	Fast

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC} BIAS V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)	A-port and control inputs	–0.5	7	V
		B port and V_{REF}	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	7	V
		B port	–0.5	4.6	
I_O	Current into any output in the low state	A port		48	mA
		B port		200	
I_O	Current into any A-port output in the high state(3)			48	mA
	Continuous current through each V_{CC} or GND			±100	mA
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
θ_{JA}	Package thermal impedance(4)			55	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions[(1)(2)(3)(4)]

			MIN	NOM	MAX	UNIT
V_{CC} BIAS V_{CC}	Supply voltage		3.15	3.3	3.45	V
V_{TT}	Termination voltage	GTL	1.14	1.2	1.26	V
		GTLP	1.35	1.5	1.65	
V_{REF}	Reference voltage	GTL	0.74	0.8	0.87	V
		GTLP	0.87	1	1.1	
V_I	Input voltage	B port and SSCLK			V_{TT}	V
		Except B port and SSCLK		V_{CC}	5.5	
V_{IH}	High-level input voltage	B port and SSCLK	V_{REF} + 0.05			V
		Except B port and SSCLK	2			
V_{IL}	Low-level input voltage	B port and SSCLK			V_{REF} – 0.05	V
		Except B port and SSCLK			0.8	
I_{IK}	Input clamp current				–18	mA
I_{OH}	High-level output current	A port and CLKOUT			–24	mA
I_{OL}	Low-level output current	A port and CLKOUT			24	mA
		B port and SSCLK			100	
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		20			µs/V
T_A	Operating free-air temperature		–40		85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) Proper connection sequence for use of the B-port I/O precharge feature is GND and BIAS V_{CC} = 3.3 V first, I/O second, and V_{CC} = 3.3 V last, because the BIAS V_{CC} precharge circuitry is disabled when any V_{CC} pin is connected. The control and V_{REF} inputs can be connected anytime, but normally are connected during the I/O stage. If B-port precharge is not required, any connection sequence is acceptable but, generally, GND is connected first.
(3) V_{TT} and R_{TT} can be adjusted to accommodate backplane impedances if the dc-recommended I_{OL} ratings are not exceeded.
(4) V_{REF} can be adjusted to optimize noise margins, but normally is two-thirds V_{TT}. TI-OPC circuitry is enabled in the A-to-B direction and is activated when V_{TT} > 0.7 V above V_{REF}. If operated in the A-to-B direction, V_{REF} should be set to within 0.6 V of V_{TT} to minimize current drain.

Electrical Characteristics

over recommended operating free-air temperature range for GTLP (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[(1)]	MAX	UNIT
V_{IK}		V_{CC} = 3.15 V,	I_I = –18 mA			–1.2	V
V_{OH}	A port and CLKOUT	V_{CC} = 3.15 V to 3.45 V,	I_{OH} = –100 µA	V_{CC} – 0.2			V
		V_{CC} = 3.15 V	I_{OH} = –12 mA	2.4			
			I_{OH} = –24 mA	2			
V_{OL}	A port and CLKOUT	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	V
		V_{CC} = 3.15 V	I_{OL} = 12 mA			0.4	
			I_{OL} = 24 mA			0.5	
	B port and SSCLK	V_{CC} = 3.15 V to 3.45 V,	I_{OL} = 100 µA			0.2	
		V_{CC} = 3.15 V	I_{OL} = 10 mA			0.2	
			I_{OL} = 64 mA			0.4	
			I_{OL} = 100 mA			0.55	
I_I	SYSCLK and control inputs	V_{CC} = 3.45 V,	V_I = 0 to 5.5 V			±10	µA
I_{OZ}[(2)]	B port and SSCLK	V_{CC} = 3.45 V, V_{REF} within 0.6 V of V_{TT},	V_O = 0 to 2.3 V			±10	µA
	CLKOUT	V_{CC} = 3.45 V,	V_O = 0 to 5.5 V			±10	
I_{OZH}[(2)]	A port	V_{CC} = 3.45 V,	V_O = V_{CC}			10	µA
I_{OZL}[(2)]	A port	V_{CC} = 3.45 V,	V_O = GND			–10	µA
I_{BHL}[(3)]	A port	V_{CC} = 3.15 V,	V_I = 0.8 V	75			µA
I_{BHH}[(4)]	A port	V_{CC} = 3.15 V,	V_I = 2 V	–75			µA
I_{BHLO}[(5)]	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	500			µA
I_{BHHO}[(6)]	A port	V_{CC} = 3.45 V,	V_I = 0 to V_{CC}	–500			µA
I_{CC}	A port, B port, or SSCLK	V_{CC} = 3.45 V, I_O = 0, V_I (A-port or control input) = V_{CC} or GND, V_I (B port) = V_{TT} or GND	Outputs high			50	mA
			Outputs low			50	
			Outputs disabled			50	
ΔI_{CC}[(7)]		V_{CC} = 3.45 V, One A-port or control input at V_{CC} – 0.6 V, Other A-port or control inputs at V_{CC} or GND				1.5	mA
C_i	SYSCLK inputs	V_I = 3.15 V or 0			4	5	pF
	Control inputs	V_I = 3.15 V or 0			3.5	5.5	
C_{io}	A port	V_O = 3.15 V or 0			7.5	9.5	pF
	B port or SSCLK	V_O = 1.5 V or 0			9.5	12	
C_o	CLKOUT	V_O = 3.15 V or 0			6	7.5	pF

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) For I/O ports, the parameter I_I includes the off-state output leakage current.
(3) The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
(5) An external driver must source at least I_{BHLO} to switch this node from low to high.
(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.
(7) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Hot-Insertion Specifications for A Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 5.5 V		10	μA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	μA
I_{OZPD}	V_{CC} = 1.5 V to 0,	V_O = 0.5 V to 3 V,	$\overline{OE}$ = 0		±30	μA

Live-Insertion Specifications for B Port

over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
I_{off}	V_{CC} = 0,	BIAS V_{CC} = 0,	V_I or V_O = 0 to 1.5 V		10	μA
I_{OZPU}	V_{CC} = 0 to 1.5 V,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	μA
I_{OZPD}	V_{CC} = 1.5 V to 0,	BIAS V_{CC} = 0,	V_O = 0.5 V to 1.5 V, $\overline{OE}$ = 0		±30	μA
I_{CC} (BIAS V_{CC})	V_{CC} = 0 to 3.15 V	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0 to 1.5 V		5	mA
	V_{CC} = 3.15 V to 3.45 V				10	μA
V_O	V_{CC} = 0,	BIAS V_{CC} = 3.3 V,	I_O = 0	0.95	1.05	V
I_O	V_{CC} = 0,	BIAS V_{CC} = 3.15 V to 3.45 V,	V_O (B port) = 0.6 V	–1		μA

Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (unless otherwise noted)

			MIN	MAX	UNIT
f_{clock}	Clock frequency			175	MHz
t_w	Pulse duration	SYSCLK (A to B) or (B to A) high or low	2.5		ns
		SYSCLK to CLKOUT high or low	2.8		
		SYSCLK to SSCLK (FSTA GND) high or low	2.8		
		SYSCLK to SSCLK (FSTA V_{CC}) high or low	2.3		
		SSCLK (B to A) high or low	2.8		
		SSCLK to CLKOUT high or low	2.8		
		$\overline{CKOE}$ (A to B) or (B to A) high	2.5		
t_{su}	Setup time	A before SYSCLK↑	1.1		ns
		B before SYSCLK↑	2.2		
		B before SSCLK↑	1.6		
		A before $\overline{CKOE}$↓	1.4		
		B before $\overline{CKOE}$↓	0.8		
t_h	Hold time	A after SYSCLK↑	0.3		ns
		B after SYSCLK↑	0.7		
		B after SSCLK↑	1.1		
		A after $\overline{CKOE}$↓	0		
		B after $\overline{CKOE}$↓	0.7		

Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature,
V_{TT} = 1.5 V and V_{REF} = 1 V for GTLP (see Figure 1)

PARAMETER	CLOCK	FROM (INPUT)	TO (OUTPUT)	EDGE RATE(1)	FSTA	MIN	TYP(2)	MAX	UNIT
f_{max}	SYSCLK	A or B	B or A			175			MHz
		SYSCLK	CLKOUT			175			
			SSCLK		GND	175			
					V_{CC}	150			
	SSCLK	B	A			175			
		SSCLK	CLKOUT			175			
t_{pd}		A	B	Fast		2.3		6.2	ns
				Slow		3		7.3	
		$\overline{\text{CKOE}}$	B	Fast		2.6		6	
				Slow		3.1		7.6	
		SYSCLK	B	Fast		2.6		6	
				Slow		3		7.1	
t_{en}		$\overline{\text{OE}}$	B	Fast		2.3		5.1	ns
t_{dis}						2.7		5.5	
t_{en}		$\overline{\text{OE}}$	B	Slow		2.9		6	ns
t_{dis}						3.6		6.6	
t_r		Rise time, B and SSCLK outputs (20% to 80%)		Fast			1.1		ns
				Slow			2.1		
t_f		Fall time, B and SSCLK outputs (80% to 20%)		Fast			1.8		ns
				Slow			2.4		
t_{pd}		B	A			1.5		4.6	ns
		$\overline{\text{CKOE}}$				2.1		6	
		SYSCLK	A			1.9		6	
		SSCLK				2.3		6.6	
		SYSCLK	CLKOUT			3.3		8.3	
		SSCLK				3.7		9	
t_{en}		$\overline{\text{OE}}$	A			1.6		5	ns
t_{dis}						2.1		6.4	
t_{en}		$\overline{\text{CKOE}}$	CLKOUT			2		5.2	ns
t_{dis}						2.4		6.1	

(1) Slow (ERC = H) and Fast (ERC = L)
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

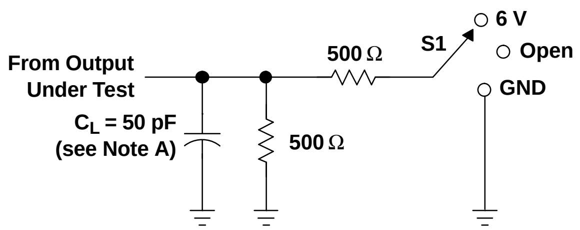
Skew Characteristics(1)

over recommended ranges of supply voltage and operating free-air temperature, V_{REF} = 1 V, standard lumped loads (C_L = 30 pF for B port) (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE(2)	FSTA	TEST CONDITIONS	MIN	MAX	UNIT
$t_{sk(LH)}$ (3)	SYSCLK	B	Fast				0.5	ns
$t_{sk(HL)}$ (3)							0.5	
$t_{sk(LH)}$ (3)	SYSCLK	B	Slow				0.5	ns
$t_{sk(HL)}$ (3)							0.5	
$t_{sk(LH)}$ (3)	SYSCLK	SSCLK + ΔB (see Figure 2)	Fast	GND	V_{CC} = 3.15 V, T_A = 85°C	3.2	4.6	ns
					V_{CC} = 3.3 V, T_A = 25°C	2.9	4.3	
					V_{CC} = 3.45 V, T_A = –40°C	2.8	4.1	
$t_{sk(HL)}$ (3)	SYSCLK	SSCLK + ΔB (see Figure 2)	Fast	GND	V_{CC} = 3.15 V, T_A = 85°C	3.6	5	ns
					V_{CC} = 3.3 V, T_A = 25°C	3.4	4.8	
					V_{CC} = 3.45 V, T_A = –40°C	3.3	4.6	
$t_{sk(LH)}$ (3)	SYSCLK	SSCLK + ΔB (see Figure 2)	Slow	GND	V_{CC} = 3.15 V, T_A = 85°C	3	4.6	ns
					V_{CC} = 3.3 V, T_A = 25°C	2.6	4.3	
					V_{CC} = 3.45 V, T_A = –40°C	2.4	4	
$t_{sk(HL)}$ (3)	SYSCLK	SSCLK + ΔB (see Figure 2)	Slow	GND	V_{CC} = 3.15 V, T_A = 85°C	3.7	5.2	ns
					V_{CC} = 3.3 V, T_A = 25°C	3.6	5.1	
					V_{CC} = 3.45 V, T_A = –40°C	3.5	5	
$t_{sk(LH)}$ (3)	SYSCLK	SSCLK + ΔB (see Figure 2)	Fast	V_{CC}	V_{CC} = 3.15 V, T_A = 85°C	6.5	8.3	ns
					V_{CC} = 3.3 V, T_A = 25°C	6.3	8.2	
					V_{CC} = 3.45 V, T_A = –40°C	5.6	7.4	
$t_{sk(HL)}$ (3)	SYSCLK	SSCLK + ΔB (see Figure 2)	Fast	V_{CC}	V_{CC} = 3.15 V, T_A = 85°C	7	8.7	ns
					V_{CC} = 3.3 V, T_A = 25°C	6.5	8.3	
					V_{CC} = 3.45 V, T_A = –40°C	6.2	8	
$t_{sk(LH)}$ (3)	SYSCLK	SSCLK + ΔB (see Figure 2)	Slow	V_{CC}	V_{CC} = 3.15 V, T_A = 85°C	6.4	8.3	ns
					V_{CC} = 3.3 V, T_A = 25°C	5.9	7.7	
					V_{CC} = 3.45 V, T_A = –40°C	5.5	7.4	
$t_{sk(HL)}$ (3)	SYSCLK	SSCLK + ΔB (see Figure 2)	Slow	V_{CC}	V_{CC} = 3.15 V, T_A = 85°C	7.2	8.9	ns
					V_{CC} = 3.3 V, T_A = 25°C	6.8	8.6	
					V_{CC} = 3.45 V, T_A = –40°C	6.6	8.3	
$t_{sk(t)}$ (3)	SYSCLK	B	Fast				1.4	ns
			Slow				2	
$t_{sk(prLH)}$ (4)	SYSCLK	B					1.8	ns
$t_{sk(prHL)}$ (4)							2.8	

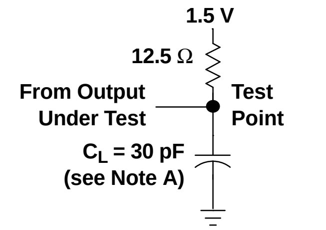
(1) Actual skew values between the GTLP outputs could vary on the backplane due to the loading and impedance seen by the device.
(2) Slow (ERC = H) and Fast (ERC = L)
(3) $t_{sk(LH)}/t_{sk(HL)}$ and $t_{sk(t)}$ – Output-to-output skew is defined as the absolute value of the difference between the actual propagation delay for all outputs with the same packaged device. The specifications are given for specific worst-case V_{CC} and temperature. The specifications apply to any outputs switching in the same direction, either high to low [$t_{sk(HL)}$], low to high [$t_{sk(LH)}$], or in opposite directions, both low to high and high to low [$t_{sk(t)}$].
(4) $t_{sk(prLH)}$ or $t_{sk(prHL)}$ – Part-to-part skew is designed as the absolute value of the difference between the actual propagation delay for all outputs from device to device. The parameter is specified for a specific worst-case V_{CC} and temperature. Furthermore, these values are provided by TI SPICE simulations.

PARAMETER MEASUREMENT INFORMATION

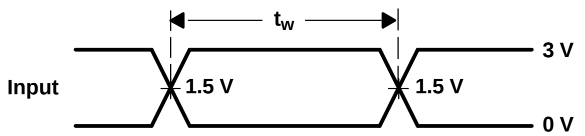


LOAD CIRCUIT FOR A OUTPUTS

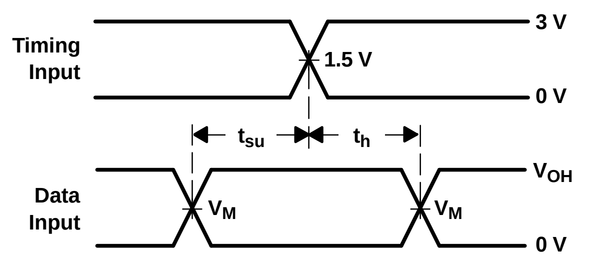
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



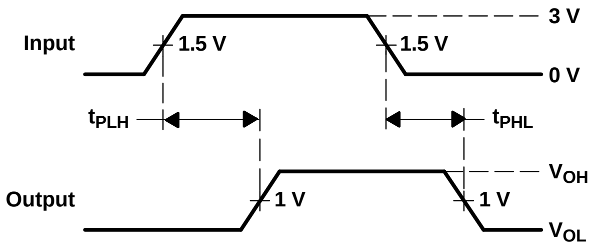
LOAD CIRCUIT FOR B OUTPUTS



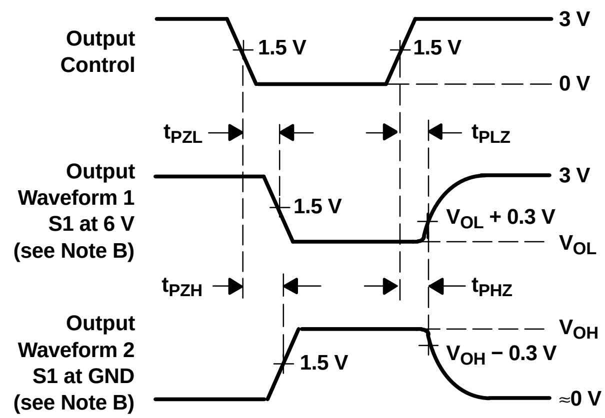
VOLTAGE WAVEFORMS
PULSE DURATION



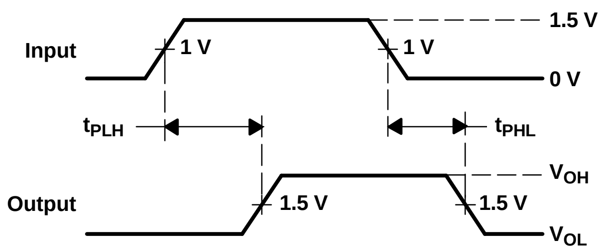
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
(V_M = 1.5 V for A port and 1 V for B port)
(V_{OH} = 3 V for A port and 1.5 V for B port)



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(A port to B port)



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
(A port)

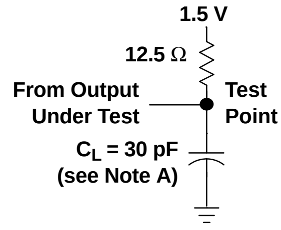


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
(B port to A port)

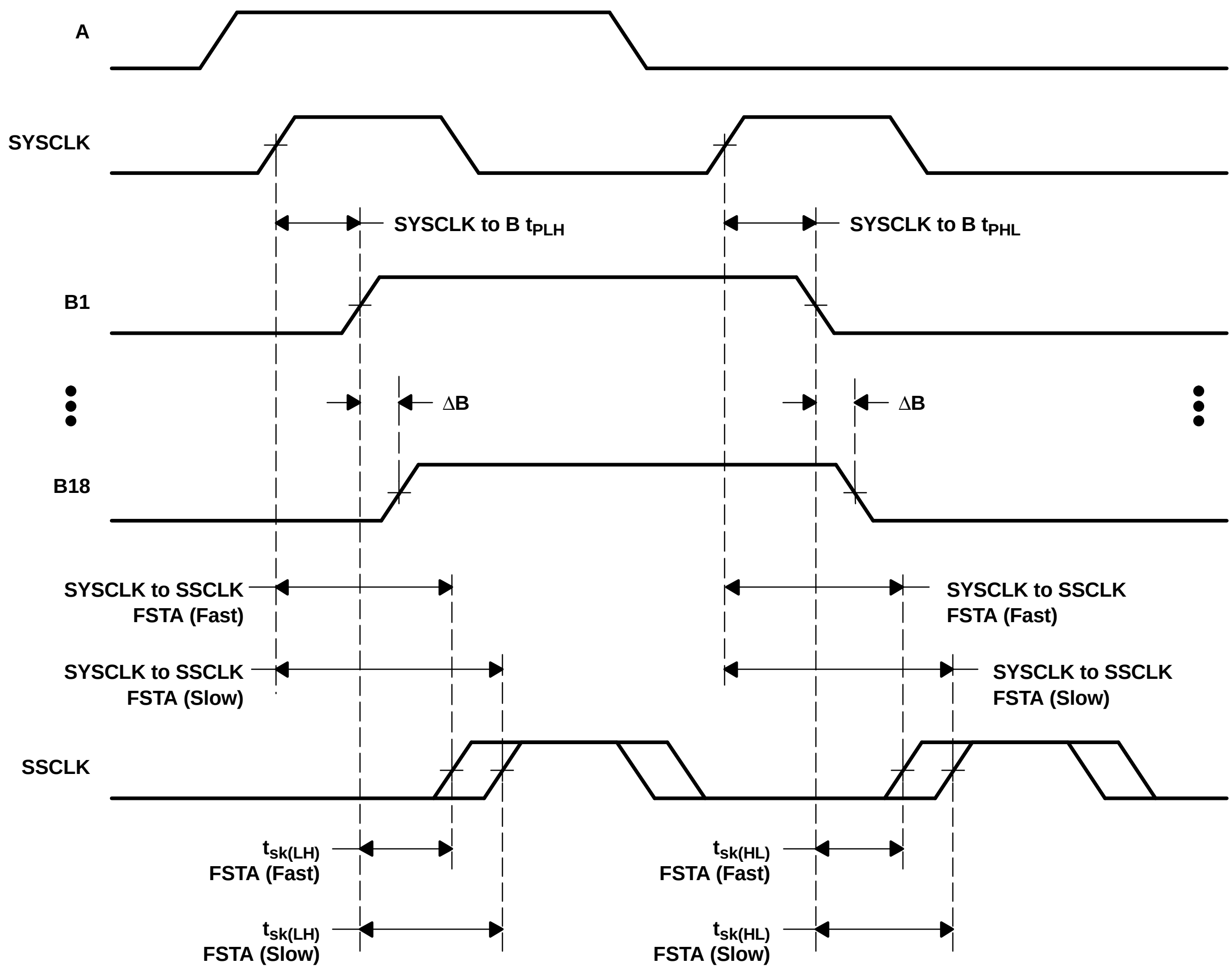
NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. Load circuit for A outputs also is used for CLKOUT; load circuit for B outputs also is used for SSCLK.

Figure 1. Load Circuits and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



LOAD CIRCUIT FOR B OUTPUTS



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. Load circuit for B outputs also is used for SSCLK.

Figure 2. Load Circuit and SYSCLK to SSCLK + ΔB Skew Waveforms

DISTRIBUTED-LOAD BACKPLANE SWITCHING CHARACTERISTICS

The preceding switching characteristics table shows the switching characteristics of the device into a lumped load (Figure 1). However, the designer's backplane application probably is a distributed load. The physical representation is shown in Figure 3. This backplane, or distributed load, can be closely approximated to a resistor inductance capacitance (RLC) circuit, as shown in Figure 4. This device has been designed for optimum performance in this RLC circuit. The following switching characteristics table shows the switching characteristics of the device into the RLC load, to help the designer to better understand the performance of the GTLP device in this typical backplane. See www.ti.com/sc/gtlp for more information.

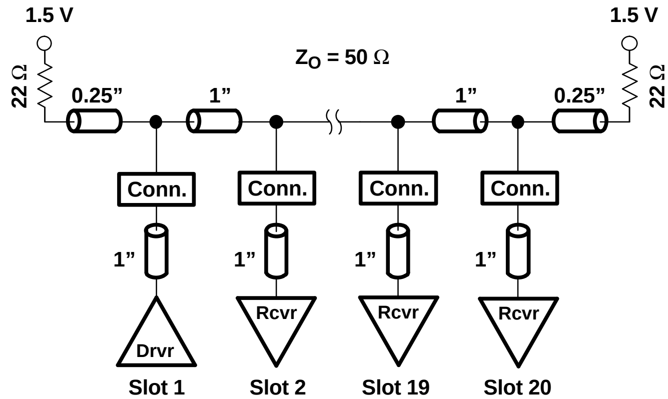


Figure 3. High-Drive Test Backplane

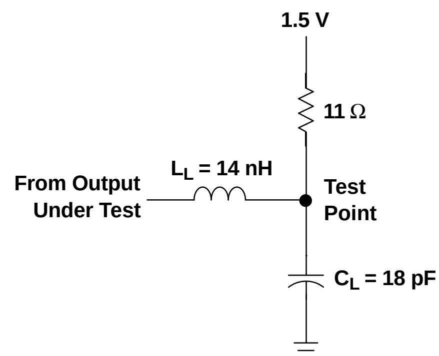


Figure 4. High-Drive RLC Network

Switching Characteristics

over recommended operating conditions for the bus transceiver function (unless otherwise noted) (see Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	EDGE RATE[1]	FSTA	TYP[2]	UNIT
t_{PLH}	A	B	Fast	–	4.8	ns
t_{PHL}					4.2	
t_{PLH}			Slow	–	5.6	
t_{PHL}					5.2	
t_{PLH}	SYSCLK	B	Fast	–	4.9	ns
t_{PHL}					4.5	
t_{PLH}			Slow	–	5.5	
t_{PHL}					5.2	
t_r	Rise time, B and SSCLK outputs (20% to 80%)		Fast	–	0.9	ns
			Slow	–	1.3	
t_f	Fall time, B and SSCLK outputs (80% to 20%)		Fast	–	2.3	ns
			Slow	–	2.7	

(1) Slow (ERC = H) and Fast (ERC = L)
(2) All typical values are at V_{CC} = 3.3 V, T_A = 25°C. All values are derived from TI SPICE models.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
74GTLPH1627DGGRE4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
74GTLPH1627DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
SN74GTLPH1627DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

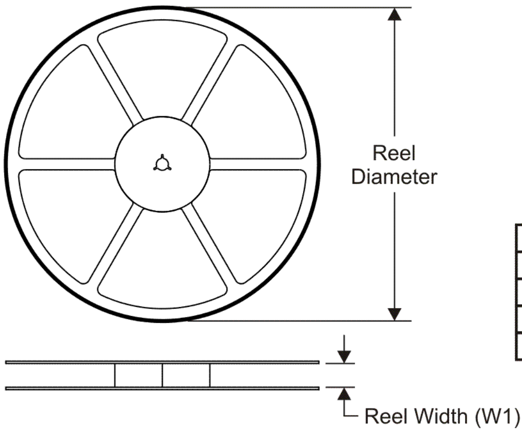
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

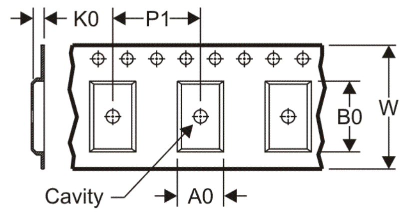
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

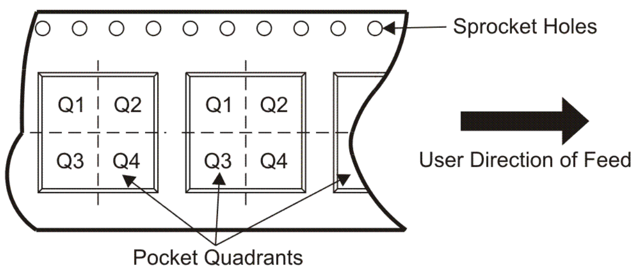


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

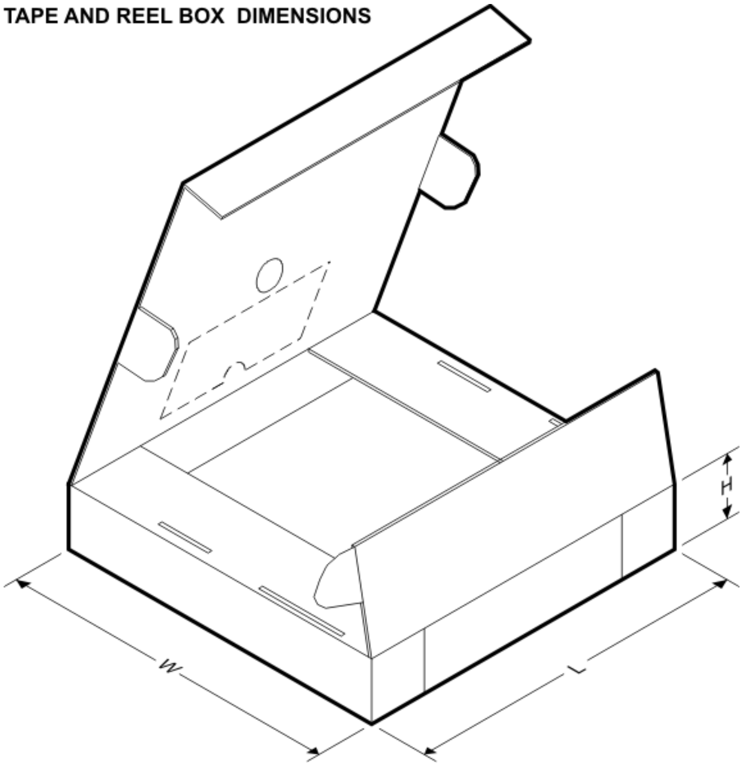
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74GTLPH1627DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

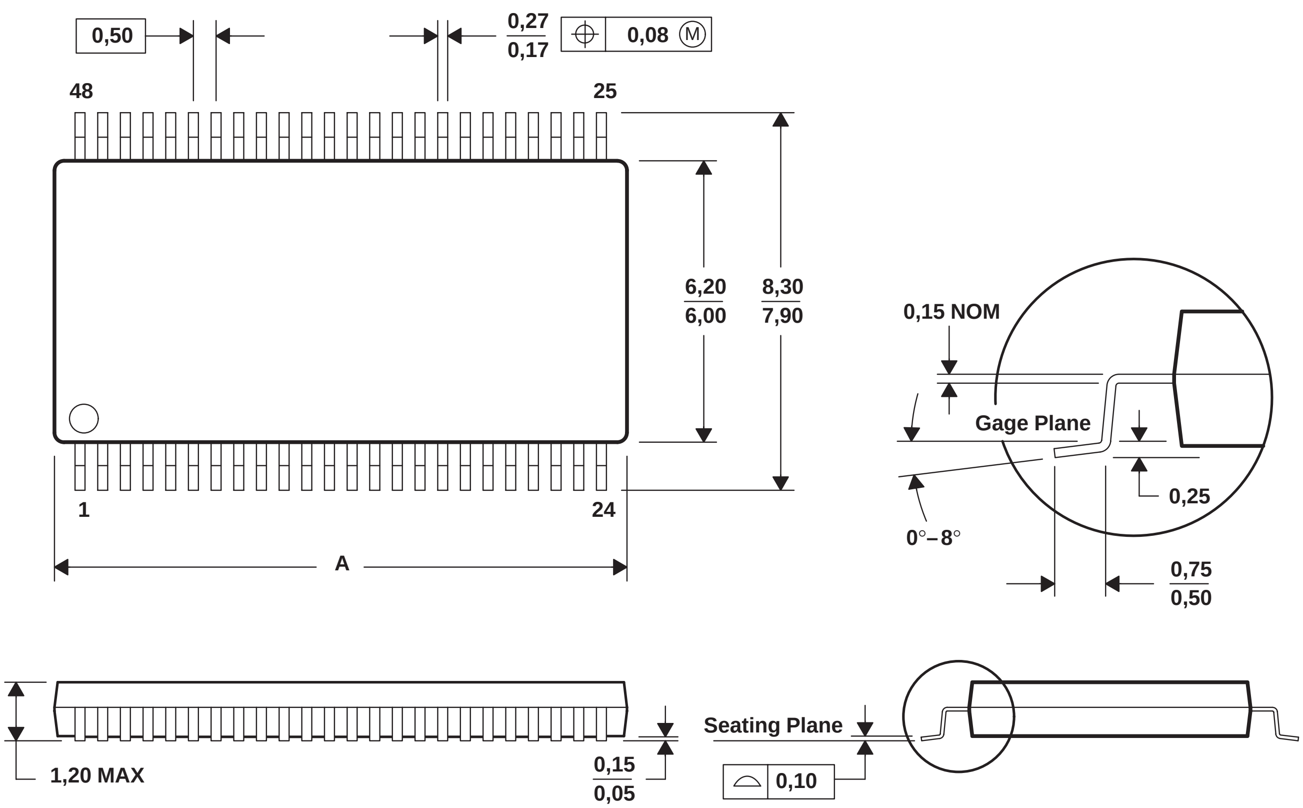


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74GTLPH1627DGGR	TSSOP	DGG	64	2000	346.0	346.0	41.0

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153