

PTN5150H

CC logic for USB Type-C applications

Rev. 1 — 13 April 2016

Product data sheet

1. General description

PTN5150H is a small thin low power CC Logic chip supporting the USB Type-C connector application with Configuration Channel (CC) control logic detection and indication functions. The features of PTN5150H enable USB Type-C connector to be used in both host and device ends of the Type-C cable. It can support Type-C to USB legacy cables and adapters defined in USB Type-C Spec. PTN5150H can work autonomously, or can connect to a controller through I²C-bus interface.

PTN5150H can be configured to dual role, host, or device mode through external configuration pin or through I2C interface. The CC control logic detection and indication block supports 3 current modes (default current 500 mA/900 mA, medium current 1.5 A and high current 3.0 A) in DFP advertisement's perspective. When in UFP advertisement's perspective, the control logic will detect if a DFP with different pull-up R_p current source is connected. In addition, it will detect if R_a is present on CC1/CC2 pins. Upon detection of plug orientation, pin ID will indicate if PTN5150H is working under either host role or device role, and other status will also be reflected in I2C registers.

2. Features and benefits

- Support type C connector with existing chipsets
 - ◆ USB Type-C Rev 1.1 compliance
 - ◆ Compatible with legacy OTG hardware and software
 - ◆ Support plug, orientation, role and charging current detection.
 - ◆ USB-ID pin for OTG application
 - ◆ I²C-bus interface support for fast mode
- CC control logic detection and indication
 - ◆ PORT input pin to configure in DRP (Hi-Z), UFP (low) or DFP (high)
 - ◆ Current mode detection when PTN5150H is operating under UFP (device) role: default current mode (<0.5 A/0.9 A); medium current mode (<1.5 A); high current mode (<3.0 A)
 - ◆ Integrated accurate R_p current sources to support default mode and high current mode under host mode: default current mode at 80 μA; medium current mode at 180 μA; high current mode at 330 μA
 - ◆ Integrate R_d resistor in UFP mode
 - ◆ Report detail port states and accessory modes in I2C registers
 - ◆ Support VCONN1/2 power detected status through VCONN Status I2C register 0AH
- Current consumption:
 - ◆ Hibernation mode: 4.5 μA
 - ◆ Standby in DRP mode: 15 μA



- ◆ Standby in DFP mode: 15 μ A
- ◆ Standby in UFP mode: 15 μ A
- Power supply: VDD=2.7 V to 5.5 V
- VBUS_DET: 28 V Absolute Max Tolerance
- High ESD protection for VBUS and CC1/2 pins
 - ◆ ESD protection exceeds 7000 V HBM per JDS-001-2012 and 500 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Operating Temperature Range: -40 °C to +85 °C
- X2QFN12 package 1.6 mm \times 1.6 mm \times 0.35 mm, 0.4 mm pitch

3. Applications

- Tablets/Mobile Devices
- Ultrabook/Notebook Computers
- Docking Stations

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PTN5150HHX	5H	X2QFN12	Plastic, super thin quad flat package; no leads; 12 terminals; body 1.6 mm \times 1.6 mm \times 0.35 mm, 0.4 mm lead pitch	SOT1355-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PTN5150HHX	PTN5150HHXMP	X2QFN12	REEL 13" Q2/T3 *STANDARD MARK SMD DP	10000	T _{amb} = -40 °C to +85 °C
PTN5150HHX	PTN5150HHXZ	X2QFN12	REEL 7" Q2/T3 *STANDARD MARK SMD SMALLPQ DP	500	T _{amb} = -40 °C to +85 °C

5. Functional diagram

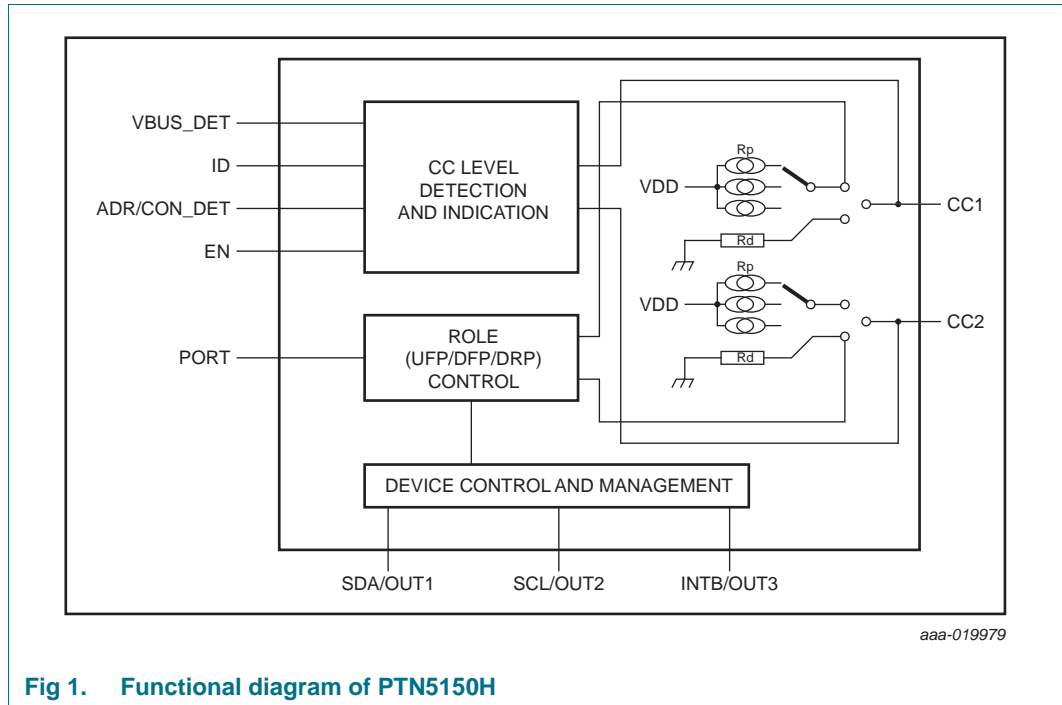


Fig 1. Functional diagram of PTN5150H

6. Pinning information

6.1 Pinning

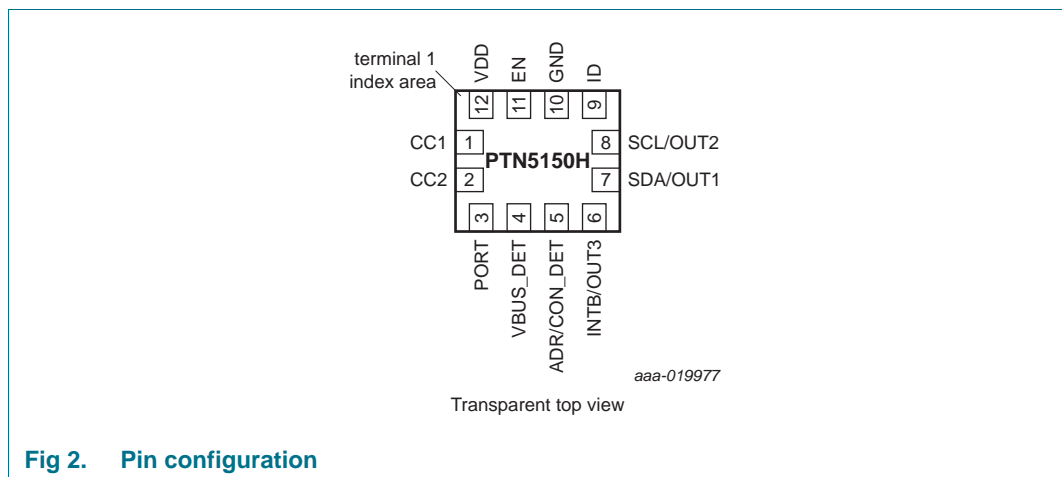


Fig 2. Pin configuration

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Type	Description									
1	CC1	I/O	Configure Channels as defined in USB Type-C specification									
2	CC2											
3	PORT	Input	<p>Trinary GPIO Input selection run from VDD</p> <p>PORT= VDD: DFP mode (Rp = 80 uA power default for non-I2C mode).</p> <p>PORT= Mid (or floating): DRP mode</p> <p>PORT=GND: UFP mode</p> <p>If ADR = High or Low (I2C mode), PORT input status will be only latched during power up. To change the mode selection, system must write I2C register bit to override mode selection.</p> <p>If ADR = Mid (no- I2C mode). PORT input can be dynamically change.</p>									
4	VBUS_DET	Input	<p>VBUS Detection Pin. (28 V Max Tolerance)</p> <p>One 1 MΩ ± 1 % external resistor required between system Vbus and VBUS_DET pin</p>									
5	ADR/CON_DET	I/O	<p>Trinary GPIO Input ADR pin run from VDD</p> <ul style="list-style-type: none"> ADR pull up to VDD with 10 kΩ resistor (I2C Enabled with ADDR bit 6 equal to 1, I2C Address 0x7C) ADR pull down to GND with 10 kΩ resistor. (I2C Enabled with ADDR bit 6 equal to 0, I2C Address 0x3C) ADR = Mid or floating (Pin 6/7/8) configured as OUT1/2/3 in non-I2C mode <p>Output. This pin will automatically switch from input to CON_DET output in "non-I2C mode or set 09H bit[0] to 0" after TINPUTLATCH</p> <ul style="list-style-type: none"> CON_DET = High (Connection Detected) CON_DET = Low (No Connection) 									
6	INTB/OUT3	O/D output	<p>Interrupt to notify I2C status register changed</p> <p>INTB: (only valid in I2C mode)</p> <ul style="list-style-type: none"> Low = Interrupt asserted Hi-Z = Interrupt de-asserted <p>OUT3: (only valid in non- I2C mode)</p> <ul style="list-style-type: none"> Low = Analog Audio Detected Hi-Z = No Detection 									
7	SDA/OUT1	O/D Input /output	<p>I2C SDA (Open Drain Input & Output)</p> <p>OUT 2 & OUT 1 : (Open Drain Output)</p> <table border="0"> <tr> <td>0</td> <td>0</td> <td>= high current mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>= medium current mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>= default current mode</td> </tr> </table>	0	0	= high current mode	1	0	= medium current mode	1	1	= default current mode
0	0	= high current mode										
1	0	= medium current mode										
1	1	= default current mode										
8	SCL/OUT2	O/D Input /output	<p>I2C SCL (Open Drain Input)</p> <p>OUT 2 & OUT 1 : (Open Drain Output)</p> <table border="0"> <tr> <td>0</td> <td>0</td> <td>= high current mode</td> </tr> <tr> <td>1</td> <td>0</td> <td>= medium current mode</td> </tr> <tr> <td>1</td> <td>1</td> <td>= default current mode</td> </tr> </table>	0	0	= high current mode	1	0	= medium current mode	1	1	= default current mode
0	0	= high current mode										
1	0	= medium current mode										
1	1	= default current mode										
9	ID	O/D output	<p>ID (Open Drain Output)</p> <p>Low = DFP mode detected valid UFP on CC1 or CC2 line. This signal is used to enable OTG mode, requires external pull up resistor.</p>									

Table 3. Pin description ...continued

Symbol	Pin	Type	Description
10	GND	Power	Ground
11	EN	Input	Chip Enable and Disable <ul style="list-style-type: none"> • High = Chip Enable • Low = Chip disable or hibernation mode. When chip is placed under hibernation mode, I2C configuration register (02H, 09H, 18H) contents are retained.
12	VDD	Power	Power supply

7. Functional description

7.1 CC detection and indication block

For USB Type-C solution, two pins on the connector, CC1 and CC2, are used to establish and manage the DFP/UFP connection between a host port and a device port.

A hardware GPIO trinary pin, PORT, is provided to configure PTN5150H in either DFP/DRP/UFP mode alternatively, the PORT input can be override later by override the I2C registers. If the GPIO Trinary ADR input is mid-level or floating (non I2C), PORT input pin can dynamically change at any time to reconfigure the DFP/DRP/UFP. The GPIO trinary input pins should be powered by VDD.

- When PTN5150H is operating under host role, different current modes (high/medium/default) can be configured through I2C register. During initial power up, default current mode is being selected. In order to indicate different current modes, three Rp current sources are being implemented.

Table 4. Current source implementation for each DFP advertisement

DFP advertisement	Current source to VDD	Current source precision
Default USB Power	80 μ A	± 20 %
1.5 A at 5 V	180 μ A	± 8 %
3.0 A at 5 V	330 μ A	± 8 %

Internal comparators are constantly monitoring the voltage levels of CC1 and CC2 pins. PTN5150H reports if an UFP (device) or powered cable is connected externally on the CC pins. When no external connection is detected, cable connected bit in the I2C register will be cleared. Any changes in the attach/detach events or Rp current source changes will trigger INTB pin to go LOW.

Table 5. RD implementation for each UFP advertisement

UFP advertisement	RD value	RD accuracy
UFP mode	5.1 k Ω	± 10 %

Table 6. Voltage range detection for each DFP advertisement

DFP advertisement	UFP (V_{Rd}) voltage range	Powered cable/adaptor V_{Ra} voltage range	No connect (V_{open}) voltage range
Default USB Power	0.25 V to 1.50 V	0.00 V to 0.15 V	>1.65 V
1.5 A at 5 V	0.45 V to 1.50 V	0.00 V to 0.35 V	>1.65 V
3.0 A at 5 V	0.85 V to 2.45 V	0.00 V to 0.75 V	>2.75 V

- When PTN5150H is operating under device role (UFP), it is able to detect different current modes indicated by external host's pull-up resistors. Internally there is a pull-down resistor (R_d) of 5.1 k Ω on CC1 and CC2 pins. Status of current mode detected is reported in the I2C register. If pin 6/7/8 is configured as OUT1/2/3, OUT1/2 reports the detected R_p pull up current source value as well.

The configuration channel (CC1 or CC2) is used to serve the following purposes in this block

- Detect connection of USB ports, e.g. a DFP (host) or a UFP (device), and establish host or device roles between two connected ports. When there is no power supplied to PTN5150H, device role (with internal pull-down resistor R_d active) will be the default configuration.
- Resolve cable orientation and twist connections to establish USB data bus routing.
- Discover optional accessory modes such as audio adapter accessory and debug accessory modes. Resistors (R_a , R_d , R_p , or Open) connected on CC1/CC2 will be reported in the I2C registers, and host controller can configure the external interface accordingly.

7.2 ADR/CON_DET output pin

Pin 5 is multiple purpose I/O pin. When device power up, pin 5 is input which latched the input voltage level to configure I2C address. The I2C register offset 09H has default value "1" to disable CON_DET output. After TINPUT_LATCH, pin 5 becomes CON_DET output. When USB Type-C cable attached or detached in either DFP or UFP mode, CON_DET will asserted a signal to notify the system the status. The same attached or detached status also stored in the I2C interrupt register.

For ADR strapping resistor selection, 10 k Ω pull up or pull down resistor is recommended.

7.3 VCONN1/VCONN2 power output control

When a USB Type-C system need to support VCONN power in DFP or UFP power accessories mode, the system need to know the orientation to provide VCONN power. PTN5150H provides two bits of VCONN status register 0AH and an interrupt signal to notify system whether VCONN power is detected on VCONN1 or VCONN2 and then turn on discrete PowerFET using via 2 x GPIO. [Figure 3](#) shows the system level implementation of VCONN power with PTN5150H.

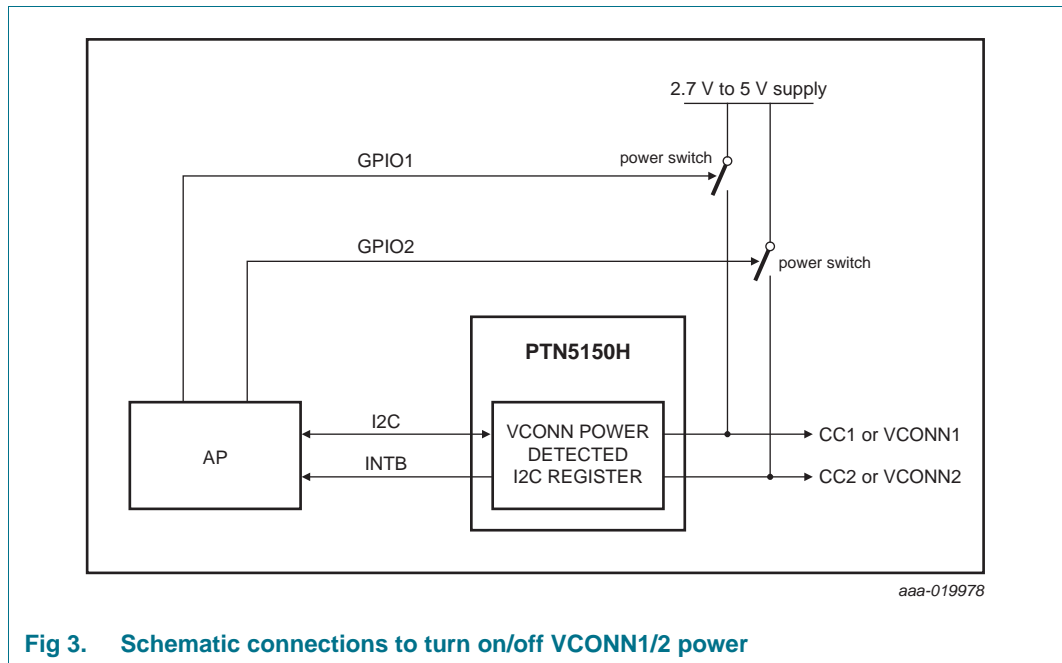


Fig 3. Schematic connections to turn on/off VCONN1/2 power

7.4 Off state

When PTN5150H is not powered (i.e., VDD = 0 V), special steps should be done to prevent back-current issues on control pins such as PORT or ADR pins when these pins' states are not low. These pins can be controlled through two different ways.

1. pull-up/pull-down resistors - make sure these pull-up resistors' VDD is the same power source as to power PTN5150H. When power to PTN5150H is off, power to these pull-up resistors will be off as well.
2. external processor's GPIO - if PTN5150H is turned off when the external processor's power stays on, processor should configure these GPIOs connected to these control pins as output low (< 0.4 V) or tri-state mode (configure GPIOs as input mode). This will make sure no current will be flowing into PTN5150H through these control pins.

7.5 I²C-bus

PTN5150H can work with systems with or without I²C-bus. "I²C mode" is defined as ADR pin has external 10 kΩ pull-up or pull-down resistor during power up, and "non-I²C mode" is defined as ADR pin is not connected to any external pull-up or pull-down resistor during power up. When operating in I²C mode, all features of PTN5150H can be configured and accessed through registers. OUT1, OUT2, OUT3 are not available in I²C mode. PORT input will be a one-time latched during power up.

In non-I²C mode, a subset of features can be configured or accessed through these I/O pins:

- PORT input: In non I²C-bus mode, PORT input can be dynamically change.
- CON_DET output: attached/detached notification
- OUT1/OUT2 output: detected R_p current source value
- OUT3: Analog Audio Detect

7.6 I²C-bus programmability

PTN5150H has I²C-bus interface that enables system integrator to program register settings suitable for the application needs. [Table 7](#) describes possible settings for different functions of the device. Although some functions of the device can be configured through external hardware pins (such as PORT), it also allows the system integrator to override the settings by programming the internal registers through I2C.

After power-on, the device samples the hardware pin values (as I2C is not operational yet) and reflects the status in the I2C status registers as default condition.

Table 7. I2C registers and descriptions

Register offset	Register name	Bits	Reset value	Description
01H	Version ID	[7:3]	00001	Device version ID
Read Only	Vendor ID	[2:0]	011	Vendor ID
02H	Control	[7:5]	000	Reserved
Read/Write		[4:3]	00	Rp Selection (DFP mode) 00: 80 μA Default 01: 180 μA Medium 10: 330 μA High 11 Reserved
		[2:1]	PORT pin state	Mode Selection 00: Device (UFP Mode) 01: Host (DFP Mode) 10: Dual Role (DRP Mode) During power up, device will latch the input of PORT input pin to configure UFP/DFP/DRP. After power up, writing to these register bits will overwrite the PORT Mode selection.
		[0]	0	Interrupt Mask for detached/attached 0: Does not Mask Interrupts 1: Mask Interrupts for register offset 03H bit[1:0].
03H	Interrupt Status	[7:2]	000000	Reserved
Read Only/Clear on Read		[1]	0	Cable Detach Interrupt 0: No Interrupt 1: Cable Detached
		[0]	0	Cable Attach Interrupt 0: No Interrupt 1: Cable Attached

Table 7. I2C registers and descriptions ...continued

Register offset	Register name	Bits	Reset value	Description
04H Read Only	CC Status	[7]	0	VBUS Detection (UFP mode after valid CC detection) 0: VBUS not detected 1: VBUS detected
		[6:5]	00	Rp Detection (In UFP mode) 00: Standby 01: Rp = Std USB 10: Rp = 1.5A 11: Rp = 3.0A
		[4:2]	000	Port Attachment Status 000: Not Connected 001: DFP attached 010: UFP attached 011: Analog Audio Accessory attached 100: Debug Accessory attached 101: Reserved 110: Reserved 111: Reserved
		[1:0]	00	CC Polarity 00: Cable Not Attached 01: CC1 is connected (normal orientation) 10: CC2 is connected (reversed orientation) 11: Reserved
05H	Reserved	[7:0]	00000000	Reserved
06H	Reserved	[7:0]	00000000	Reserved
07H	Reserved	[7:0]	00000000	Reserved
08H	Reserved	[7:0]	00000000	Reserved
09H Read/Write	CON_DET configuration register	[7:1]	0000000	Reserved
		[0]	1	Disable CON_DET output bit (Read/Write) 0: Enable CON_DET output on pin 5 1: Disable CON_DET output on pin 5 Recommend to disable CON_DET output for system using I2C to access PTN5150H

Table 7. I2C registers and descriptions ...continued

Register offset	Register name	Bits	Reset value	Description
0AH Read Only	VCONN Status register	[7:2]	000000	Reserved
		[1:0]	00	VCONN Detected Status (Read Only) 00: Standby 01: VCONN power should be applied on CC1 10: VCONN power should be applied on CC2 11: Reserved Ra detect happens in all modes. VCONN enable happens autonomously when as DFP (including in DRP mode). Prior to accessing this register, system must write register offset 43H with value of 0xe0 to enable VCONN detected status. If register offset 43H is not set to 0xe0, VCONN detected status read out is always 00.
10H	Reset register	[7:1]	0000000	Reserved.
		[0]	0	1: Reset system digital block
11H	Reserved	[7:0]	00001100	Reserved. Do not write any other values other than "00001100" (power up setting) to this register
12H	Reserved	[7:0]	000000	Reserved.
13H	Reserved	[7:0]	10100001	Reserved. Do not write to this register
14H	Reserved	[7:0]	00011111	Reserved. Do not write to this register
15H	Reserved	[7:0]	11001001	Reserved. Do not write to this register
16H	Reserved	[7:0]	01010001	Reserved. Do not write to this register
17H	Reserved	[7:0]	01010000	Reserved. Do not write to this register
18H Read/Write	Interrupt Mask register	[7]	0	Reserved
		[6]	0	Reserved
		[5]	0	Reserved
		[4]	1	Interrupt Mask for CC1 or CC2 Comparator Change 0: Does not Mask Interrupts 1: Mask Interrupts
		[3]	1	Interrupt Mask for role Change 0: Does not Mask Interrupts 1: Mask Interrupts
		[2]	1	Interrupt Mask for orientation Found 0: Does not Mask Interrupts 1: Mask Interrupts
		[1]	1	Interrupt Mask for debug Accessories Found 0: Does not Mask Interrupts 1: Mask Interrupts
		[0]	1	Interrupt Mask for audio Accessories Found 0: Does not Mask Interrupts 1: Mask Interrupts

Table 7. I2C registers and descriptions ...continued

Register offset	Register name	Bits	Reset value	Description
19H Read Only/Clear on Read	Interrupt Register status	[7]	0	Reserved
		[6]	0	Reserved
		[5]	0	Reserved
		[4]	0	Interrupt Status for Comparator Change 0: No interrupt 1: When attached as UFP, Change of Rp current advertisement detected. New advertisement is reflected on register offset 04H bit[6:5].
		[3]	0	Interrupt status for role change 0: No interrupt 1: Role changed detected. New role is reflected on register offset 04H bit[4:2].
		[2]	0	Interrupt status for orientation found 0: No interrupt 1: Orientation detected on attachment. New orientation is reflected on register offset 04H bit[1:0].
		[1]	0	Interrupt status for debug accessories found 0: No interrupt 1: Debug Accessory attachment detected. Register offset 04H bit[4:2] should be updated to 3'b100.
		[0]	0	Interrupt status for audio accessories found 0: No interrupt 1: Audio Accessory attachment detected. Register offset 04H bit[4:2] should be updated to 3'b011.

7.7 I²C-bus read and write operations

PTN5150H supports programming of the internal registers through the I²C-bus interface. I²C-bus can support up to 400 kHz data rate. 8-bit device slave address of PTN5150H is defined in combination with ADR pin.

Table 8. Read/write device slave address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave address	8	0	ADR	1	1	1	1	0	R/W

Reading/writing the internal registers must be done according to the following protocol. The read protocol contains two phases:

- Command phase
- Data phase

The command phase is an I²C write to PTN5150H that contains a single data byte indicating the internal register address to read out. The data phase is an I²C read operation that contains one byte of data and STOP bit is asserted, starting from the least significant byte.

The I2C write operation contains only the command phase, which contains 8-bit internal register address, followed by one byte of data to be written to the register, starting from the least significant byte.

It is recommended to use single-byte write/read commands to PTN5150H. Incremental address read/write function is not supported. [Figure 4](#) and [Figure 5](#) illustrate the protocol used on the I²C-bus to write and read register inside the device.

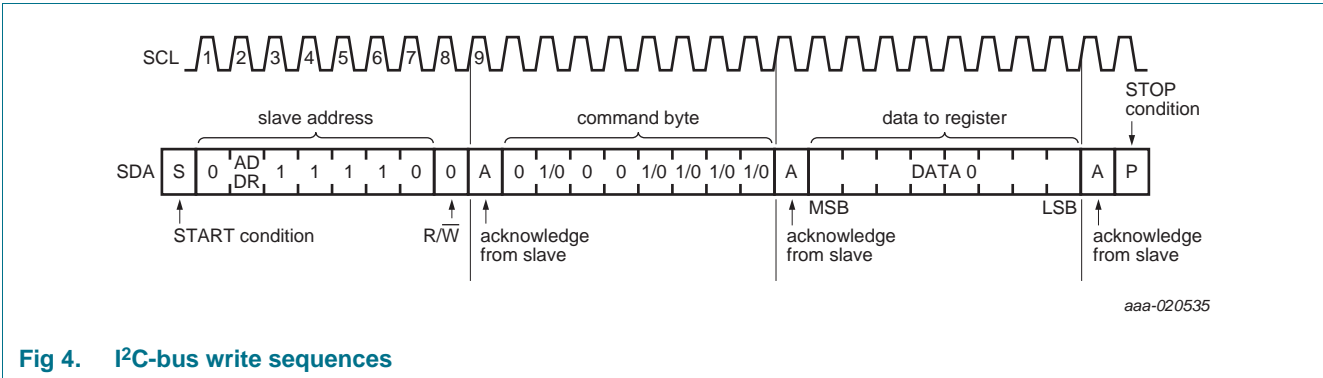


Fig 4. I²C-bus write sequences

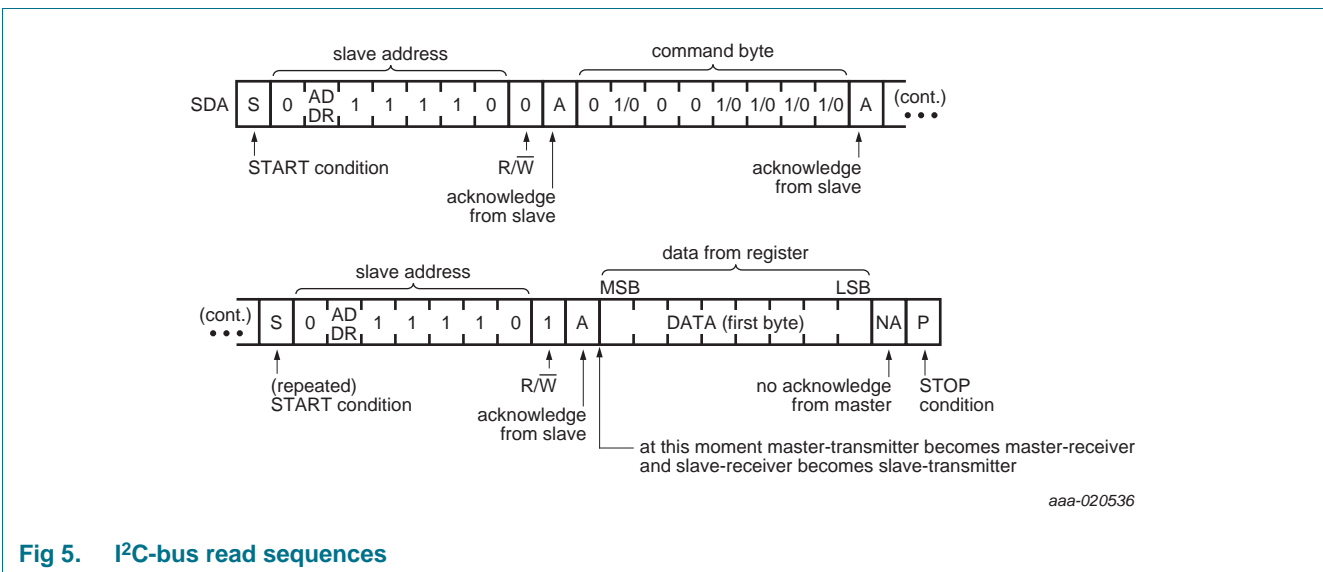


Fig 5. I²C-bus read sequences

8. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
VDD ^[1]	Supply voltage		-0.5	+6.0	V
VBUS_DET	VBUS Detect		-0.5	+28.0	V
Control pins	PORT, ADR/CON_DET, INTB/OUT3, CC1, CC2, EN, ID		-0.5	VDD +0.3	V
	SCL/OUT2, SDA/OUT1		-0.5	VDD +0.3	V
T _{stg}	Storage temperature		-65	150	°C
V _{esd}	Electrostatic discharge CC1/CC2/VBUS_DET	HBM ^[2]	-	7000	V
	All other pins	HBM ^[2]	-	2000	V
	All pins	CDM ^[3]	-	500	V

[1] All voltage values, except differential voltages, are with respect to network ground terminal.

[2] Human Body Model: ANSI/EOS/ESD-S5.1-1994, standard for ESD sensitivity testing, Human Body Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

[3] Charged Device Model: ANSI/EOS/ESD-S5.3-1-1999, standard for ESD sensitivity testing, Charged Device Model - Component level; Electrostatic Discharge Association, Rome, NY, USA.

9. Recommended operating conditions

Table 10. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	supply voltage	-40 to +85 °C	+2.7	-	+5.5	V
T _{VDDramp}	VDD ramp up time	Time to reach 90% of VDD	-	-	10	ms
VBUS_DET	VBUS Detect	VBUS Analog Input	4.0	5.0	21	V
V _i	input voltage	CMOS inputs (PORT, ADR)	-0.5	-	VDD+0.3	V
		I2C inputs (SCL, SDA, EN)	-0.5	-	1.98	V
T _{amb}	ambient temperature	operating in free air	-40	-	85	°C

10. Characteristics

Table 11. General characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Device role (UFP) Sink CC Detection						
R _d	Pull down resistor	UFP mode	4.59	5.10	5.61	kΩ
V _{CLAMPH}	High current mode clamp voltage	VDD=0 V	0.85	-	2.18	V
V _{CLAMPM}	Medium current mode clamp voltage	VDD=0 V	0.45	-	1.25	V

Table 11. General characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CLAMPD}	Default current mode clamp voltage	VDD=0 V	0.25	-	1.25	V
V _{THH}	High current mode threshold	UFP mode	1.16	1.23	1.31	V
V _{THM}	Medium current mode threshold	UFP mode	0.61	0.66	0.70	V
V _{THD}	Default current mode threshold	UFP mode	0.15	0.2	0.25	V
Host role (DFP advertisement) Current source						
I _{PH}	Current source	High current source mode (3 A)	304	330	356	μA
I _{PM}	Current source	Medium current source mode (1.5 A)	166	180	194	μA
I _{PD}	Current source	Default current source mode	64	80	96	μA
VBUS Detect Threshold						
V _{VBUSDET}	VBUSDET threshold	with external 1 MΩ ± 1 % resistor	2.4	2.9	4.1	V
Current Consumption						
I _{DD_ hibernation}	hibernation mode current	VDD = 3.3 V; EN = LOW	2	4.5	10	μA
I _{DD_ active}	active supply current; cable attached	VDD = 3.3 V PORT = high (DFP)	65	100	130	μA
		VDD = 3.3 V PORT = low (UFP)	5	15	35	μA
I _{DD_ standby}	standby/polling current; no cable attached	VDD = 3.3 V PORT = floating (DRP)	5	15	35	μA
		VDD = 3.3 V PORT = high (DFP)	5	15	35	μA
		VDD = 3.3 V PORT = low (UFP)	5	15	35	μA
T _{CCdebounce}	debounce time	time a port shall wait before it can determine it is attached	-	120	-	ms
T _{disconnection}	disconnection time	time a port shall respond when it is disconnected	-	1.2	-	ms
T _{Startup}	start-up time	supply voltage valid to R _p /R _d active	-	25	-	ms
T _{rcfg}		When selected DFP mode, system overwrite to UFP mode using I2C or PORT input, the Trcfg delay is measured from disabled R _p to enable R _d	-	2	-	ms
		When selected UFP mode, system overwrite to DFP mode using I2C or PORT input, the Trcfg delay is measured from to disable R _d and enable R _p	-	35	-	ms

Table 12. PORT control input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{pu}	external pull up resistor	External pull-up resistor is connected to VDD	-	10	-	kΩ
R _{pd}	external pull down resistor	External pull-down resistor is connected to GND	-	10	-	kΩ
V _{IL}	Input Low Voltage		-	-	0.4	V
V _{IM}	Input Mid level Voltage		40%*VDD	50%*VDD	60%*VDD	V
V _{IH}	Input High Voltage		80%*VDD	-	-	V

Table 13. ADR/CON_DET input/output characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{pu}	external pull up resistor	External pull-up resistor is connected to VDD	-	10	-	kΩ
R _{pd}	external pull down resistor	External pull-down resistor is connected to GND	-	10	-	kΩ
V _{IL}	Input Low Voltage		-	-	0.4	V
V _{IM}	Input Mid level Voltage		40%*VDD	50%*VDD	60%*VDD	V
V _{IH}	Input High Voltage		80%*VDD	-	-	V
V _{OH}	Output High Voltage	I _{OH} = 3 mA	80%*VDD	-	-	V
V _{OL}	Output Low Voltage	I _{OL} = 3 mA	-	-	20%*VDD	V

[1] CON_DET output can be enabled or disabled by accessing I2C register offset 09H bit[0]

Table 14. EN, SCL and SDA input characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IL(MAX)}	maximum input voltage low level		-	-	+0.4	V
V _{IH(MIN)}	minimum input voltage high level		1.05	-	-	V
I2C Fast mode interface pins (SCL, SDA)						
V _{HYS}	Hysteresis of Schmitt trigger inputs		0.09	-	-	V

Table 15. Open-drain output buffer characteristics (OUT2, OUT1, INTB/OUT3, ID pins)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VOL	low-level output voltage	IOL=3mA	0	-	0.4V	V

11. Package outline

X2QFN12: plastic, super thin quad flat package; no leads; 12 terminals; body 1.6 x 1.6 x 0.35 mm

SOT1355-1

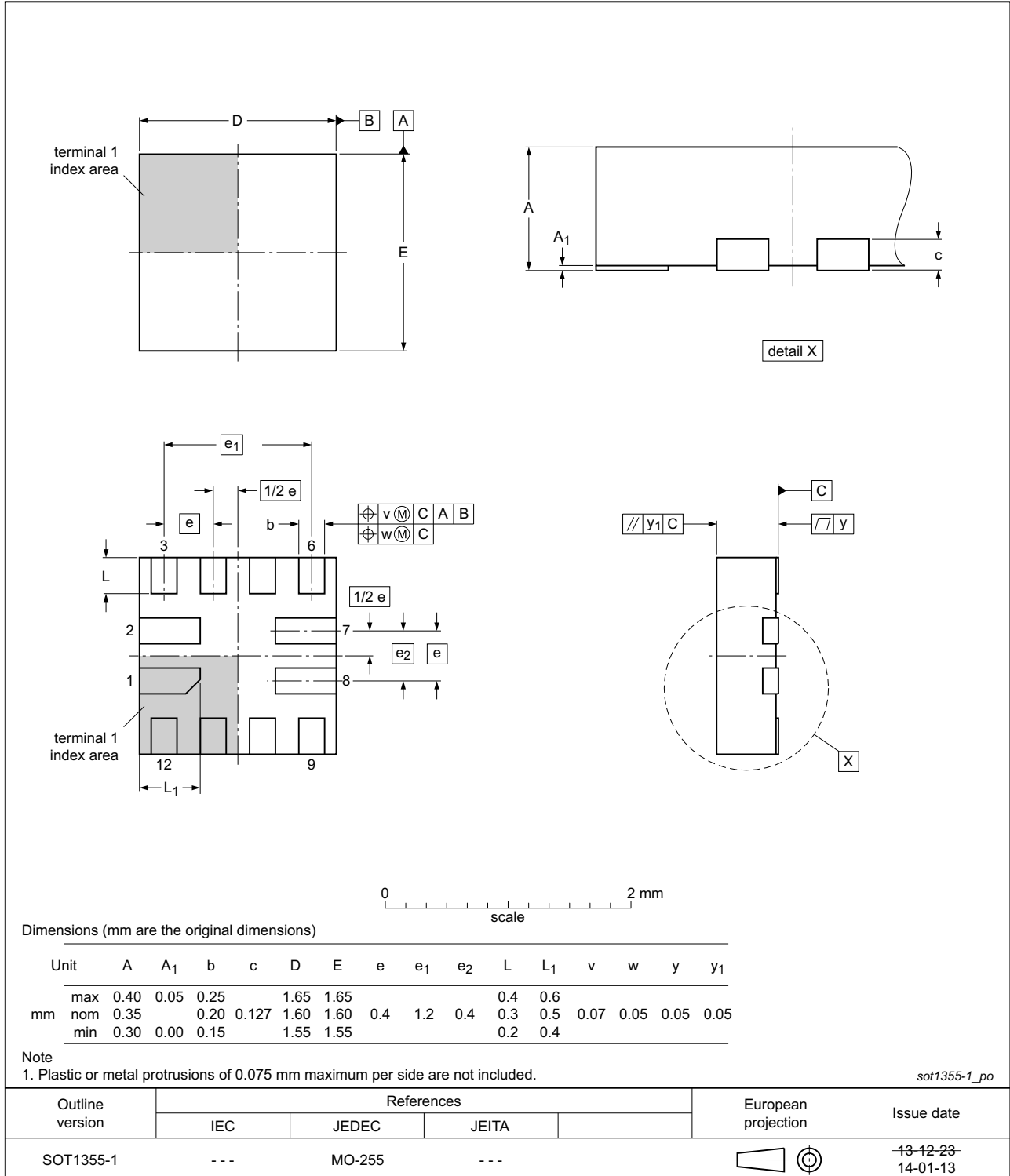


Fig 6. Package outline X2QFN12 (SOT1355-1)

12. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PTN5150H v.1	20160413	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 13 April 2016

Document identifier: PTN5150H