Application Notes

Reliability Testing Procedures

SMD Soldering Recommendations

Reliability Testing Procedures

Reliability Parameter	Test	Tested according to	Condition to be satisfied after testing
AC/DC Bias Reliability	AC/DC Life Test	CECC 42000, Test 4.20 or IEC 1051-1, Test 4.20. 1000 h at UCT	$\lvert DV_n/V_n$ @ 1 mA$\rvert$ < 10% R > 10 MW
Pulse Current Capability	I_{MAX} 8/20 µs	CECC 42000, Test C 2.1 or IEC 1051-1, Test 4.5. 10 pulses in the same direction at 2 pulses per minute at maximum peak current for 10 pulses	$\lvert DV_n/V_n$ @ 1 mA$\rvert$ < 10% no visible damage
Pulse Energy Capability	W_{MAX} 10/1000 µs	CECC 42000, Test C 2.1 or IEC 1051-1, Test 4.5. 10 pulses in the same direction at 1 pulse every minute at maximum peak current for 10 pulses	$\lvert DV_n/V_n$ @ 1 mA$\rvert$ < 10% no visible damage
Isolation Voltage Capability	Isolation Voltage	CECC 42000, Test 4.7 or IEC 1051-1, Test 4.8. Metal Ball method, 1 minute AC at isolation voltage	>1000V
Environmental and Storage Reliability	Climatic Sequence	CECC 42000, Test 4.16 or IEC 1051-1, Test 4.17. a) Dry heat, 16 h, UCT, Test Ba, IEC 68-2-2 b) Damp heat, cyclic, the first cycle: 55°C, 93% RH, 24 h, Test Db 68-2-4 c) Cold, LCT, 2 h, Test Aa, IEC 68-2-1 d) Damp heat, cyclic, remaining 5 cycles: 55°C, 93% RH, 24 h /cycle, Test Bd, IEC 68-2-30	$\lvert DV_n/V_n$ @ 1 mA$\rvert$ < 10% R > 10 MW
	Thermal Shock	CECC 42000, Test 4.12, Test Na, IEC 68-2-14 5 cycles UCT/LCT, 30 minutes	$\lvert DV_n/V_n$ @ 1 mA$\rvert$ < 10% no visible damage
	Steady State Damp Heat	CECC 42000, Test 4.17, Test Ca, IEC 68-2-3 56 days, 40°C, 93% RH	$\lvert DV_n/V_n$ @ 1 mA$\rvert$ < 10% R > 10 MW
Mechanical Reliability	Solderability	CECC 42000, Test 4.10.1., Test Ta, IEC 68-2-20 solder bath method, 235°C ± 5°C, 2 s	Solderable at shipment and after 6 months of storage
	Resistance to Soldering Heat	CECC 42000, Test 4.10.2., Test Tb, IEC 68-2-20 260°C ± 5°C, 10 s	$\lvert DV_n/V_n$ @ 1 mA$\rvert$ < 5%
	Robustness of Termination	CECC 42000, Test 4.11 Test Ua, IEC 68-2-21	$\lvert DV_n/V_n$ @ 1 mA$\rvert$ < 5%
	Vibration	CECC 42000, Test 4.15., Test Fc, IEC 68-2-6, Frequency range 10 to 55 Hz Amplitude 0.75 mm or 98 m/s² Total duration 6 h (3 x 2 h) Waveshape - half sine	$\lvert DV_n/V_n$ @ 1 mA$\rvert$ < 10% no visible damage
	Mechanical Shock	CECC 42000, Test 4.14, Test Ea, IEC 68-2-27 Acceleration = 490 m/s², Pulse duration = 11 ms, Waveshape - half sine Number of shocks = 3 x 6	$\lvert DV_n/V_n$ @ 1 mA$\rvert$ < 10% no visible damage
Fire Hazard	Flammability Test	CECC 42000, Test 4.18.1 or IEC 695-2-2 Needle Flame Test, 10 s	Maximum 5 s

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GENERAL COMMENTS

Popular soldering techniques used for surface mount components are Wave, Infrared and Vapor Phase Reflow processes.

WAVE SOLDERING

This process is generally associated with discrete components mounted on the underside of printed circuit boards or for large top-side components with bottom-side mounting tabs to be attached, such as the frames of transformers, relays, connectors, etc. SMD varistors to be wave soldered are first glued to the circuit board, usually by an epoxy adhesive. When the PCB has been fully populated and an appropriate time is allowed for adhesive curing, the completed assembly is then placed on a conveyor and run through a single or double wave process.

INFRARED AND VAPOR PHASE

These reflow processes are typically associated with top-side component placement. This technique utilizes a mixture of adhesive and solder compounds (an sometimes fluxes) that are blended into a paste. The paste is then screened onto PCB soldering pads specifically designed to accept a particular sized SMD component. Recommended solder paste wet layer thickness is 25 to 40 micrometers. Once the circuit board is fully populated with SMD components, it is placed in a reflow environment, either a heating tunnel or vapor phase chamber, where the paste is heated to slightly above its eutectic temperature. When the solder paste reflows, the SMD components are attached to the solder pads.

SOLDER FLUXES

Solder fluxes are generally applied to populated circuit boards to prevent oxides from forming during the heating process and to facilitate the flowing of the solder. Solder fluxes can be either a part of the solder paste compound or can be separate materials, usually fluids. Recommended fluxes are:

- Non-activated (R) fluxes, whenever possible
- Mildly activated (RMA) fluxes of class L3CN (e.g., Multicore No Clean, Low Residue X33F8S-07i flux)
- Class ORLO (e.g., Kester VOC Free, No Clean 977 flux)

Activated (RA), water soluble or strong acidic fluxes with chlorine content > 0.2 wt.% are ***NOT RECOMMENDED***. Use of such fluxes could create high leakage current paths along the body of the varistor components.

When a flux is applied prior to wave soldering, it is important to completely dry any residual flux solvents prior to the soldering process.

THERMAL SHOCK

To avoid the possibility of generating stresses in the varistor chip due to thermal shock, a preheat stage to within 100 C of the peak soldering process temperature is recommended. Additionally, SMD varistors should not be subjected to a temperature gradient greater than 4 C/sec, with an ideal gradient being 2 C/sec. Peak temperatures should be controlled. Examples for soldering conditions for SMD varistors are shown in Fig.1 through 3.

Whenever several different types of SMD components are being soldered, each having a specific soldering profile, the soldering profile with the least heat and the minimum amount of heating time is recommended. Once soldering has been completed, it is necessary to minimize the possibility of thermal shock by allowing a hot PCB to cool to less than 50 C before cleaning.

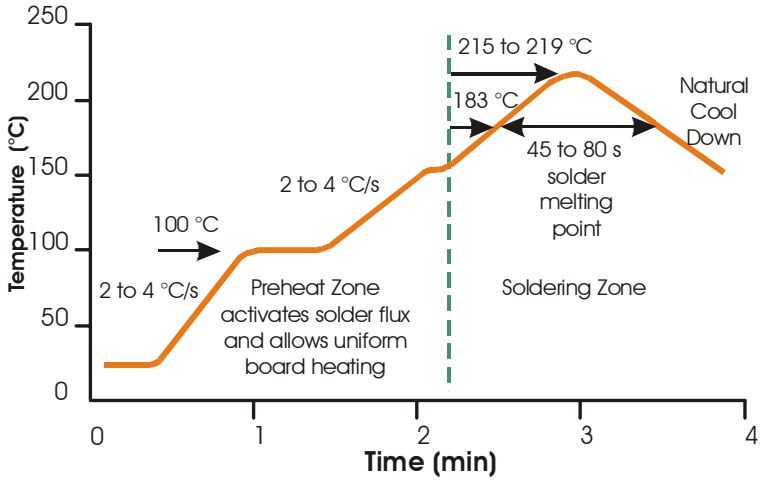

Fig. 1. Infrared Reflow Temperature Profile

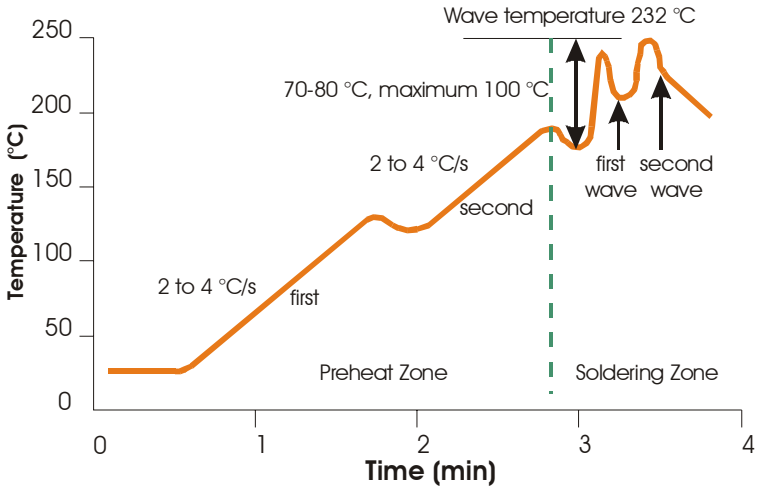

Fig. 2. Wave Soldering Temperature Profile

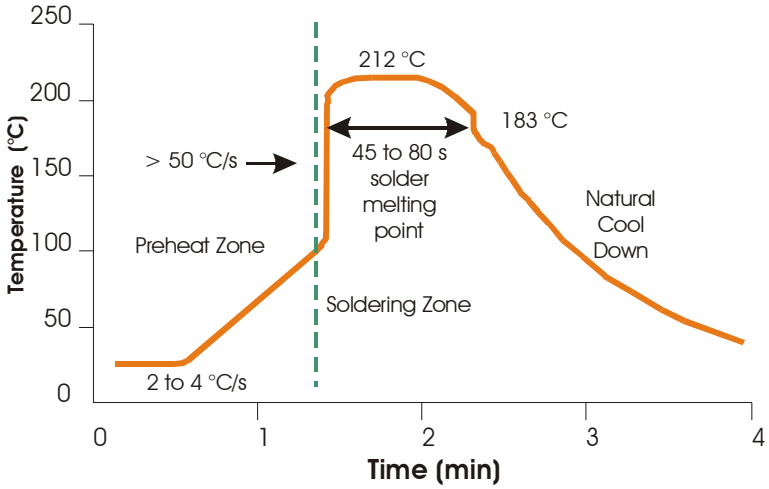

Fig. 3. Vapour Phase Temperature Profile

INSPECTION CRITERIA FOR WAVE AND REFLOW PROCESSES

The inspection criteria to determine acceptable solder joints, when Wave, Infrared or Vapor Phase Reflow processes are used, will depend on several key variables, principally termination materials and process profiles.

WAVE AND IR REFLOW: Silver/Palladium (AgPd) and Nickel-Barrier (NiSn) Terminations

Typical “before” and “after” soldering results are given in Fig. 4. Both nickel-barrier and silver/palladium terminated varistors form a reliable electrical contact and metallurgical bond between the end terminations and the solder pads. The bond between these two metallic surfaces is exceptionally strong and has been tested by both vertical pull and lateral (horizontal) push tests. The results, in both cases, exceed established industry standards for adhesion.

The solder joint *appearance* of a nickel-barrier terminated versus a silver/palladium terminated varistor will be slightly different. Solder forms a metallurgical junction with the thin tin-alloy (over the nickel-barrier layer), and due to its small volume “climbs” the outer surface of the termination, forming a classical meniscus. Due to the surface tension characteristics of silver/palladium terminations, the meniscus will be slightly lower. This optical appearance difference should be taken into consideration when programming visual inspection of the PCB after soldering.

VAPOR PHASE REFLOW: Silver/Palladium (AgPd) Terminations

When the peak soldering temperature of a Vapor Phase Reflow process is less than 210 C, a phenomenon known as “mirror” or “negative” meniscus results. Solder forms a metallurgical junction with the entire volume of the end termination, i.e., it diffuses from pad to end termination across the inner side, forming a “mirror” or “negative” meniscus. The height of the solder penetration can be clearly seen on the end termination (see Fig. 5) and is always higher than 30% of the chip height.

VAPOR PHASE REFLOW: Nickel-Barrier (NiSn) Terminations

Similar to the explanation given above for solder climbing, the outer surface of the electro-plated tin-alloy layer (over the nickel-barrier layer) of the termination, a classical meniscus is formed as demonstrated in Fig. 5.

Silver/Palladium (AgPd) & Nickel-Barrier (NiSn) End Terminations

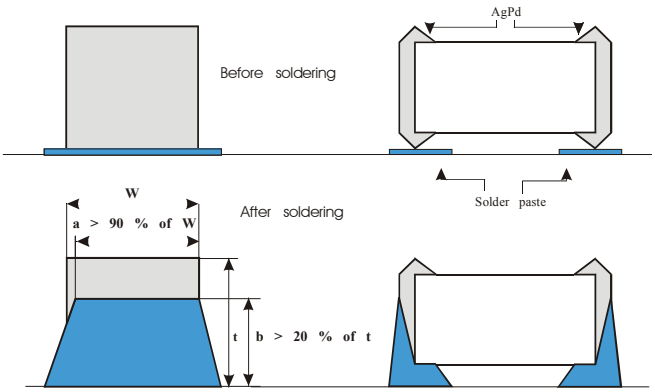

Fig. 4. Soldering Criterion in Case of Wave and IR Reflow Soldering

Silver/Palladium (AgPd) End Termination & Nickel-Barrier End Termination

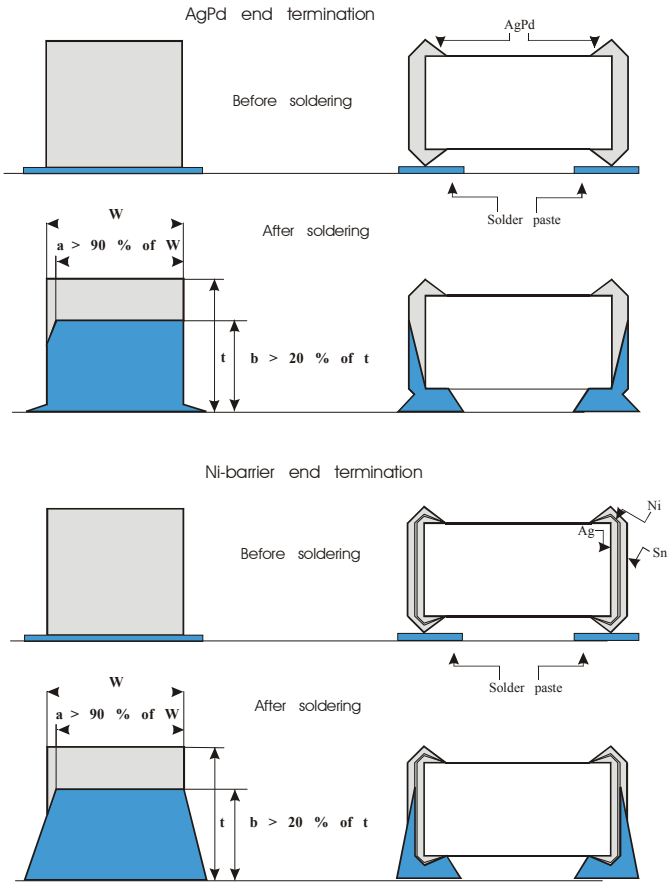

Fig. 5. Soldering Criterion in case of Vapor Soldering

SILVER/PALLADIUM (AgPd) TERMINATIONS

KEKO-VARICON chip varistors with AgPd terminations have soldering performances very close to Ni-barrier terminations. A comparison of soldering curves typical of each type of termination material is shown in the chart below, entitled Soldering Temperature-Time Characteristics

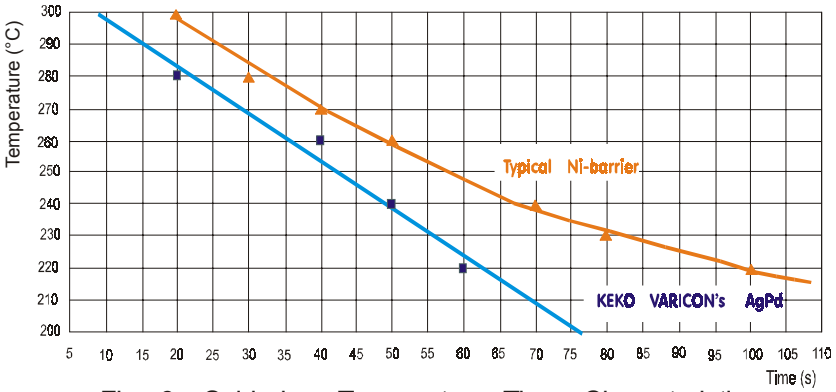

Fig. 6. Soldering Temperature -Time Characteristics

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ENVIRONMENTALLY FRIENDLY

Since the application of AgPd terminations on KEKO-VARICON chips does not require the use of problematic nickel and tin-alloy electroplating processes, these varistors are truly considered *environmentally friendly*.

SOLDER TESTS AND RETAINED SAMPLES

Solder tests are preformed on each production lot as shown in the following chart. Test results and accompanying samples are retained for a minimum of two (2) years. Solderability of a specific lot can be checked at any time within this period should a customer require this information.

Test Parameter	Resistance to Flux	Solderability	Static Leaching	Dynamic Leacing
Soldering method	Dipping	Dipping	Dipping	Dipping with agitation
Flux	L3CN ORLO	L3CN, ORLO, R	L3CN, ORLO, R	L3CN, ORLO, R
Solder	62Sn/36 Pb/2 Ag	62Sn/36 Pb/2 Ag	62Sn/36 Pb/2 Ag	62Sn/36 Pb/2 Ag
Soldering termperature (C)	235 ± 5	235 ± 5	260 ± 5	235 ± 5
Soldering time	2	2	10	>15
Burn-in Conditions	V_{DC}max, 48 h	-	-	-
Acceptance criterion	V_N < 5% I_{DC} must stay unchanged	> 95% of end terminal must be covered by solder	> 95% of end terminal must be covered by solder	> 95% of end terminal must be covered by solder

REWORK CRITERIA – SOLDERING IRON

Unless absolutely necessary, the use of soldering irons is NOT recommended for reworking varistor chips. If no other means of rework is available, the following criteria must be strictly followed:

- Do not allow the tip of the iron to directly contact the top of the chip
- Do not exceed the following soldering iron specifications:
  - Output Power: 30 Watts maximum
  - Temperature of Soldering Iron Tip: 280 C maximum
  - Soldering Time: 10 Seconds maximum

STORAGE CONDITIONS

SMD varistors should be used within 1 year of purchase to avoid possible soldering problems caused by oxidized terminals. The storage environment should be controlled, with humidity less than 40%. Varistor chips should always be stored in their original packaged unit.

Where varistor chips have been in storage for more than 1 year, and where there is evidence of solderability difficulties, KEKO-VARICON can “refresh” the terminations to eliminate these problems.