

AD8615/AD8616/AD8618

FEATURES

- Low offset voltage: 65 μ V maximum**
- Single-supply operation: 2.7 V to 5.0 V**
- Low noise: 8 nV/ $\sqrt{\text{Hz}}$**
- Wide bandwidth: >20 MHz**
- Slew rate: 12 V/ μ s**
- High output current: 150 mA**
- No phase reversal**
- Low input bias current: 1 pA**
- Low supply current: 2 mA**
- Unity-gain stable**

APPLICATIONS

- Barcode scanners**
- Battery-powered instrumentation**
- Multipole filters**
- Sensors**
- ASIC input or output amplifiers**
- Audio**
- Photodiode amplification**

GENERAL DESCRIPTION

The AD8615/AD8616/AD8618 are single/dual/quad, rail-to-rail, input and output, single-supply amplifiers featuring very low offset voltage, wide signal bandwidth, and low input voltage and current noise. The parts use a patented trimming technique that achieves superior precision without laser trimming. The AD8615/AD8616/AD8618 are fully specified to operate from 2.7 V to 5 V single supplies.

The combination of >20 MHz bandwidth, low offset, low noise, and low input bias current makes these amplifiers useful in a wide variety of applications. Filters, integrators, photodiode amplifiers, and high impedance sensors all benefit from the combination of performance features. AC applications benefit from the wide bandwidth and low distortion. The AD8615/AD8616/AD8618 offer the highest output drive capability of the DigiTrim[®] family, which is excellent for audio line drivers and other low impedance applications.

Applications for the parts include portable and low powered instrumentation, audio amplification for portable devices, portable phone headsets, bar code scanners, and multipole filters. The ability to swing rail-to-rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in single-supply systems.

Rev. E

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PIN CONFIGURATIONS

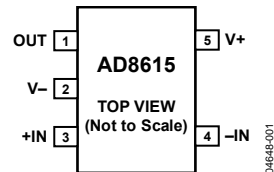


Figure 1. 5-Lead TSOT-23 (UJ-5)

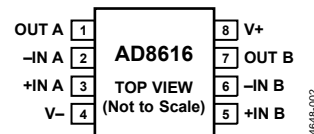


Figure 2. 8-Lead MSOP (RM-8)

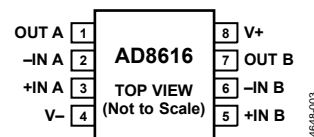


Figure 3. 8-Lead SOIC (R-8)

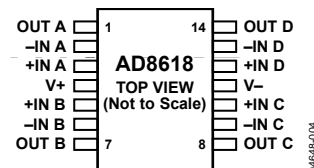


Figure 4. 14-Lead TSSOP (RU-14)

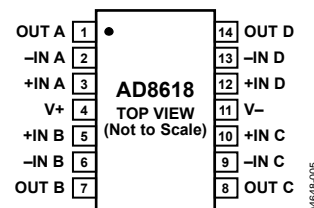


Figure 5. 14-Lead SOIC (R-14)

The AD8615/AD8616/AD8618 are specified over the extended industrial temperature range (-40°C to $+125^{\circ}\text{C}$). The AD8615 is available in 5-lead TSOT-23 package. The AD8616 is available in 8-lead MSOP and narrow SOIC surface-mount packages; the MSOP version is available in tape and reel only. The AD8618 is available in 14-lead SOIC and TSSOP packages.

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REVISION HISTORY

9/08—Rev. D to Rev. E

Changes to General Description Section	1
Updated Outline Dimensions	15
Changes to Ordering Guide	17

5/08—Rev. C to Rev. D

Changes to Layout	1
Changes to Figure 38.....	11
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Changes to Layout	15
Changes to Layout	16

6/05—Rev. B to Rev. C

Change to Table 1	3
Change to Table 2	4
Change to Figure 20	8

1/05—Rev. A to Rev. B

Added AD8615	Universal
Changes to Figure 12.....	8
Deleted Figure 19; Renumbered Subsequently.....	8
Changes to Figure 20.....	9
Changes to Figure 29.....	10
Changes to Figure 31.....	11
Deleted Figure 34; Renumbered Subsequently.....	11
Deleted Figure 35; Renumbered Subsequently.....	35

4/04—Rev. 0 to Rev. A

Added AD8618	Universal
Updated Outline Dimensions	16

1/04—Revision 0: Initial Version

SPECIFICATIONS

$V_S = 5\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage, AD8616/AD8618	V_{OS}	$V_S = 3.5\text{ V}$ at $V_{CM} = 0.5\text{ V}$ and 3.0 V		23	60	μV
Offset Voltage, AD8615				23	100	μV
		$V_{CM} = 0\text{ V}$ to 5 V		80	500	μV
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			800	μV
Offset Voltage Drift, AD8616/AD8618	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.5	7	$\mu\text{V}/^\circ\text{C}$
Offset Voltage Drift, AD8615				3	10	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B			0.2	1	pA
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			50	pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			550	pA
Input Offset Current	I_{OS}			0.1	0.5	pA
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$			50	pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			250	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V}$ to 4.5 V	80	100		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V}$ to 5 V	105	1500		V/mV
Input Capacitance	C_{DIFF}			2.5		pF
	C_{CM}			6.7		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$	4.98	4.99		V
		$I_L = 10\text{ mA}$	4.88	4.92		V
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.7			V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$		7.5	15	mV
		$I_L = 10\text{ mA}$		70	100	mV
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			200	mV
Output Current	I_{OUT}			± 150		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_V = 1$		3		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V}$ to 5.5 V	70	90		dB
Supply Current per Amplifier	I_{SY}	$V_O = 0\text{ V}$		1.7	2	mA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			2.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		12		$\text{V}/\mu\text{s}$
Settling Time	t_s	To 0.01%		<0.5		μs
Gain Bandwidth Product	GBP			24		MHz
Phase Margin	ϕ_m			63		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	$e_n\text{ p-p}$	0.1 Hz to 10 Hz		2.4		μV
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		10		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		7		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$
Channel Separation	C_S	$f = 10\text{ kHz}$		-115		dB
		$f = 100\text{ kHz}$		-110		dB

AD8615/AD8616/AD8618

$V_S = 2.7\text{ V}$, $V_{CM} = V_S/2$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage, AD8616/AD8618	V_{OS}	$V_S = 3.5\text{ V}$ at $V_{CM} = 0.5\text{ V}$ and 3.0 V		23	65	μV
Offset Voltage, AD8615				23	100	μV
		$V_{CM} = 0\text{ V}$ to 2.7 V		80	500	μV
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			800	μV
Offset Voltage Drift, AD8616/AD8618	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.5	7	$\mu\text{V}/^\circ\text{C}$
Offset Voltage Drift, AD8615				3	10	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.2	1	pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			50	pA
					550	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$		0.1	0.5	pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			50	pA
					250	pA
Input Voltage Range			0		2.7	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V}$ to 2.7 V	80	100		dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_O = 0.5\text{ V}$ to 2.2 V	55	150		V/mV
Input Capacitance	C_{DIFF} C_{CM}			2.5		pF pF
				7.8		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.65	2.68		V
			2.6			V
Output Voltage Low	V_{OL}	$I_L = 1\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		11	25	mV
					30	mV
Output Current	I_{OUT}			± 50		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_V = 1$		3		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V}$ to 5.5 V	70	90		dB
Supply Current per Amplifier	I_{SY}	$V_O = 0\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.7	2	mA
					2.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$		12		$\text{V}/\mu\text{s}$
Settling Time	t_S	To 0.01%		<0.3		μs
Gain Bandwidth Product	GBP			23		MHz
Phase Margin	ϕ_m			42		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise	e_n p-p	0.1 Hz to 10 Hz		2.1		μV
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		10		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		7		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 1\text{ kHz}$		0.05		$\text{pA}/\sqrt{\text{Hz}}$
Channel Separation	C_S	$f = 10\text{ kHz}$		-115		dB
		$f = 100\text{ kHz}$		-110		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to V_S
Differential Input Voltage	± 3 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+125^{\circ}\text{C}$
Lead Temperature (Soldering, 60 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for a device soldered in a circuit board for surface-mount packages.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead TSOT-23 (UJ)	207	61	$^{\circ}\text{C}/\text{W}$
8-Lead MSOP (RM)	210	45	$^{\circ}\text{C}/\text{W}$
8-Lead SOIC (R)	158	43	$^{\circ}\text{C}/\text{W}$
14-Lead SOIC (R)	120	36	$^{\circ}\text{C}/\text{W}$
14-Lead TSSOP (RU)	180	35	$^{\circ}\text{C}/\text{W}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

