

ADCMP580/ADCMP581/ADCMP582

FEATURES

- 180 ps propagation delay**
- 25 ps overdrive and slew rate dispersion**
- 8 GHz equivalent input rise time bandwidth**
- 100 ps minimum pulse width**
- 37 ps typical output rise/fall**
- 10 ps deterministic jitter (DJ)**
- 200 fs random jitter (RJ)**
- 2 V to +3 V input range with +5 V/-5 V supplies**
- On-chip terminations at both input pins**
- Resistor-programmable hysteresis**
- Differential latch control**
- Power supply rejection > 70 dB**

APPLICATIONS

- Automatic test equipment (ATE)**
- High speed instrumentation**
- Pulse spectroscopy**
- Medical imaging and diagnostics**
- High speed line receivers**
- Threshold detection**
- Peak and zero-crossing detectors**
- High speed trigger circuitry**
- Clock and data signal restoration**

GENERAL DESCRIPTION

The ADCMP580/ADCMP581/ADCMP582 are ultrafast voltage comparators fabricated on the Analog Devices, Inc. proprietary XFCB3 Silicon Germanium (SiGe) bipolar process. The ADCMP580 features CML output drivers, the ADCMP581 features reduced swing ECL (negative ECL) output drivers, and the ADCMP582 features reduced swing PECL (positive ECL) output drivers.

All three comparators offer 180 ps propagation delay and 100 ps minimum pulse width for 10 Gbps operation with 200 fs random jitter (RJ). Overdrive and slew rate dispersion are typically less than 15 ps.

The ± 5 V power supplies enable a wide -2 V to +3 V input range with logic levels referenced to the CML/NECL/PECL outputs. The inputs have 50 Ω on-chip termination resistors with the optional capability to be left open (on an individual pin basis) for applications requiring high impedance input.

FUNCTIONAL BLOCK DIAGRAM

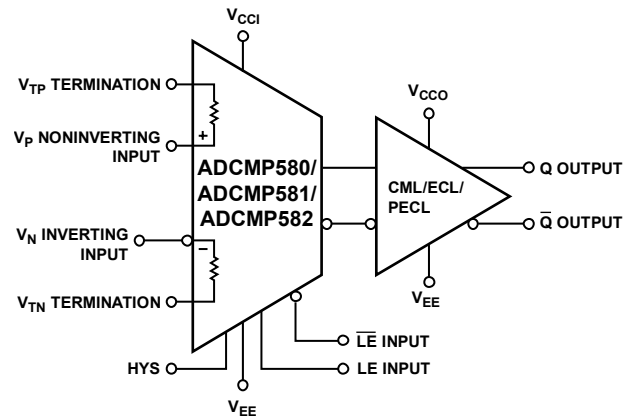


Figure 1.

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The CML output stage is designed to directly drive 400 mV into 50 Ω transmission lines terminated to ground. The NECL output stages are designed to directly drive 400 mV into 50 Ω terminated to -2 V. The PECL output stages are designed to directly drive 400 mV into 50 Ω terminated to $V_{CCO} - 2$ V. High speed latch and programmable hysteresis are also provided. The differential latch input controls are also 50 Ω terminated to an independent V_{TT} pin to interface to either CML or ECL or to PECL logic.

The ADCMP580/ADCMP581/ADCMP582 are available in a 16-lead LFCSP_VQ.

Rev. A

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REVISION HISTORY

8/07—Rev. 0 to Rev. A

Changes to Figure 1	1
Changes to Table 4.....	7
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Changes to Figure 21, Figure 22, and Figure 23	10
Changes to Using/Disabling the Latch Feature	11
Changes to Comparator Hysteresis Section and Figure 29.....	13
Changes to Ordering Guide	14

7/05—Revision 0: Initial Version

SPECIFICATIONS

$V_{CCI} = 5.0\text{ V}$; $V_{EE} = -5.0\text{ V}$; $V_{CCO} = 3.3\text{ V}$; $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DC INPUT CHARACTERISTICS						
Input Voltage Range	V_P, V_N		-2.0		+3.0	V
Input Differential Range			-2.0		+2.0	V
Input Offset Voltage	V_{OS}		-10.0	±4	+10.0	mV
Offset Voltage Temperature Coefficient	$\Delta V_{OS}/dT$			10		$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_P, I_N	Open termination		15	30.0	μA
Input Bias Current Temperature Coefficient	$\Delta I_B/dT$			50		$\text{nA}/^\circ\text{C}$
Input Offset Current				+2	±5.0	μA
Input Resistance				47 to 53		Ω
Input Resistance, Differential Mode		Open termination		50		$\text{k}\Omega$
Input Resistance, Common Mode		Open termination		500		$\text{k}\Omega$
Active Gain	A_V			48		dB
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -2.0\text{ V to }+3.0\text{ V}$		60		dB
Hysteresis		$R_{HYS} = \infty$		1		mV
LATCH ENABLE CHARACTERISTICS						
Latch Enable Input Impedance	Z_{IN}	Each pin, V_{TT} at ac ground		47 to 53		Ω
Latch-to-Output Delay	t_{PLOH}, t_{PLOL}	$V_{OD} = 200\text{ mV}$		175		ps
Latch Minimum Pulse Width	t_{PL}	$V_{OD} = 200\text{ mV}$		100		ps
ADCMP580 (CML)						
Latch Enable Input Range			-0.8		0	V
Latch Enable Input Differential			0.2	0.4	0.5	V
Latch Setup Time	t_S	$V_{OD} = 200\text{ mV}$		95		ps
Latch Hold Time	t_H	$V_{OD} = 200\text{ mV}$		-90		ps
ADCMP581 (NECL)						
Latch Enable Input Range			-1.8		+0.8	V
Latch Enable Input Differential			0.2	0.4	0.5	V
Latch Setup Time	t_S	$V_{OD} = 200\text{ mV}$		70		ps
Latch Hold Time	t_H	$V_{OD} = 200\text{ mV}$		-65		ps
ADCMP582 (PECL)						
Latch Enable Input Range			$V_{CCO} - 1.8$		$V_{CCO} - 0.8$	V
Latch Enable Input Differential			0.2	0.4	0.5	V
Latch Setup Time	t_S	$V_{OD} = 200\text{ mV}$		30		ps
Latch Hold Time	t_H	$V_{OD} = 200\text{ mV}$		-25		ps
DC OUTPUT CHARACTERISTICS						
ADCMP580 (CML)						
Output Impedance	Z_{OUT}			50		Ω
Output Voltage High Level	V_{OH}	50 Ω to GND	-0.10	0	+0.03	V
Output Voltage Low Level	V_{OL}	50 Ω to GND	-0.50	-0.40	-0.35	V
Output Voltage Differential		50 Ω to GND	340	395	450	mV
ADCMP581 (NECL)						
Output Voltage High Level	V_{OH}	50 Ω to -2 V, $T_A = 125^\circ\text{C}$	-0.99	-0.87	-0.75	V
Output Voltage High Level	V_{OH}	50 Ω to -2 V, $T_A = 25^\circ\text{C}$	-1.06	-0.94	-0.82	V
Output Voltage High Level	V_{OH}	50 Ω to -2 V, $T_A = -55^\circ\text{C}$	-1.11	-0.99	-0.87	V
Output Voltage Low Level	V_{OL}	50 Ω to -2 V, $T_A = 125^\circ\text{C}$	-1.43	-1.26	-1.13	V
Output Voltage Low Level	V_{OL}	50 Ω to -2 V, $T_A = 25^\circ\text{C}$	-1.50	-1.33	-1.20	V
Output Voltage Low Level	V_{OL}	50 Ω to -2 V, $T_A = -55^\circ\text{C}$	-1.55	-1.38	-1.25	V
Output Voltage Differential		50 Ω to -2.0 V	340	395	450	mV

ADCMP580/ADCMP581/ADCMP582

Parameter	Symbol	Condition	Min	Typ	Max	Unit
ADCMP582 (PECL)						
Output Voltage High Level	V_{OH}	$V_{CCO} = 3.3\text{ V}$ 50 Ω to $V_{CCO} - 2\text{ V}$, $T_A = 125^\circ\text{C}$	$V_{CCO} - 0.99$	$V_{CCO} - 0.87$	$V_{CCO} - 0.75$	V
Output Voltage High Level	V_{OH}	50 Ω to $V_{CCO} - 2\text{ V}$, $T_A = 25^\circ\text{C}$	$V_{CCO} - 1.06$	$V_{CCO} - 0.94$	$V_{CCO} - 0.82$	V
Output Voltage High Level	V_{OH}	50 Ω to $V_{CCO} - 2\text{ V}$, $T_A = -55^\circ\text{C}$	$V_{CCO} - 1.11$	$V_{CCO} - 0.99$	$V_{CCO} - 0.87$	V
Output Voltage Low Level	V_{OL}	50 Ω to $V_{CCO} - 2\text{ V}$, $T_A = 125^\circ\text{C}$	$V_{CCO} - 1.43$	$V_{CCO} - 1.26$	$V_{CCO} - 1.13$	V
Output Voltage Low Level	V_{OL}	50 Ω to $V_{CCO} - 2\text{ V}$, $T_A = 25^\circ\text{C}$	$V_{CCO} - 1.50$	$V_{CCO} - 1.33$	$V_{CCO} - 1.20$	V
Output Voltage Low Level	V_{OL}	50 Ω to $V_{CCO} - 2\text{ V}$, $T_A = -55^\circ\text{C}$	$V_{CCO} - 1.55$	$V_{CCO} - 1.35$	$V_{CCO} - 1.25$	V
Output Voltage Differential		50 Ω to $V_{CCO} - 2.0\text{ V}$	340	395	450	mV
AC PERFORMANCE						
Propagation Delay	t_{PD}	$V_{OD} = 500\text{ mV}$		180		ps
Propagation Delay Temperature Coefficient	$\Delta t_{PD}/dT$			0.25		ps/ $^\circ\text{C}$
Propagation Delay Skew—Rising Transition to Falling Transition		$V_{OD} = 500\text{ mV}$, 5 V/ns		10		ps
Overdrive Dispersion		50 mV < V_{OD} < 1.0 V		10		ps
		10 mV < V_{OD} < 200 mV		15		ps
Slew Rate Dispersion		2 V/ns to 10 V/ns		15		ps
Pulse Width Dispersion		100 ps to 5 ns		15		ps
Duty Cycle Dispersion 5% to 95%		1.0 V/ns, 15 MHz, $V_{CM} = 0.0\text{ V}$		10		ps
Common-Mode Dispersion		$V_{OD} = 0.2\text{ V}$, $-2\text{ V} < V_{CM} < 3\text{ V}$		5		ps/V
Equivalent Input Bandwidth ¹	BW_{EQ}	0.0 V to 400 mV input, $t_R = t_F = 25\text{ ps}$, 20/80		8		GHz
Toggle Rate		>50% output swing		12.5		Gbps
Deterministic Jitter	DJ	$V_{OD} = 500\text{ mV}$, 5 V/ns, PRBS ³¹ – 1 NRZ, 5 Gbps		15		ps
Deterministic Jitter	DJ	$V_{OD} = 200\text{ mV}$, 5 V/ns, PRBS ³¹ – 1 NRZ, 10 Gbps		25		ps
RMS Random Jitter	RJ	$V_{OD} = 200\text{ mV}$, 5 V/ns, 1.25 GHz		0.2		ps
Minimum Pulse Width	PW_{MIN}	$\Delta t_{PD} < 5\text{ ps}$		100		ps
Minimum Pulse Width	PW_{MIN}	$\Delta t_{PD} < 10\text{ ps}$		80		ps
Rise/Fall Time	t_R, t_F	20/80		37		ps
POWER SUPPLY						
Positive Supply Voltage	V_{CCI}		+4.5	+5.0	+5.5	V
Negative Supply Voltage	V_{EE}		-5.5	-5.0	-4.5	V
ADCMP580 (CML)						
Positive Supply Current	I_{VCCI}	$V_{CCI} = 5.0\text{ V}$, 50 Ω to GND		6	8	mA
Negative Supply Current	I_{VEE}	$V_{EE} = -5.0\text{ V}$, 50 Ω to GND	-50	-40	-34	mA
Power Dissipation	P_D	50 Ω to GND		230	260	mW
ADCMP581 (NECL)						
Positive Supply Current	I_{VCCI}	$V_{CCI} = 5.0\text{ V}$, 50 Ω to -2 V		6	8	mA
Negative Supply Current	I_{VEE}	$V_{EE} = -5.0\text{ V}$, 50 Ω to -2 V	-35	-25	-19	mA
Power Dissipation	P_D	50 Ω to -2 V		155	200	mW
ADCMP582 (PECL)						
Logic Supply Voltage	V_{CCO}		+2.5	+3.3	+5.0	V
Input Supply Current	I_{VCCI}	$V_{CCI} = 5.0\text{ V}$, 50 Ω to $V_{CCO} - 2\text{ V}$		6	8	mA
Output Supply Current	I_{VCCO}	$V_{CCO} = 5.0\text{ V}$, 50 Ω to $V_{CCO} - 2\text{ V}$		44	55	mA
Negative Supply Current	I_{VEE}	$V_{EE} = -5.0\text{ V}$, 50 Ω to $V_{CCO} - 2\text{ V}$	-35	-25	-19	mA
Power Dissipation	P_D	50 Ω to $V_{CCO} - 2\text{ V}$		310	350	mW
Power Supply Rejection (V_{CCI})	PSR_{VCCI}	$V_{CCI} = 5.0\text{ V} + 5\%$		-75		dB
Power Supply Rejection (V_{EE})	PSR_{VEE}	$V_{EE} = -5.0\text{ V} + 5\%$		-60		dB
Power Supply Rejection (V_{CCO})	PSR_{VCCO}	$V_{CCO} = 3.3\text{ V} + 5\%$ (ADCMP582)		-75		dB

¹ Equivalent input bandwidth assumes a simple first-order input response and is calculated with the following formula: $BW_{EQ} = 0.22/(t_{rCOMP}^2 - t_{rIN}^2)$, where t_{rIN} is the 20/80 transition time of a quasi-Gaussian input edge applied to the comparator input and t_{rCOMP} is the effective transition time digitized by the comparator.

TIMING INFORMATION

Figure 2 shows the ADCMP580/ADCMP581/ADCMP582 compare and latch timing relationships. Table 2 provides the definitions of the terms shown in Figure 2.

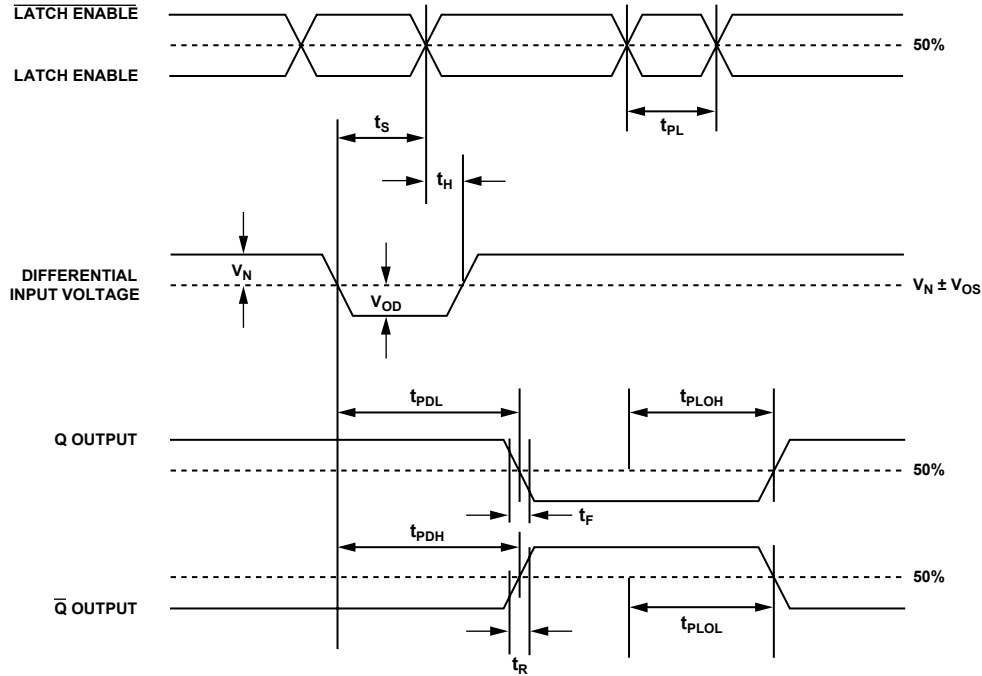


Figure 2. Comparator Timing Diagram

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Table 2. Timing Descriptions

Symbol	Timing	Description
t_{PDH}	Input-to-Output High Delay	Propagation delay measured from the time the input signal crosses the reference (\pm the input offset voltage) to the 50% point of an output low-to-high transition.
t_{PDL}	Input-to-Output Low Delay	Propagation delay measured from the time the input signal crosses the reference (\pm the input offset voltage) to the 50% point of an output high-to-low transition.
t_{PLOH}	Latch Enable-to-Output High Delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition.
t_{PLOL}	Latch Enable-to-Output Low Delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition.
t_H	Minimum Hold Time	Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs.
t_{PL}	Minimum Latch Enable Pulse Width	Minimum time that the latch enable signal must be high to acquire an input signal change.
t_S	Minimum Setup Time	Minimum time before the negative transition of the latch enable signal that an input signal change must be present to be acquired and held at the outputs.
t_R	Output Rise Time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points.
t_F	Output Fall Time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points.
V_N	Normal Input Voltage	Difference between the input voltages V_P and V_N for output true.
V_{OD}	Voltage Overdrive	Difference between the input voltages V_P and V_N for output false.

ADCMP580/ADCMP581/ADCMP582

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
SUPPLY VOLTAGES	
Positive Supply Voltage (V_{CC1} to GND)	-0.5 V to +6.0 V
Negative Supply Voltage (V_{EE} to GND)	-6.0 V to +0.5 V
Logic Supply Voltage (V_{CC0} to GND)	-0.5 V to +6.0 V
INPUT VOLTAGES	
Input Voltage	-3.0 V to +4.0 V
Differential Input Voltage	-2 V to +2 V
Input Voltage, Latch Enable	-2.5 V to +5.5 V
HYSTERESIS CONTROL PIN	
Applied Voltage (HYS to V_{EE})	-5.5 V to +0.5 V
Maximum Input/Output Current	1 mA
OUTPUT CURRENT	
ADCMP580 (CML)	-25 mA
ADCMP581 (NECL)	-40 mA
ADCMP582 (PECL)	-40 mA
TEMPERATURE	
Operating Temperature Range, Ambient	-40°C to +125°C
Operating Temperature, Junction	125°C
Storage Temperature Range	-65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CONSIDERATIONS

The ADCMP580/ADCMP581/ADCMP582 16-lead LFCSP option has a θ_{JA} (junction-to-ambient thermal resistance) of 70°C/W in still air.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

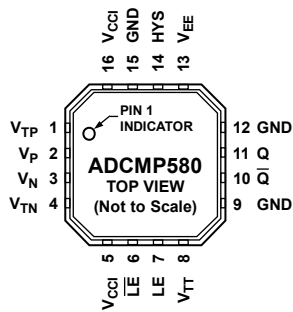


Figure 3. ADCMP580 Pin Configuration

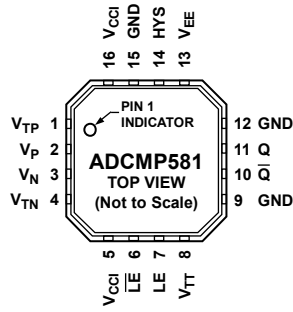


Figure 4. ADCMP581 Pin Configuration

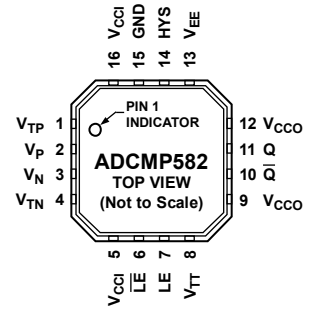


Figure 5. ADCMP582 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V _{TP}	Termination Resistor Return Pin for VP Input.
2	V _P	Noninverting Analog Input.
3	V _N	Inverting Analog Input.
4	V _{TN}	Termination Resistor Return Pin for V _N Input.
5, 16	V _{CCI}	Positive Supply Voltage.
6	\overline{LE}	Latch Enable Input Pin, Inverting Side. In compare mode ($\overline{LE} = \text{low}$), the output tracks changes at the input of the comparator. In latch mode ($\overline{LE} = \text{high}$), the output reflects the input state just prior to the comparator being placed into latch mode. \overline{LE} must be driven in complement with LE.
7	LE	Latch Enable Input Pin, Noninverting Side. In compare mode (LE = high), the output tracks changes at the input of the comparator. In latch mode (LE = low), the output reflects the input state just prior to the comparator being placed into latch mode. LE must be driven in complement with \overline{LE} .
8	V _{TT}	Termination Return Pin for the LE/ \overline{LE} Input Pins. For the ADCMP580 (CML output stage), this pin should be connected to the GND ground. For the ADCMP581 (ECL output stage), this pin should be connected to the -2 V termination potential. For the ADCMP582 (PECL output stage), this pin should be connected to the V _{CCO} - 2 V termination potential.
9, 12	GND/V _{CCO}	Digital Ground Pin/Positive Logic Power Supply Terminal. For the ADCMP580/ADCMP581, this pin should be connected to the GND pin. For the ADCMP582, this pin should be connected to the positive logic power V _{CCO} supply.
10	\overline{Q}	Inverting Output. \overline{Q} is logic low if the analog voltage at the noninverting input, V _P , is greater than the analog voltage at the inverting input, V _N , provided that the comparator is in compare mode. See the LE/ \overline{LE} descriptions (Pin 6 to Pin 7) for more information.
11	Q	Noninverting Output. Q is logic high if the analog voltage at the noninverting input, V _P , is greater than the analog voltage at the inverting input, V _N , provided that the comparator is in compare mode. See the LE/ \overline{LE} descriptions (Pin 6 to Pin 7) for more information.
13	V _{EE}	Negative Power Supply.
14	HYS	Hysteresis Control. Leave this pin disconnected for zero hysteresis. Connect this pin to the V _{EE} supply with a suitably sized resistor to add the desired amount of hysteresis. Refer to Figure 9 for proper sizing of the HYS hysteresis control resistor.
15	GND	Analog Ground.
Heat Sink Paddle	N/C	The metallic back surface of the package is not electrically connected to any part of the circuit. It can be left floating for optimal electrical isolation between the package handle and the substrate of the die. It can also be soldered to the application board if improved thermal and/or mechanical stability is desired. Exposed metal at package corners is connected to the heat sink paddle.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC1} = 5.0\text{ V}$, $V_{EE} = -5.0\text{ V}$, $V_{CC0} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

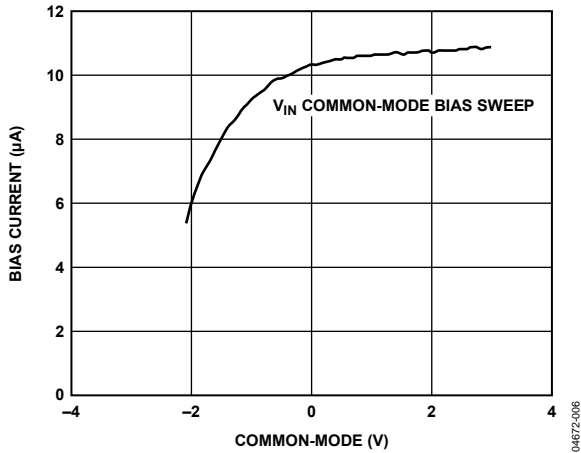


Figure 6. Bias Current vs. Common-Mode Voltage

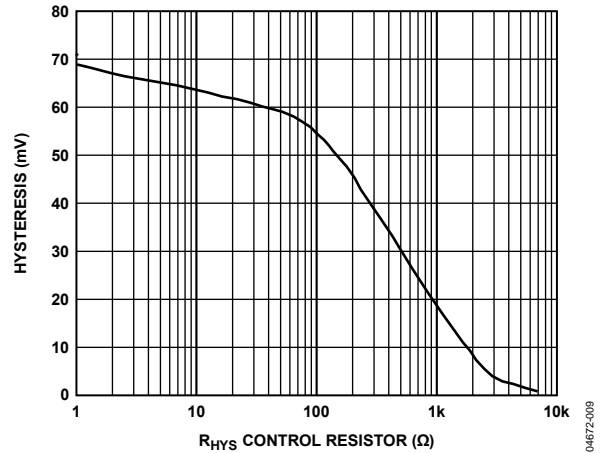


Figure 9. Hysteresis vs. R_{HYS} Control Resistor

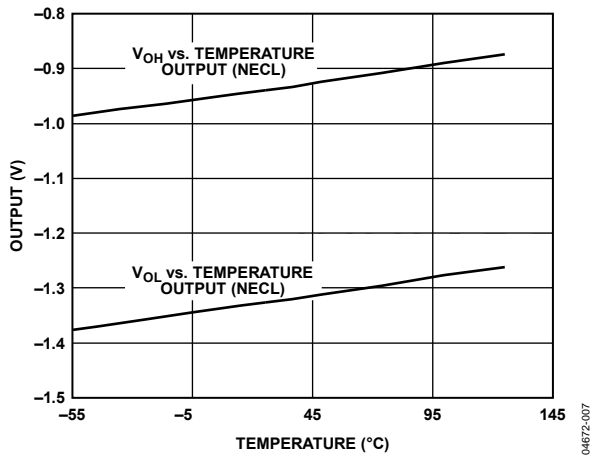


Figure 7. ADCMP581 Output Voltage vs. Temperature

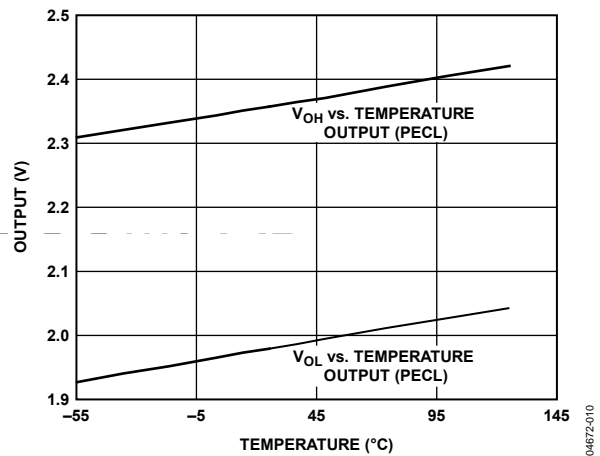


Figure 10. ADCMP582 Output Voltage vs. Temperature

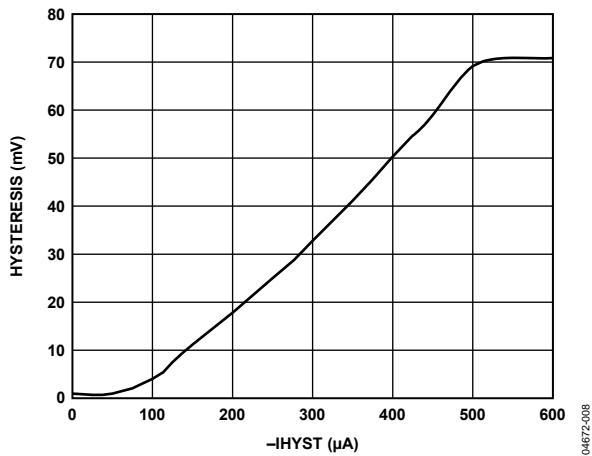


Figure 8. Hysteresis vs. $-IHYST$

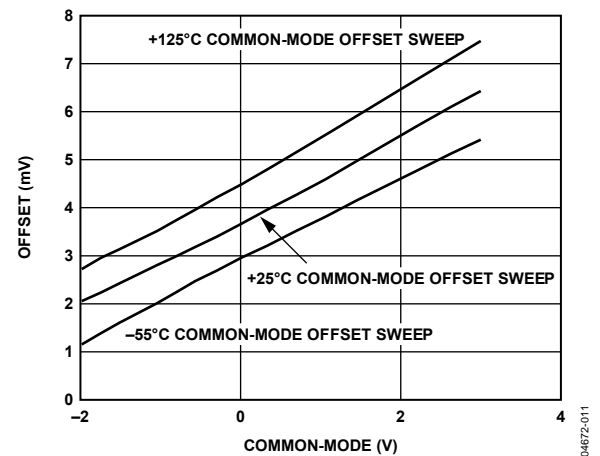


Figure 11. A Typical V_{OS} vs. Common-Mode Voltage

