

256K (32K x 8) Static RAM

Features

- High speed
 - 55 ns
- Temperature Ranges
 - Commercial: 0°C to 70°C
 - Industrial: -40°C to 85°C
 - Automotive: -40°C to 125°C
- Voltage range
 - 4.5V – 5.5V
- Low active power and standby power
- Easy memory expansion with \overline{CE} and \overline{OE} features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Available in a Pb-free and non Pb-free standard 28-pin narrow SOIC, 28-pin TSOP-1, 28-pin Reverse TSOP-1 and 28-pin DIP packages

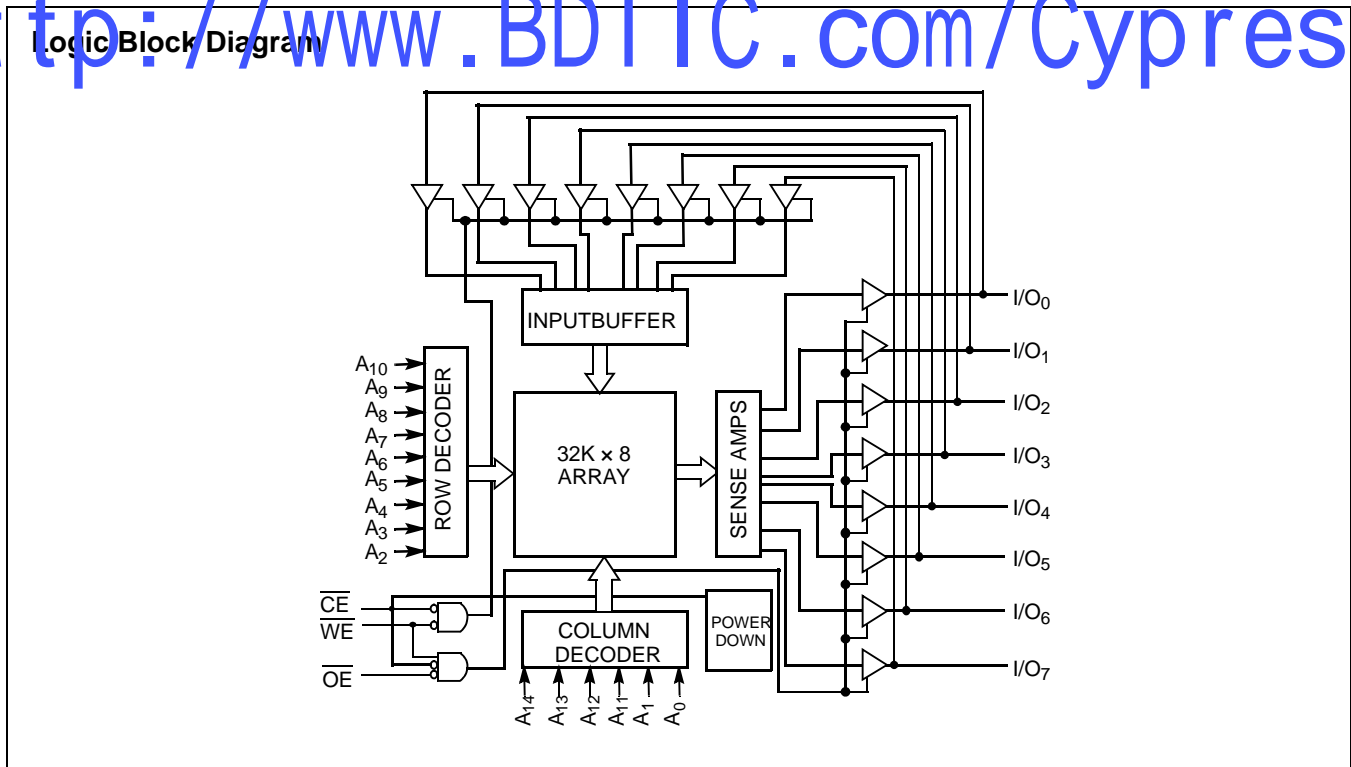
Functional Description^[1]

The CY62256 is a high-performance CMOS static RAM organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and active LOW output enable (\overline{OE}) and Tri-state drivers. This device has an automatic power-down feature, reducing the power consumption by 99.9% when deselected.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high-impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.

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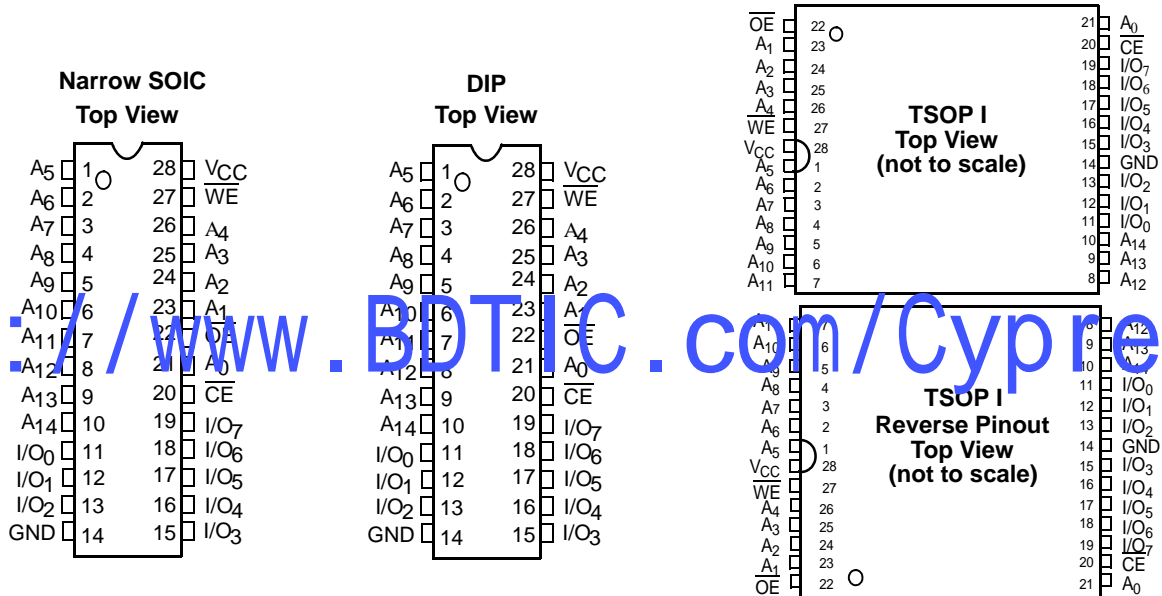


Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Product Portfolio

Product		V _{CC} Range (V)			Speed (ns)	Power Dissipation			
						Operating, I _{CC} (mA)		Standby, I _{SB2} (μA)	
		Min.	Typ. ^[2]	Max.		Typ. ^[2]	Max.	Typ. ^[2]	Max.
CY62256L	Com'l/Ind'l	4.5	5.0	5.5	55/70	25	50	2	50
CY62256LL	Commercial				70	25	50	0.1	5
CY62256LL	Industrial				55/70	25	50	0.1	10
CY62256LL	Automotive				55	25	50	0.1	15

Pin Configurations


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Pin Definitions

Pin Number	Type	Description
1–10, 21, 23–26	Input	A ₀ –A ₁₄ . Address Inputs
11–13, 15–19,	Input/Output	I/O ₀ –I/O ₇ . Data lines. Used as input or output lines depending on operation
27	Input/Control	WE. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
20	Input/Control	CE. When LOW, selects the chip. When HIGH, deselects the chip
22	Input/Control	OE. Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are Tri-stated, and act as input data pins
14	Ground	GND. Ground for the device
28	Power Supply	V _{CC} . Power supply for the device

Note:

2. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions (T_A = 25°C, V_{CC}). Parameters are guaranteed by design and characterization, and not 100% tested.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature -65°C to +150°C
- Ambient Temperature with Power Applied..... -55°C to +125°C
- Supply Voltage to Ground Potential (Pin 28 to Pin 14) -0.5V to +7V
- DC Voltage Applied to Outputs in High-Z State^[3] -0.5V to V_{CC} + 0.5V

- DC Input Voltage^[3] -0.5V to V_{CC} + 0.5V
- Output Current into Outputs (LOW)..... 20 mA
- Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)
- Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature (T _A) ^[4]	V _{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%
Automotive	-40°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62256-55			CY62256-70			Unit	
			Min.	Typ. ^[2]	Max.	Min.	Typ. ^[2]	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -1.0 mA	2.4			2.4			V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 2.1 mA			0.4			0.4	V	
V _{IH}	Input HIGH Voltage		2.2		V _{CC} + 0.5V	2.2		V _{CC} + 0.5V	V	
V _{IL}	Input LOW Voltage		-0.5		0.8	-0.5		0.8	V	
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-0.5		+0.5	-0.5		+0.5	μA	
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-0.5		+0.5	-0.5		+0.5	μA	
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = 5.0V, I _{OUT} = 0 mA, f = f _{Max} = 10 MHz		25	50		25	50	mA	
I _{SB1}	Automatic CE Power-down Current—TTL Inputs	V _{CC} = 5.5V, CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{Max}		0.4	0.6		0.4	0.6	mA	
I _{SB2}	Automatic CE Power-down Current—CMOS Inputs	V _{CC} = 5.5V, CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		2	50		2	50	μA	
				LL - Com'l	0.1	5		0.1	5	
				LL - Ind'l	0.1	10		0.1	10	
				LL - Auto	0.1	15				

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Capacitance^[5]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC(typ.)}	6	pF
C _{OUT}	Output Capacitance		8	pF

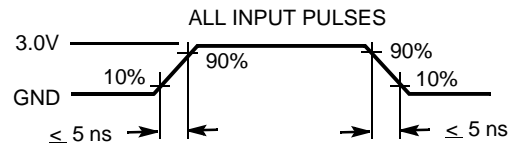
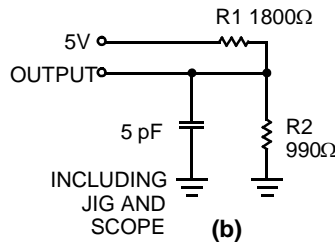
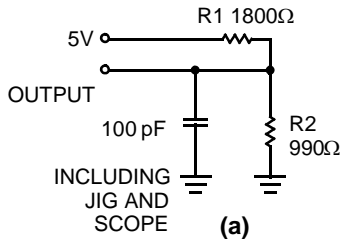
Thermal Resistance^[5]

Parameter	Description	Test Conditions	DIP	SOIC	TSOP	RTSOP	Unit
Θ _{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 4.25 x 1.125 inch, 2-layer printed circuit board	75.61	76.56	93.89	93.89	°C/W
Θ _{JC}	Thermal Resistance (Junction to Case)		43.12	36.07	24.64	24.64	°C/W

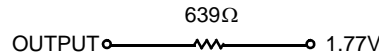
Notes:

3. V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
4. T_A is the "Instant-On" case temperature.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT

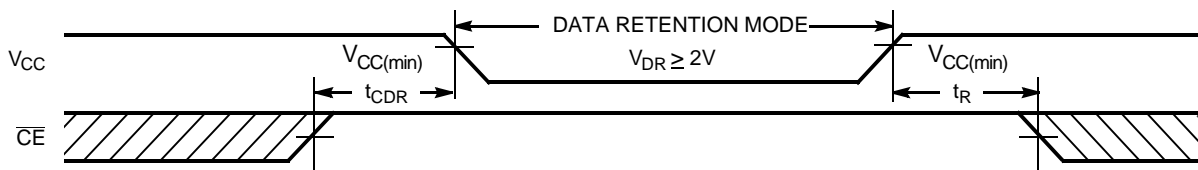


Data Retention Characteristics

Parameter	Description	Conditions ^[6]	Min.	Typ. ^[2]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		2.0			V
I _{CCDR}	Data Retention Current	L	V _{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V	2	50	μA
		LL - Com'l		0.1	5	μA
		LL - Ind'l		0.1	10	μA
		LL - Auto		0.1	10	μA
t _{DR} ^[5]	Chip Deselect to Data Retention Time		0			ns
t _R ^[5]	Operation Recovery Time		t _{RC}			ns

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Data Retention Waveform



Note:

6. No input may exceed V_{CC} + 0.5V.

