5 Port 10/100 Hardware NAT/NAPT Router

Features

Ethernet Switch

- Built in 6 MAC and 5 PHY
- Support 10Base-T and 100Base-T on LAN ports
- Support 10Base-T, 100Base-TX and 100Base-FX on WAN port
- Up to 2K MAC addresses
- Broadcast storm protection
- Auto MDI-MDIX
- Layer2-4 Multi-Field classifier
  - ◆ Support 8-MultiField entry
  - ◆ Support traffic policy
  - ◆ Support Multi-Filed filter
  - ◆ Support copy to mirror port
  - ◆ Support trap to CPU port
- Class of Service
  - ◆ Port based, MAC address, 802.1p, IPv4 ToS, IPv6 DSCP,TCP/UDP logical port and Multi-Field
  - ◆ Support 4-level priority queues per port
  - ◆ WRR/WFQ/SP
- Support hardware IGMP v1,v2 snooping
- Support Port mirroring
- Support 16 VLAN (IEEE Std 802.1q)
  - ◆ Port-based/tagged-based VLAN
  - ◆ Shared VLAN Learning/Independent VLAN Learning (SVL/IVL)
- Support insert, remove tag
- Support VLAN priority remarking
- Support STP, RSTP and MSTP
- Support port-based access control
- Support bandwidth control
  - ◆ In/Out port bandwidth control
  - ◆ Traffic Policy
  - ◆ WFQ
- Support double tag header
- Provide per port LED

32-bit CPU and Peripheral

- Provide 16-bit SDRAM (up to 32MB) with selectable clock speed.
- Optional serial/parallel bus Flash memory (up to 16MB)
- 1 simplified UART
- 15 multi-function pins
- 1 interrupt input pin
- 2 general purpose timers and 1 watchdog timer
- Selectable CPU clock rates: 125, 150, 175 MHz
- 4K I-Cache, 4K D-Cache, 8K I-MEM, and 4K D-MEM

Routing Engine

- Support IPoE, PPPoE, TCP/UDP, GRE/PPTP, UDP/L2TP auto-routing
- Hardware based layer 3/layer 4 NAT/NAPT routing to offload CPU computing power
- Support virtual server to maximize the network throughput
- 4K entries for routing table
- Support Application Level Gateway (ALG) tables

Package

- 128 pin LQFP

General Description

Integrating CPU, 5-port Ethernet switch and packet buffer, IP3210A provides the most cost-effect solution for IP sharing router. Among these Ethernet ports, four ports are used as LAN ports and one as WAN port. There are six MACs and the associated layer 3, 4 router and layer 2 switch engines in the SoC.

Supporting layer 2, layer 3 and layer 4 traffic classification, the switch engine can meet triple play applications. Hardware based IGMP snooping can support the real-time multimedia application without the intervention of CPU. The switch engine provides rich functions to meet the requirement of future applications.

The build-in hardware layer 3, 4 NAT/NAPT engine effectively supports the WAN-to-LAN and LAN-to-WAN auto-routing for IPoE, PPPoE, TCP/UDP, GRE/PPTP and UDP/L2TP packets. The hardware based NAT/NAPT routing engine accelerates the packet routing performance by inspecting the packet header and forwarding either to the CPU or to a destination port. The protocol ID, MAC address, IP address and port number of an incoming packet is checked and auto-routing is executed accordingly. For packets with recognized packet types, the NAT/NAPT engine routes the packet directly to the destination port. For unrecognized packets, the engine redirects the packet to CPU for further process before being sent to the destination port. This architecture greatly offloads the CPU computing power, featuring a high throughput NAT/NAPT router.

The embedded high performance 32-bit RISC core can be programmed to operate at selectable clock frequencies at 125, 150 or 175 MHz. The 7-stage pipelined architecture, together with build-in 4K I-Cache, 4K D-Cache, 8K I-MEM, and 4K D-MEM, increase the RISC instruction execution efficiency. With the aid of MMU, IP3210A can greatly reduce the memory management task for some OS. Two general-purpose timers and one watchdog timer are provided for programmer's convenience. Convenient firmware program debugging is also supported via the UART and JTAG interfaces.

External flash memory is used to store the firmware code for CPU and external SDRAM is used for both code execution and data storage. For greater flexibility of flash memory selection, both serial and parallel flash interface are supported and configurable through a pin strapping option. The industrial standard 16-pin interface is supported for the external SDRAM. The maximum capacity for flash memory and SDRAM are 16MB and 32MB, respectively. Effective DMA engines are designed to move incoming and outgoing packets directly between the MAC and SDRAM without the need of CPU involvement.

Revision History

Revision #	Change Description
IP3210A-DS-R00	Initial release

Disclaimer

This document probably contains the inaccurate data or typographic error. In order to keep this document correct, IC Plus reserves the right to change or improve the content of this document.

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1. Block Diagram

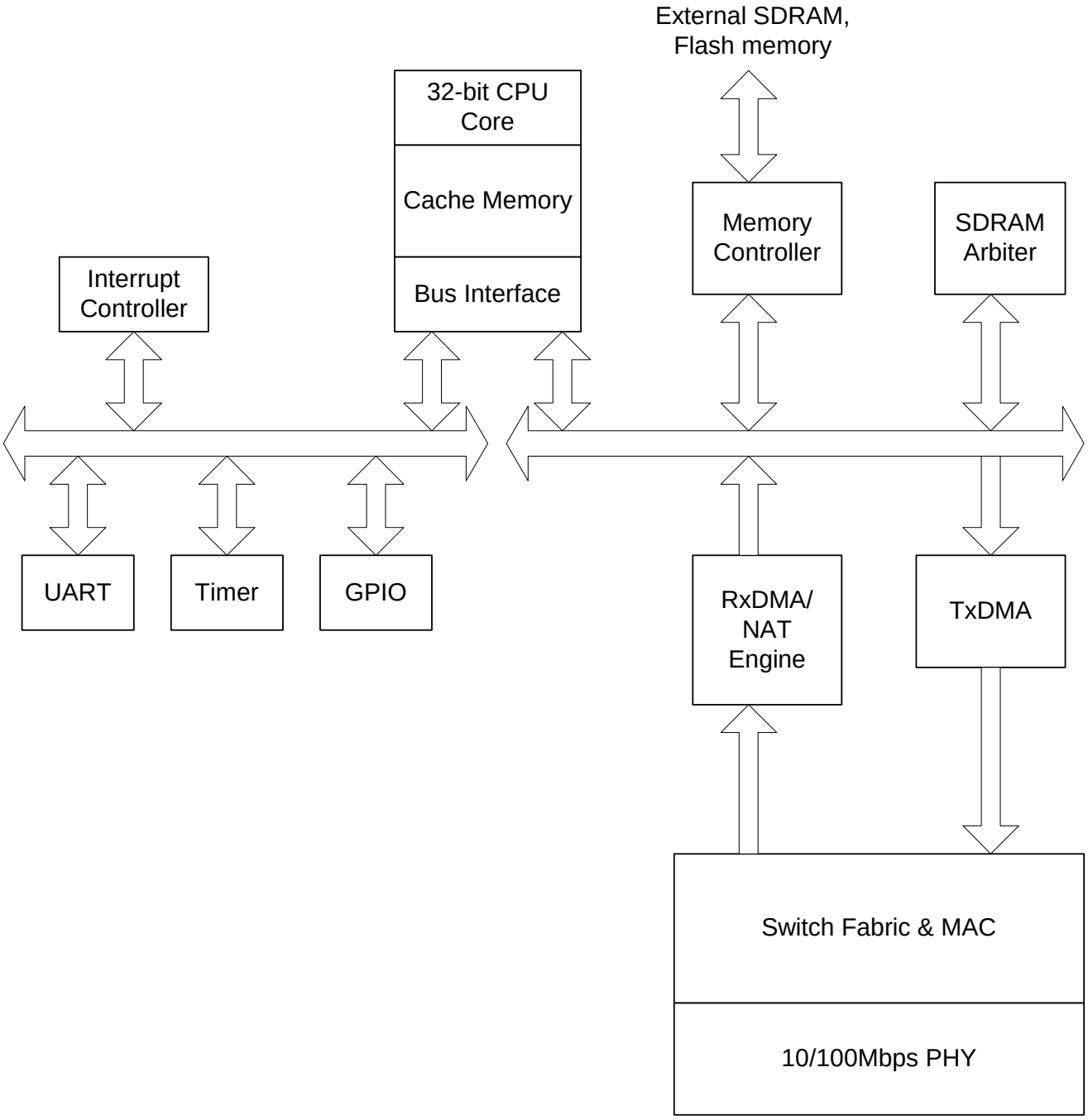
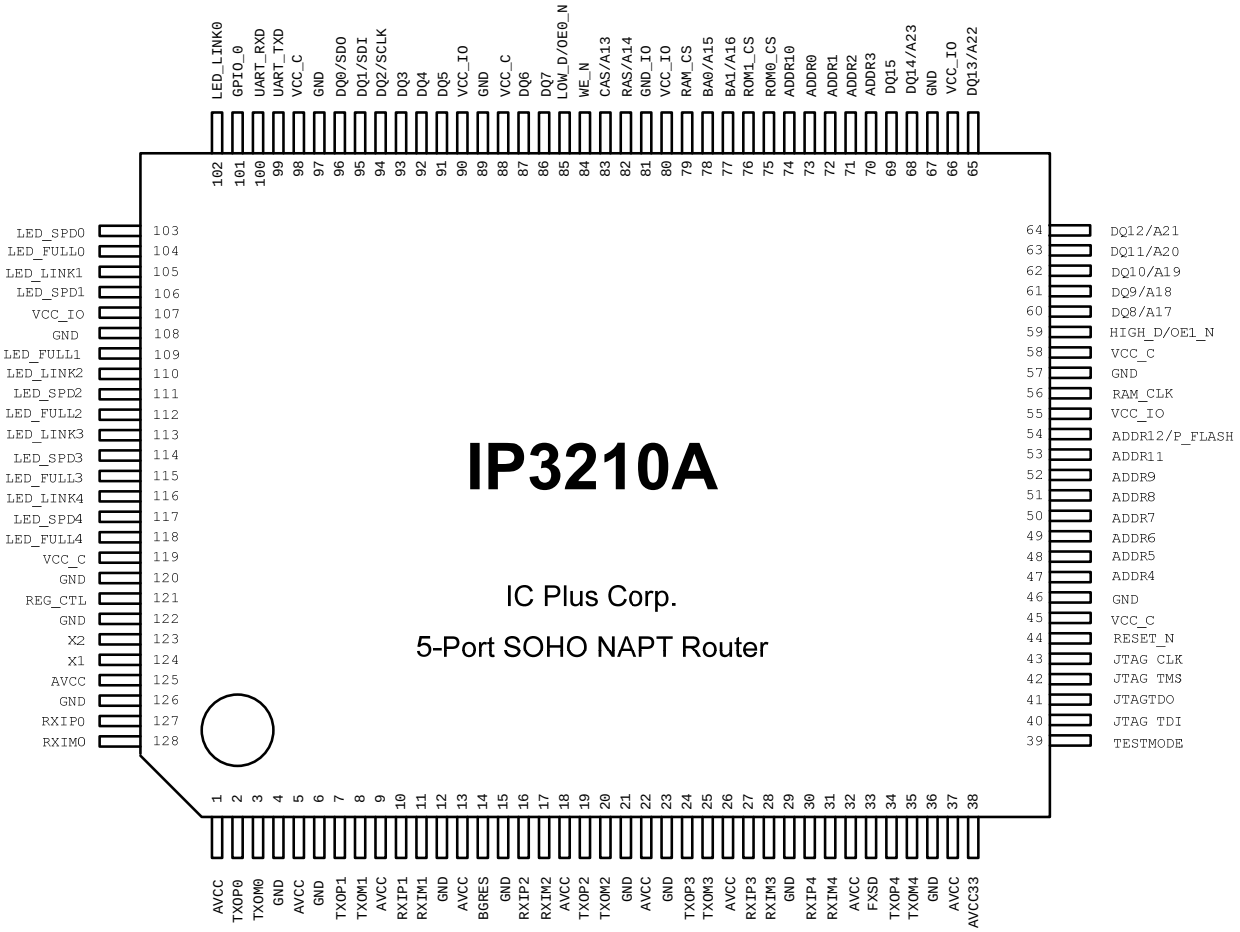


Figure 1 IP3210A 5-port 10/100 NAT/NAPT router block diagram

2. Pin Diagram



3. Pin Description

Type	Description
I	Input pin
O	Output pin
IPL	Input pin with internal pull low 140K ohm
IPH	Input pin with internal pull high 222K ohm

Type	Description
A	Analog pin
P	Power pin
G	Ground pin

Pin No.	Label	Type	Description
SDRAM Bus and Flash Memory Bus			
91~96, 87, 86	DQ0~DQ7	I/O	Shared data bus for Flash memory and SDRAM. During SDRAM access cycle, these pins function as data bus, DQ0~DQ7. During flash memory access cycle, these pins function as data bus, DQ0~DQ7. If serial flash memory is selected, DQ0~DQ2 are used as the following functions. DQ[2] : Serial Flash Clock output DQ[1] : Data output to Serial Flash memory. Connect this pin to DI of the serial flash memory. DQ[0] : Data input from Serial Flash memory. Connect this pin to DO of the serial flash memory.
60~65, 68, 69	DQ8/A17~DQ14/A23, DQ15/ A-1	I/O	During SDRAM access cycle, these pins function as data bus, DQ15~DQ8. During flash memory access cycle, these pins function as address bus. A-1 is the LSB of the parallel flash memory address bus.
47~53	ADDR4 ~ ADDR11	O	Address bus for SDRAM and parallel Flash memory.
54	ADDR12//P_FLASH	I/O	IP3210A will latch the state of this pin upon reset. “1”: Parallel bus flash memory. “0”: Serial bus flash memory. This pin is used as address A12 for SDRAM or flash memory.
59	HIGH_D/OE1_N	O	DQ15~DQ8 enable for SDRAM during the SDRAM access cycle. Byte output enable during Flash memory access cycle.
85	Low_D/OE0_N	O	DQ7~DQ0 enable for SDRAM during the SDRAM access cycle. Byte output enable during Flash memory access cycle.
82	RAS/A14	O	RAS for SDRAM access cycle. A14 address for Flash memory cycle.
83	CAS/A13	O	CAS for SDRAM access cycle. A13 address for Flash memory cycle.
56	RAM_CLK	O	Clock for SD RAM access cycle.
75, 76	ROM0_CS, ROM1_CS	O	Chip selection for flash memory 0 and flash memory 1.
78, 77	BA0/A15, BA1/A16	O	During SDRAM access cycle, it functions as the bank selection. During flash memory access cycle, it functions as the memory address bus.
79	RAM_CS	O	Active low output. SDRAM chip selection.
84	WE_N	O	Active low output. Write enable for SDRAM or parallel flash memory.

Pin description (continued)

Pin No.	Label	Type	Description
LED pin			
102~104, 103~118	LED0_LINK0~LED_SPD1, LED_FULL1~LED_FULL4	O	Active low LED driving pins. LINK/ACT: Active when the cable is linked up or TX , RX ongoing. SPD: Active when the cable is linked at 100MBps speed. FULL: Active when the cable is operating in full duplex mode.
MDI			
2,3,7,8, 19,20, 24, 25, 34, 35	TXOP0,TXOM0 TXOP1,TXOM1 TXOP2,TXOM2 TXOP3,TXOM3 TXOP4,TXOM4	I/O	These pins are directly connected to the TX pair of the transformer. TXOP0 and TXOM0 represent the positive polarity of port 0 and negative polarity of port 0 respectively. TXOP4 and TXOM4 are connected port 4. TXOP4 and TXOM4 are also configured as the Fiber SerDes output, please refer to the paragraph “DC Characteristics” for more detail information.
127, 128, 10, 11, 16, 17, 27, 28, 30, 31	RXIP0, RXIM0 RXIP1, RXIM1 RXIP2, RXIM2 RXIP3, RXIM3 RXIP4, RXIM4	I/O	These pins are directly connected to the RX pair of the transformer. RXOP0 and RXOM0 represent the positive polarity of port 0 and negative polarity of port 0 respectively. RXOP4 and RXOM4 are connected to port 4. RXOP4 and RXOM4 are also configured as the Fiber SerDes input, please refer to the paragraph “DC Characteristics” for more detail information.
Power Supply			
1, 5, 13, 18, 22, 26, 32, 9, 125, 37	AVCC	P	Analog circuit power supply. These pins should be connected to 1.95V power source.
38	VCC33	P	Analog 3.3V power source. This pin should be separated with the IO power source with a ferrite bead.
45, 58, 88,119, 98	VCC_C	P	Digital core power supply. These pins should be connected to 1.95V power source.
55, 66, 80, 90 ,107	VCC_IO	P	I/O signal power supply. These pins should be connected to 3.3V power source.
4, 6, 12, 15, 21, 23, 29, 36, 46, 57, 67, 89, 97, 120, 122, 126, 108, 81	GND	G	These pins should be connected to ground plane.

Pin description (continued)

Pin No.	Label	Type	Description
Miscellaneous Pins			
14	BGRES	A	This pin sets the band gap reference voltage for the internal circuit. Should be connected to GND through a 6.19K ohm resistor.
39	TEST MODE	I, IPL	This pin sets the testing mode upon reset. Leave it unconnected during the normal operation. TEST_MODE = 0: Normal operation mode; TEST_MODE = 1: Test mode;
40 ~ 43	JTAGTDI/GPIO16 JTAGTDO/GPIO13,JTAGTMS/GPIO15,JTAGCLK/GPIO14	I/O	During test mode, these pins are used for JTAG test. During normal operation mode, these pins are used as GPIO.
44	RESET_N	I	Low active reset input.
99	UART_TX/GPIO17	O	UART TX signal or GPIO 17
100	UART_RX/GPIO18	I	UART RX Signal or GPIO 18
101	GPIO0/INT	I/O	General purpose I/O signal or level sensitive Interrupt input
121	REG_CTL	A	This pin controls the base of a PNP transistor. The collector of the PNP transistor is 1.95V which is supplied to the power source of VCC_C.
124	X1	I	Connected to the 25MHz clock or crystal input
123	X2	O	Connected to the other side of 25MHz crystal.
33	FXSD	I	Tie this pin to GND when port 4 is connected to TP cable Please refer to the paragraph “DC Characteristics” for more detail information.

4. Functional Description

4.1 Ethernet Switch Engine

4.1.1 Switch Register

All the PHY and Switch registers are accessible in IP3210A through the “SMI for switch configuration” register (0x AF003000). To read/write these PHY/Switch registers, the firmware on IP3210A should write the PHY/Switch ID, register location and read/write command to the proper bit fields in SMI control register and trigger bit31 with an ‘1’. Table 4-1 shows the PHY/Switch register location defined for the Ethernet Switch Engine.

Table 4-1 PHY/Switch register location for Ethernet Switch Engine

PHY part		Switch part	
PHY ID	00 ~04	Switch ID	20 ~ 26
Register Address	0 ~ 06	Register Address	0 ~ 31

4.1.2 Flow Control

IP3210A supports two flow control mechanism configurable by firmware. For the fast path receiving, the firmware can program the hardware to turn on flow control function if the number of available RX packet buffers is less than a pre-specified threshold and to turn off flow control function if the number of available RX packet buffers is greater than a pre-specified threshold. The threshold values for tuning off/on low control are programmed through the FL_OFF_TH field and the FL_ON_TH field of FLOWCNTRL1 (0xAF003050) register. Alternatively, the firmware can manually turn on the flow control function by writing ‘1’ to the FLM_ON field of FLOWCNTRL2 (0xAF003054) register and turn off the flow control function by writing ‘1’ to the FLM_OFF field of FLOWCNTRL2 (0xAF003054) register. This manual control mechanism is enabled by setting ‘1’ to the FL_Manual field of FLOWCNTRL2 (0xAF003054) register.

4.1.3 Quality of Service (QoS)

IP3210A utilizes a combination of traffic policy, priority classification and output queue scheduling to achieve policy-based QoS to meet the requirement of internet services, such as file transfer, email, video, voice and Web. Traffic policy can aggregate traffic flow and police against its traffic profile. This mechanism can effectively manipulate the traffics entering the switch. Finally, packets will be placed into appropriate output queue based on priority classification.

4.1.4 Traffic Policy

IP3210A traffic policy is maintained by the combination of classifier, meter and dropper. The classifier separates received packets into different traffic streams based on the pre-defined condition. IP3210A provides 8 Multi-Field entries, where each entry is a combination of one or more layer 2-4 headers. Multi-Field classification can classify packets into traffic classes and traffic flows. For instance, an end-to-end flow is recognized by using five tuples. Each Multi-Field contains a meter for measuring the traffic. The meter passes the in-profile packets for forwarding and put out-of-profile packets into dropper for dropping. The designer can configure the parameters of traffic policy from MII register 26.0-23.

Each entry associated with Multi-Field counter is used to monitor the traffic rate. The counter value is represented in byte unit. The CPU can monitor the traffic rate to periodically read the value of multi-field counter through MII register.

4.1.5 Priority Classification

The priority classification is used to separate packets into four priority levels. In IP3210A, packet classification can categorize packets based on port-based classification and packet-based classification. Port-based classification, packets coming from the same port have a fixed priority level. Packet-based classification is based on one header filed or a combination of more header fields. Packet-based classification has a flexible packet classification to

classify priority level designated by the following header fields:

- Special tag
- Source MAC address
- Destination MAC address
- VID
- VLAN priority
- IPv4 ToS/IPv6 DSCP
- TCP/UDP logical port
- Layer 2-4 Multi-Field

Figure 2 illustrates the priority classification flow chart.

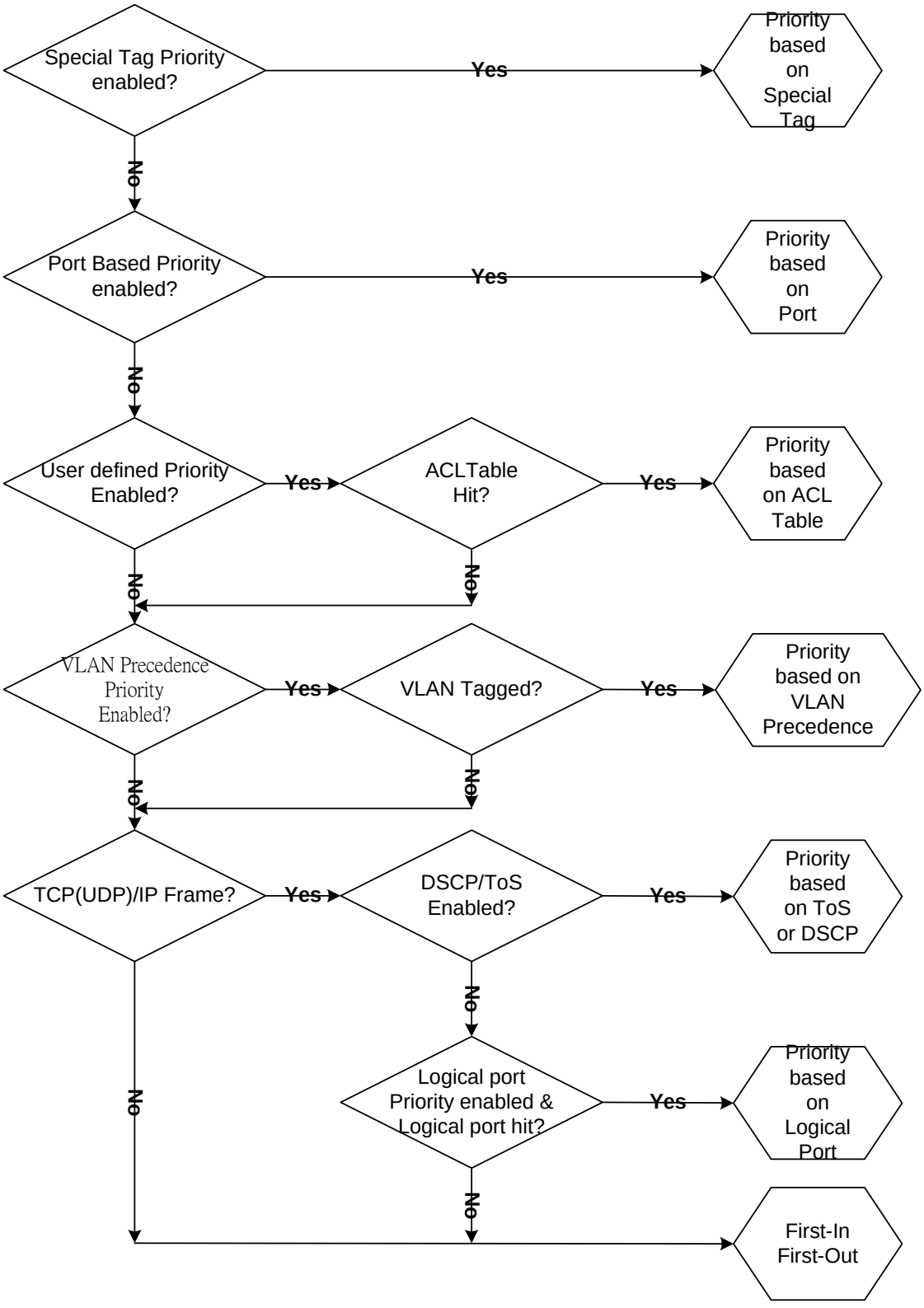


Figure 2 IP3210A Traffic Classification Rule

4.1.6 Output Queue Scheduling

IP3210A supports four scheduling modes at Table 4-2.

Table 4-2 Four Scheduling Modes

Mode #	Q3	Q2	Q1	Q0
Mode 0	WRR	WRR	WRR	WRR
Mode 1	WFQ	WFQ	WFQ	WFQ(BE)
Mode 2	SP	WFQ	WFQ	BE
Mode 3	SP	SP	SP	SP

SP: Strictly Priority; WRR: Weight Round Robin; WFQ: Weight Fair Queuing; BE: Best Effort

SP:
In strict priority mode, the packets stored in the highest priority queue will be sent until it is empty. The second highest priority queue is then activated with all its packets being sent. This procedure repeats with packets in queues with descending order until packets in the lowest priority queue are sent.

WRR:
The designer can control the number of packets transmitted on an output queue by setting its weight.

WFQ:
The designer can allocate a bandwidth on an output queue by setting its rate. Configuring WFQ bandwidth can be through the internal register.

4.1.7 IGMP Snooping

IP3210A supports IGMP v1 and v2 snooping specified in RFC 1112 and RFC 2236 respectively. Because IGMP is used between hosts and neighboring multicast routers, IP3210A listens to the IGMP message communication between router and host to establish multicast group membership. Based on the group membership information, IP3210A forwards IP multicast data to its members which are registered in the group table. This mechanism is referred to as the “hardware based IGMP snooping”. The timeout mechanism is necessary, so that the host can silently leave a specific multicast group. “Silently Leave” means that a host does not respond to the query message when it intends to leave a multicast group. In addition to the hardware based IGMP snooping, IP3210A also supports pure firmware based IGMP snooping and IGMP snooping with CPU assistance mode. The firmware based IGMP snooping implies that the firmware must handle IP multicast traffic which includes multicast data packets and IP multicast control packets. In the firmware based IGMP snooping mode, the multicast control packet is used to maintain the multicast table and then the multicast data packet is forwarded to the destination ports according to this table. In IGMP snooping with CPU assistance mode, the IP data packet is forwarded by the internal switch engine and the multicast membership table is maintained by CPU. In hardware based IGMP snooping, all multicast packets are handled by the hardware without the intervention of CPU once the IGMP function is enabled.

IP3210A supports not only IGMP snooping but also MLD snooping. The difference between these two mechanisms is that there is no option for hardware based MLD snooping. It only supports firmware MLD snooping mode and MLD snooping with CPU assistance. For MLD snooping with CPU assistance, IP3210A traps MLD control packets to CPU for further building multicast table and the multicast data packet is forwarded based on this table. For firmware MLD snooping, IP3210A traps all IPv6 multicast packet to CPU and CPU should process these packets and forward to the proper ports.

4.1.8 Security Filtering

IP3210A provides flexible security configuration to protect against attacks and filter suspicious traffics. These packets can be dropped or forwarded to CPU for further process. IP3210A provides packet filtering based on physical port, MAC address, logical port and layer 2-4 Multi-Field packet headers.

4.1.9 Physical Port Filtering

The forwarding and learning ability of a port can be disabled respectively. The security rule is that any user shall be authenticated by an authenticating server or the administrator when accessing to the network. Administrator (or CPU) can disable forwarding and learning ability on a given port, if a host is in the unauthorized state.

4.1.10 MAC Address Filtering

The feature of MAC address filtering can be configured in two modes: The negative list mode and positive list mode. The negative list mode allows IP3210A to drop packets based on the list of either specific source MAC address or specific destination MAC address. The negative list mode can also drop packet on per VLAN group base. Configuring contexts of the negative list MAC address is through "Address Table Access Register". The positive list mode only accepts those packets registered in SMAC (source MAC address) table.

4.1.11 Logical Port Filtering

IP3210A can discard packets based on the layer 4 logical port. The logical port can define a particular port number or a range of port numbers. If the source's logical port or the destination's logical port in the incoming packet matches any of the pre-defined logical ports, the incoming packet will be discarded.

4.1.12 Layer 2-4 Multi-Field Filtering

In addition to supporting simple layer 2 to layer 4 filtering rule, IP3210A can also filter packets based on a combination of layer 2-4 Multi-Field packet headers.

4.1.13 Spanning Tree

The spanning tree protocol can be implemented through the cooperation of both firmware and hardware. In software implementation, CPU must process BPDU packet and configure each port. In hardware implementation, the switch traps BPDU to CPU and either forwards or drops packet according to the register settings. The Table 4-2 describes how to configure the state of each port in IP3210A.

Table 4-2 BPDU packet state

State	Fwd BPDU packet to CPU	Fwd BPDU packet to each port	Address learning	Fwd all packets normally	Forwarding, Learning[1]
Disable	X (note 2)	X (note 2)	X	X	X, X
Blocking	O	X (note 3)	X	X	X, X
Listening	O	O	X	X	X, X
Learning	O	O	O	X	X, O
Forwarding	O	O	O	O	O, O

Note1: O: enabled, X: disabled
Note2: CPU should not send packets to the switch and should discard packets coming from the switch.
Note3: CPU should not send packets to the switch.

IP3210A supports fast aging function for RSTP by programming registers 20.14[6:5] and 20.14[4:0]. The designer can configure the parameters from MII register.

4.1.14 Special Tag

The purposes of special tag are:

- To allow a packet coming from the switch to carry the ingress port number and violation event before it is sent to the CPU.
- To allow a packet sent from CPU to indicate the egress port and output queue number in special tag header.

The special tag is inserted right behind the Source MAC Address. Unlike the type ID of 802.1Q represented by 8100 in hexadecimal, the special tag is represented by 81xx in hexadecimal, where “xx” means a number other than “00”.

Source MAC Address	Destinat MAC Address	81xx	Tag Information	Payload	CRC

Special tag format

There are two formats of special tag, depending on the frame direction. The special tag format is defined as follows:

Special Tag added to the received packet (From switch side to CPU side)

The special tag information consists of ingress port number and violation event. Ingress port number indicates where the packet comes from. The violation event is an event vector consisting of security violation, VLAN violation and miss address table.

Security violation: IP3210A supports unknown SMAC filtering and the designer can enable it by register setting. Unknown SMAC means source MAC address of the received packet that is not found in the pre-defined address table. When this function is enabled, the received frames with unknown SMAC are marked as “illegal SMAC” and will not be forwarded to the destination. Instead, this packet is forwarded to the CPU so that the CPU can take the following action:

(a) VLAN violation: If a VLAN ID is found, this bit is set.

(b) Miss address table: If the searching result of the address table misses, this bit is set.

Special Tag Information	Description
Bit 7-3	Packet Information - bit 4: Reserved - bit 3: Reserved - bit 2: Miss address table - bit 1: Security violation - bit 0: VLAN violation
Bit 2-0	Ingress Port number - 3’b000: Disabled - 3’b001: Port 0 - 3’b010: Port 1 - 3’b011: Port 2 - 3’b100: Port 3 - 3’b101: Port 4 - Other: Reserved

Special Tag added to Transmitted Packet (From CPU side to switch side)

This function provides for forwarding decision, priority assignment and disabling physical port. The parameters embedded in the special tag header can be set by CPU.

Special Tagged Information	Description
Bit 7	0: Enable MAC address learning 1: Disable MAC address learning
Bit 6-5	Priority Assignment - 2'b00: Disabled - 2'b01: Queue 1 - 2'b10: Queue 2 - 2'b11: Queue 3
Bit 4-0	Output Port Mask. 1: Forward to this port. 0: Do not forward to this port. - bit 4: port 4 - bit 3: port 3 - bit 2: port 2 - bit 1: port 1 - bit 0: port 0

4.2 Router Engine

4.2.1 HNAPT Architecture

Figure 3 illustrates the fast and slow packet routing paths for a packet incoming from the WLAN port and outgoing to a LAN port. For the fast path, the switch engine forwards the packet to the NATP engine for Layer 3, 4 header parsing. The HNATP engine recognizes the packet and replaces the proper fields in Layer 3, 4 by routing table look-up. The resulting packet is then sent to the destination LAN port directly. For the slow path, the HNATP engine does not recognize the packet or the routing table does not contain proper substitution information. The packet is forwarded to the CPU for further process. The firmware running at CPU checks the incoming packet and performs proper routing substitution on the packet before directing it to the destination LAN port. The firmware may also extract proper fields from the packet to construct routing table entry so that the subsequent packets from the same source will become recognizable by the HNAPT engine and be forwarded to the destination LAN port directly through fast path. Similar routing procedures are performed for packets incoming from a LAN port and outgoing to the WLAN port. By default, the packet types that are currently supported by HNAPT engine include IPoE, PPPoE, TCP/UDP, GRE/PPTP, and UDP/L2TP. The firmware can disable the support of any of these protocols by programming the corresponding bit field in PROTOCOL Register (0xAF003080)

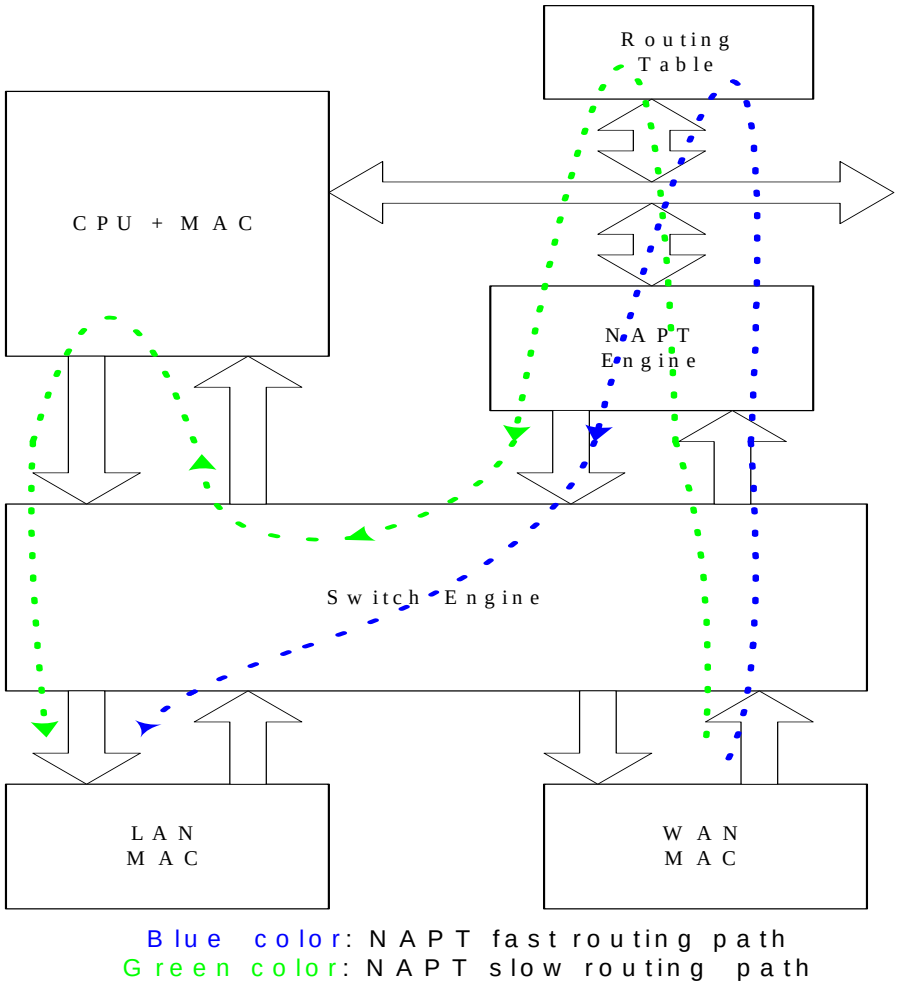


Figure 3 Fast and slow path packet routing illustration

For some special applications, it may be desirable to process all incoming packets by firmware even when the

HNAPT engine can recognize the packets. There are two special modes built in IP3210A that can be used to disable the HNAPT function completely or to direct the HNAPT processed packets to CPU instead of the destination port. The HNAPT function can be disabled by setting Nat_en field of ROUTERCNTRL (0xAF003004) register to 0, and all packets processed by HHNAPT can be directed to CPU by setting the AllToCpu field of ROUTERCNTRL to 1.

The firmware support for HNAPT is provided by a set of API modules to facilitate the programming effort when the HNAPT function is turned on. Detailed descriptions of these API modules and the programming of the HNAPT function is given in Application Notes for HNAPT firmware programming guide.

4.2.2 MAC Addresses and VLAN ID

IP3210A supports two 48-bit router source MAC addresses programmable through SA0ADDRL/ SA0ADDRH (0xAF00303C, 0xAF003040) and SA1ADDRL/ SA1ADDRH (0xAF003044, 0xAF003048) registers, respectively. Up to eight VLAN IDs can also be programmed through VLANID01, VLANID23, VLANID45, VLANID67 registers (0xAF00301C, 0xAF003020, 0xAF003024, and 0xAF003028). Each VLAN ID is 4-byte and is automatically inserted to packets between a selected pair of WAN and LAN ports with either inbound (WAN-to-LAN) or outbound (LAN-to-WAN) direction as indicated by one bit field (InBoundx) in the corresponding VLAN ID register.

4.2.3 RX/TX Queue Buffer Management

The RX and TX buffer management is accomplished by link lists established by the firmware. Buffer descriptor scheme with distinguished ownership bit for firmware and HNAPT/DMA engine is used to ensure non-conflicting access by them. For a RX or TX queue, the associated buffer descriptors are tabulated in consecutive memory locations. Registers RXSWDSCBASEADDR (0xA3003008), TXSWDSCBASEADDR (0xA3003064) and HWDSCBASEADDR (0xA300300C) are used to identify the base addresses of the tabulated descriptors for the slow path RX queue, slow path TX queue and fast path RX queue, respectively. Note that since RX packets in the fast path are directly forwarded to the destination port, there is no need to define TX queue for the fast path. At initialization, the firmware on IP3210A allocates proper memory segments for these descriptor tables and fills the three base address registers with the corresponding memory addresses.

The packet buffers for the various RX and TX queues are also allocated and linked by the firmware. At initialization, the firmware allocates a fixed number of available packet buffers and link them into a buffer queue with the first buffer address specified in FIRSTBUFBASEADDR (0xA3003010) and the last buffer address in LASTBUFBASEADDR (0xA30030D4) registers, respectively. This buffer queue is frequently updated during the normal packet receiving and transmitting operations. When a buffer is needed by RXDMA engine for storing an incoming packet, the first buffer in the queue is easily fetched as its address is readily given by FIRSTBUFBASEADDR register and, after the fetching, the RXDMA engine automatically maintains the integrity of the buffer queue by overwriting the FIRSTBUFBASEADDR register with the address of the second buffer in the queue. On the other hand, when a new buffer is allocated for the buffer queue by the firmware or when an existing buffer of a transmitted packet is ready for releasing back to the buffer queue by the TXMDA engine, this unused buffer is inserted into the queue by linking its address to the last buffer in the queue and overwriting the LASTBUFBASEADDR register with its address.

The total number of buffers allocated for the fast path RX queue is programmed by the firmware in the TotalBuffer field of FLOWCNTRL1 (0xA3003050) register. Since the packet buffers in both slow and fast path RX queues are fetched from the same buffer queue, the TotalBuffer field of FLOWCNTRL1 (0xA3003050) register must be specified with a value less than the number of buffers allocated for the buffer queue at initialization.

For power saving, the hardware ceases checking the ownership bit of the TX descriptors once the slow path TX queue becomes empty. As a result, the firmware has to program the TxSW_Trig field of SWPKTTRIG (0xA30030C0) register to 1 to trigger the hardware to start the transmission loop again if it en-queues new transmit packets into the TX queue under empty status. It is also possible to encounter the condition that all RX descriptors

for the slow path RX queue are occupied. The hardware ceases the checking on available RX descriptors to save power and the firmware has to trigger the hardware to start RX descriptor fetching for RX queue by writing the HasSWDsc field of RXDMACNTRL (0xA300304C) register to 1 when it allocates new RX descriptors for the RX queue.

To assist firmware in processing RX packets efficiently, the RX packets with recognized protocols can be placed in packet buffers such that the starting point of the L3 portion of a RX packet occurs at a fixed offset from the beginning of the packet buffer. This fixed offset is programmable by the firmware through the IPFixPos field of RXDMACFG (0xA3003014) register with a value no greater than 100. The firmware shall not set this offset value smaller than the total expected L2 length to avoid insufficient space to store the L2 portion of the packet in the buffer.

4.2.4 MAC Addresses and VLAN ID

IP3210A supports two 48-bit router source MAC addresses programmable through SA0ADDRL/SA0ADDRH (0xA300303C, 0xA3003040) and SA1ADDRL/SA1ADDRH (0xA3003044, 0xA3003048) registers, respectively. Up to eight VLAN IDs can also be programmed through VLANID01, VLANID23, VLANID45 and VLANID67 registers (0xA300301C, 0xA3003020, 0xA3003024, 0xA3003028). Each VLAN ID is 4-byte in length and is automatically inserted to packets between a selected pair of WAN and LAN ports with either inbound (WAN-to-LAN) or outbound (LAN-to-WAN) direction as indicated by one bit field (InBoundx) in the corresponding VLAN ID register.

4.2.5 Statistical Counters

The SWITCHRXCOUNTER (0xAF003210) register counts the number of packets received by the HNAPT engine from the switch engine. The RXPKTCOUNTER (0xAF003200) register consists of two counters, one for the total number of packets being received by HNAPT engine and the other for the number of packets forwarded to CPU. The TXPKTCOUNTER (0xAF003204) register also consists of two counters, one for the number of packets transmitted from the slow path TX queue and the other for the number of packets directly sent from the RX queue of the HNAPT engine. Each of these statistical counter is 16-bit and the counter wraps around to zero when overflow.

4.2.6 CPU and Peripheral Interface

IP3210A incorporates a 32-bit RISC CPU with DMA control and supports peripherals including UART, timers, interrupts, JTAG, serial/parallel flash memory and SDRAM. Register control is provided to configure the CPU speed and the features of these supported peripherals. The description of the CPU and the peripheral interfaces are given in the following.

4.2.7 CPU Core

The CPU core is a high-performance RISC with 7-stage pipeline architecture and 4 internal cache memory types (I-Cache, D-Cache, I-RAM, D-RAM). The CPU supports native big endian mode. To enhance the CPU performance, the CPU contains a Branch Target Buffer to reduce the instruction branch penalty. Incorporating write-back or write through cache controller, the CPU can drive the execution efficiency to an extreme state. A compromise between the power consumption and the system performance can be achieved by setting the CPU clock. IP3210A provides various speeds at 125, 150 and 175 MHz for system optimization and can be easily programmed by selecting the desired setting for the CPU SPEED register (0xAF005018). For high speed arithmetic computation, a multiply-and-accumulator unit that can achieve a 1-cycle 16x16 or 2-cycle 32x32 multiply and accumulate operation is built in with the CPU core. The CPU also has a memory management unit (MMU), providing a 4-Kbyte-page size and 16-entry joint translation look-aside buffer (TLB). Convenient firmware debugging is supported through the JTAG and UART interfaces.

4.2.8 UART

The UART has an external interface through two pin-outs, UART_TXD and UART_RXD, for transmit serial bit out and receive serial bit in, respectively. When the UART function is not turned on, both of these two pins can be used as GPIO pins where the UART_TXD pin is designated as GPIO[17] and UART_RXD as GPIO[18].

The UART can be configured to support various baud rates, ranging from 2400bps to 119200bps by setting bit31-16 of the UART control/status (UCS) register (0xAF002004). An interrupt to CPU can be generated after a number of bytes being received at the UART interface by programming RxThreshold and RIE fields in the UCS register. On the other hand, when TIE bit is set to 1, an interrupt to CPU is generated whenever all available TX bytes in the hardware are transmitted out of the UART interface. The no-parity, even-parity and odd-parity data format is selectable by the Parity_en and Even_Odd fields in the UCS register. The 1 or 2 stop-bit mode can also be set by the Stop_bit field. The current RX byte parity is indicated in the Parity field. RX data error conditions are reported in the UCS register through the Parity_err and Framing_err fields. TX buffer empty and TX data ongoing are read-only status from the UCS register. An Internal loopback test mode for the UART transceiver is also supported by setting the loopback field of the UCS register.

With the UCS register properly set, the UART TX operations can be performed by writing bytewise data to bit31-24 of the UART buffer (UBF) register (0xAF002000) and the RX operations by reading bytewise data from bit31-24 of the UBF register. Note that a write to bit31-24 of UBF for TX byte operation will not corrupt any RX bytes that are ready for read since the read and write data ports are physically separated although they are only logically defined at the same bit fields of UBF. On-chip 16-byte RX and TX buffers are employed to ensure the read/write performance of the UART transceiver. The buffering operation is handled by hardware and is transparent to the control register interface. For each transmit burst, the TX buffer can be filled up to 16 bytes. To prevent TX overrun condition from occurring, the next transmit burst can only start after the TX empty status bit (bit2) of UCS is set to 1 for the current transmit burst. For receiving data bytes, the RX_STATUS bit (bit23) of UBF is set to 1 by hardware whenever there is an available RX byte ready for read back by firmware. The RX_STATUS bit is automatically cleared by the hardware if no more RX byte is available. The RX overrun condition will occur if the available RX byte is not read while more than 16 bytes of data have been received. This error condition is not reported in the register and may result in unknown RX data corruption behavior. Since the maximum baud rate of the UART is relatively slow, this RX overrun condition can be easily avoided by a well-designed firmware code.

4.2.9 Timers

There are two general-purpose timers (Timer1 and Timer2) and one watchdog timer (WDTimer) in IP3210A. The general-purpose timers are programmable and used to facilitate the need of time unit used for programming purposes. The watchdog timer is used to detected conditions that may result in CPU unexpectedly hanged in an unknown state. During normal operation, the watchdog timer is periodically set by the firmware running on CPU to keep it from expiring. When a catastrophic system breakdown happens that causes a CPU halt, the firmware code that updates the watchdog timer no longer functions correctly and consequently the watchdog timer does not get updated which eventually leads to timer expires that triggers a watchdog timer interrupt. This interrupt is hardwired to trigger a CPU reboot process to rescue the breakdown.

Each of the three timers is configurable through a set of 5 registers. The three sets of registers for Timer1, Timer2 and WDTimer are (TIM1L, TIM1H, Prescaler1, Timer1C, TIS1), (TIM2L, TIM2H, Prescaler2, Timer2C, TIS2) and (TIMWDL, TIMWDH, PrescalerWD, TimerWDC, TISWD), respectively. The time scale of the three timers is controlled by their respective set of TIMnL, TIMnH and Prescalern (n = 1, 2 or WD) registers and the time unit is given by the formula below:

Timern = SDRAM_CLK rate * Prescalern value * [TIMnH-TIMnL+1] value

Where SDRAM_CLK rate is the operating frequency of the SDRAM (can be selected as 125 or 150 MHz), Prescalen value is specified by 24-bit in Prescalen register and [TIMnH-TIMnL+1] is the difference between TIMnH and TIMnL registers when the timer starts.

Timern gets started by setting TimernGo bit in TimernC register to 1. To control the proper response when timer expires, IME_Timerx bit is set to 1 to generate timer interrupt and TxAIM is set to 1 if automatic restart of the timer is desired or set to 0 if the halt of the timer is desired. The timer interrupt status is indicated by intr_timern in TISn register and is clear when it is written by a '1'. In contract to Timer1 and Timer2, TimerWD has one additional control bit, WDMode, in TISWD register. When this WDMode is programmed to 0, the watchdog timer acts as a regular timer in that it does not trigger a CPU/System reset when the timer expires. When WDMode is set to 1, the watchdog function is turned on to trigger a CPU/System reset when the timer expires.

4.2.10 Interrupt

The interrupt controller supports a number of hardware interrupt sources that are configurable through the setting of STMSK (0xAF004000), CPOL (0xAF004004), IntS1 (0xAF004008) and IntS2 (0xAF00400C) registers. The selection of interrupt sources is programmable by setting IntS1 and IntS2 with a total of up to 14 sources where Source 15 to Source 8 are specified by IntS1 and Source 7 to Source 2 by bit31-8 in IntS2. Each source field in IntS1 and IntS2 should be filled with a 4-bit number that identifies the corresponding selected source. For the router/switch application in IP3210A, 7 hardware interrupt sources are provided with each of them associated with a source number as shown in Table 4-3.

Table 4-3 Hardware interrupts source number assignment

Hardware Interrupt Source	Interrupt Source Number
Timer 1	15
Timer 2	14
Router (NAPT Engine)	13
UART	9
Timer (WatchDog)	8
GPIO0	7
Switch Engine	6

The 7 interrupts consist of three timers, one UART, one GPIO, one router and one switch hardware interrupt sources, which can be programmed to generate interrupt events to CPU. The three timer interrupts are Timer1, Timer2 and WatchDog Timer; the UART interrupt is the UART TX/RX interrupt; the GPIO0 interrupt is the external interrupt driven by GPIO pin0; the router interrupt is the interrupt generated by NATP engine and the switch interrupt is the interrupt generated by the switch engine.

Each of these interrupts can be enabled by writing an "1" to the corresponding bit of Interrupt Mask fields in the STMSK register (0xAF00400). The interrupt event of each source is maintained in the interrupt status field of the CPOL register (0xAF004004). The polarity field of the CPOL register can also be set to indicate whether the corresponding source is a high-level sensitive or low-level sensitive interrupt. An additional "CAUSE" field in STMSK register is used to reflect the interrupt source instantaneous status that can be checked at any desirable time by polling the corresponding "CAUSE" field for this interrupt source. This can be useful when it is desired to clear the interrupt source status by firmware.

Once the interrupt sources are properly programmed in IntS1/IntS2 registers and the respective fields in STMSK and CPOL registers, the occurrence of an interrupt event will trigger the CPU to enter the interrupt service routine (ISR). The firmware is responsible to clear the corresponding interrupt status after the interrupt event is served. The priority of the interrupt source goes from high to low for source15 to source2 in IntS1 and IntS2. For interrupt source15 to source8, direct interrupt vector access functionality is

supported for the respective ISRs. When the direct interrupt vector access is utilized, the firmware is responsible to program the locations of these ISRs into a set of interrupt vectors on the CPU. More detailed ISR programming methodology and examples for IP3210A can be referred to Document???

4.2.11 Memory Interface

IP3210A supports one SDRAM controller and up to two generic static memory controllers. The required functional pins for these three memory interfaces are shared and managed by hardware in order to keep low pin count for IP3210A while minimizing the impact to firmware complexity.

With address lines A[0]-A[12], CAS_N, RAS_N, BA[0]-BA[1], the SDRAM controller can support an external SDRAM up to 32M bytes of range with memory mapping from 0x00000000 to 0x01FFFFFF. The external data bus for SDRAM is 16-bit wide given by DQ[0]-DQ[15]. The SDRAM_CLK is the clock output to SDRAM, which is 125 MHz when the CPU speed is 125 or 175 MHz and is 150 MHz when the CPU speed is 150 MHz. The chip select pin, SDRAM_CS_N, for SDRAM is used to assert the SDRAM device when the SRAM memory region is accessed. The write-enable pin is WE_N and the low- and high-byte read-enable pins are LDQ_L and LDQ_H, respectively. For greater flexibility in SDRAM support, the controller is parameterized by SDRCR register. The setting of this register is SDRAM devices dependent and the best matching value for a particular device should be selected according to the guidelines provided in Applications Notes for IP3210A Memory Controller Setting. The

The two static internal memory controllers share the same address lines A[-1], A[13]-A[16] (shared pins with CAS_N, RAS_N, BA[0]-BA[1]), A[17]-A[23] (shared pins with DQ[8]-DQ[15]). Controller 1 supports up to 4M bytes of range with memory mapping from 0x1FFC0000 to 0x1FFFFFFF and controller 2 supports 12M bytes of range with memory mapping from 0x1F000000 to 0x1FFBFFFF, respectively. The chip selects pins ROM_CS_1_N and ROM_CS_2_N are used to assert external memory 1 and 2, respectively. And for the corresponding memory region 0x1FFC0000 to 0x1FFFFFF is accessed.

The two generic static memory controllers can be individually programmed to operate in either parallel or serial mode depending upon the configuration in SROMEN register. Since generic static memory controller 1 is designed to support external flash device for firmware code storage, the parallel or serial mode is decided for this controller during the system boot-up process. In particular, the controller enters parallel mode if A[12] is pulled high when power-on reset is asserted; otherwise, it enters serial mode. The resulting mode is reported as 1 for parallel and 0 for serial in pfboot field (bit0) of SROMEN. On the other hand, the parallel or serial mode for generic static memory is programmed by firmware via the pflash field (bit1) of SROMEN with a value ‘1’ for parallel and ‘0’ for serial.

In parallel mode, the external memory access is achieved by execute any normal RISC supported memory read/write instructions to the corresponding external memory map region without the need of special commands. The parameters of the control registers, ROM1CR and ROM2CR, can be set according to the timing characteristics of the external memories connected to controller 1 and controller 2, respectively. The detailed description of the selection of these parameters can be found in Applications Notes for IP3210A Memory Controller Setting.

In serial mode, external memory access for controller 1 is achieved through the issue of command on SROM1CR with the read/write address location specified in SROM1Addr and the read/write data available in SROM1Data. Similarly, external memory access for controller 2 is achieved through SROM2CR, SROM2Addr and SROM2Data. Applications Notes for IP3210A Serial Flash Controller provides the detailed description of the serial mode operation.

4.2.12 Memory Map

The physical address for the control/status register, flash memory and the SDRAM is listed in Table 4-4.

Table 4-4 Reigsters and memory physical address mapping

Physical Address Range	Devices
0x0000-0000 - 0x01FF-FFFF (32 MB)	External SDRAM
0x0000-0000 - 0x0000-2FFF (8 KB)	Embedded CPU SRAM (I memory)
0x0020-0000 - 0x0020-0FFF (4 KB)	Embedded CPU SRAM (D memory)
0x0200-0000 - 0x02FF-FFFF	Reserved
0x0300-0000 - 0x03FFF-FFFF	System Control Registers
0x0F00-0000 - 0x0FFFF-FFFF	Reserved
0x0400-0000 - 0x0BFF-FFFF	Reserved
0x0C00-0000 - 0x0EFF-FFFF	Reserved
0x0F00-0000 - 0x1CFF-FFFF	Reserved
0x1F00-0000 - 0x1FFF-FFFF (16MB)	ROM/Flash (Static Memory 1 and 2)

4.2.13 GPIO/LED/JTAG Control

The only dedicated GPIO pin is GPIO[0]. This can serve as an external interrupt source if desirable. Other GPIO pins, GPIO[1]-GPIO[19], are shared pins with other functional pins such as the LED control, the UART, the JTAG pins. The GPIOSEL register (0xAF005010) is used to assign each of the GPIO pin as in GPIO function mode or the normal function mode. In addition, each GPIO pin can be configured as either an input or output pin by the GPIOD register (0xAF00500C). To provide more flexibility for coding convenient, the output of the GPIO pins can be controlled by firmware via two mechanisms. For the first mechanism, the firmware can write '1' and '0' to the corresponding field in GPIO register (0xAF005000) to pull a particular GPIO high and low, respectively. Alternatively, a particular GPIO pin can be pulled high by writing an '1' to the corresponding bit field in GPIOS register (0xAF005004) and can be pulled low by writing an '1' to the corresponding bit field in GPIOC register (0xAF005008).

A total of 15 LED control pins divided into 5 equivalent sets in which each set has 3 pins, LED_Link, LED_SPEED, LED_FULL. All LED functions are controlled by hardware and no firmware configuration is needed.

Four-wired standard JTAG interface is supported. No firmware configuration of the JTAG interface is needed.

5. Register Description

The symbols used in the following tables are listed below.
R/W: Read/Write attributes.
SC: Self-cleared after read.
PHY: PHY ID which should be included in a frame of Serial Management Interface.
MII: MII register address which should be included in a frame of Serial Management Interface.

5.1 Router and Peripheral

Note: The address of the router and peripheral shown in the following table is the virtual address. In the following tables, the register address is byte oriented and the lower address maps to the least significant byte.

5.1.1 Flash Memory/SDRAM Control

Register Address	Bit Location	R/W	Function	Default Value
AF000004	31	R/W	Polarity of ready signal, 0: rdy_busy_n =1 means “ready”; 1: rdy_busy_n =0 means “ready”	32’hFFFFFFFF Suggested value: 32’hf008010a
	30	R/W	Mask off busy signal. 1: ignore ready/busy signal. 0: Do not ignore ready signal.	
	29:25	R/W	OEW: Output enables width. Actual time period=(OEW + 1) * SDRAM clock cycle time	
	24:23	R/W	OEH: Out enable High Hold time. Actual time period= OEH * SDRAM clock cycle time	
	22:20	R/W	AVOEL: Address valid to OE Low. Actual time period= (AVOEL+1) * SDRAM clock cycle time	
	19:15	R/W	WEW: WE width Actual time period= (WEW+1) * SDRAM clock cycle time	
	14:13	R/W	WE High Hold time	
	12:10	R/W	AVWEL: Address valid to WE Low. Actual time period= (AVWEL+1) * SDRAM clock cycle time	
	9:5	R/W	CSW: Chip select width. Actual time period= CSW * SDRAM clock cycle time	
	4:3	R/W	CSH: CS High Hold time Actual time period=CSH * SDRAM clock cycle time	
	2:0	R/W	AVCSL: Address valid to CS Low. Actual time period= (AVCSL+2) * SDRAM clock cycle time	
0xAF000008	1	R/W	1:ROM2 is parallel flash, 0: ROM2 is serial flash	32’h000000000
	0	R	When power on reset, the SOC will sampling A[12] to determine it will use parallel flash or serial flash. A[12] pull down is serial flash mode	
0xAF000010~ 0xAF000014	20	R	SDRAM MRS has finished. 1: done	32’h0FFFFFFF
	19:17	R/W	SDRAM Write recovery time	
	16	R/W	Write to precharge delay in the same bank, SdramtDPL = sdrcr[16] + 1’b1	
	15	R/W	Mode register set cycle time, SdramtRSC = {1’b1,sdrcr[15]}	
	14:13	R/W	Mode register set control register	

Register Address	Bit Location	R/W	Function	Default Value
			00 : Mode Register Set 01: Precharge all bank 10: Auto refresh 11: Do nothing	
	12	R/W	0: CAS latency =2, 1: CAS latency = 3	
	11:10	R/W	Row size: 00 : 10 bit 01 : 11 bit 10 : 12 bit 11 : 13 bit	
	9:8	R/W	Column size: 00 : 8 bit 01 : 9 bit 10 : 10 bit 11 : 11 bit	
	7:6	R/W	Refresh clock mode, RFClkMode = { sdrcr[7:6],10'h3ff}	
	5:4	R/W	RAS cycle time, SdramtRC={2'b11,sdrcr[5:4]}	
	3:2	R/W	RAS to CAS delay time, SdramtRCD=sdrcr[3:2]	
0xBFFFFFF0~ 0xBFFFFFF3	31-24	R/W	Serial Flash Command register. Send from MSB. 03H: Read 0BH: Fast Read 9FH: Read ID 06H: Write Enable 04H: Write Disable D8H: Sector Erase C7H: Bulk Erase 02H: Page program 05H: Read from Status Register 01H: Write to Status Register B9H: Deep Power Down **Note:** not support Release from Deep Power Down and Read Electronic Signatures	32'h0FFFFFFF
	11-8	R/W	Number of cycles for SCK high	
	7-4	R/W	Number of cycles for SCK low	
	2-0	R/W	How many data want to read/write	
0xBFFFFFF4	23-0	R/W	Serial Flash Address register	32'h0FFFFFFF
0xBFFFFFF8	31-24	R/W	Serial Flash data the first byte	32'hFFFFFFFF
	23-16	R/W	Serial Flash data the second byte	
	15-8	R/W	Serial Flash data the third byte	
	7-0	R/W	Serial Flash data the four byte	
0xBFBFFFF0	31-24	R/W	Serial Flash Command register. Send from MSB	32'h0FFFFFFF
	11-8	R/W	Number of cycles for SCK High	
	7-4	R/W	Number of cycles for SCK low	
	2-0	R/W	How many data want to read/write	
0xBFBFFFF4	23-0	R/W	Serial Flash Address register	32'h0FFFFFFF
0xBFBFFF	31-0	R/W	Serial Flash data the first byte	32'h0FFFFFFF

Register Address	Bit Location	R/W	Function	Default Value
F8				

5.1.2 Timer

Register Address	Bit Location	R/W	Function	Default Value
0xAF001000	19:0	R/W	Timer 1 L: Up Counter, Up to Timer 1 H then reset to 0	32'h00000000
0xAF001004	19:0	R/W	Timer 1 H: Timer 1 period setting	32'hFFFFFFFF
0xAF001008	19:0	R/W	20-bit Prescaler for Timer 1	32'hFFFFFFFF
0xAF00100C	2	R/W	Timer1 enable, 1: enable	32'h00000000
	1	R/W	Timer 1 interrupt enable, 1: enable	
	0	R/W	1: Timer 1 L auto restart when Timer 1 expires. 0: Timer 1 L stops when Timer1 expires.	
0xAF001010	0	R/W	Timer 1 interrupt status, write 1 to clear the status	32'h00000000
0xAF001014	19:0	R/W	Timer 2 L: Up Counter, Up to Timer 2 H then reset to 0	32'h00000000
0xAF001018	19:0	R/W	Timer 2 H: Timer 2 period setting	32'hFFFFFFFF
0xAF00101C	19:0	R/W	20-bit Prescaler for Timer 2	32'hFFFFFFFF
0xAF001020	2	R/W	Timer2 enable, 1: enable	32'h00000000
	1	R/W	Timer 2 interrupt enable, 1:enable	
	0	R/W	1: Timer 2 L auto restart when Timer 2 expires. 0: Timer 2 L stop when Timer2 expires.	
0xAF001024	0	R/W	Timer 2 interrupt status, write 1 to clear the status	32'h00000000
0xAF001028	0	R/W	Watchdog Timer L: Up Counter, up to Watchdog Timer H. Depends on WDmode setting, it will reset to 0 or keep it as WDTimerH.	N/A
0xAF00102C	19:0	R/W	Watchdog Timer H: Watchdog timer period setting.	32'hFFFFFFFF
0xAF001030	19:0	R/W	20-bit Prescaler for Watchdog timer	32'h00FFFFFF
0xAF001034	3	R/W	Watchdog mode or timer mode. 1: Watchdog mode: When Timer WD expires will reset SOC 0: Timer mode:	32'h00000008
	2	R/W	WDTimer enable, 1: enable	
	1	R/W	Watchdog Timer interrupt enable, 1: enable	
	0	R/W	1: Timer WD L auto restart when Timer WD expires. 0: Timer WD L stops when Timer WD expires.	
0xAF001038	3	R	Watchdog Timer interrupt status, write 1 to clear This bit does not reset by power on, software can check this bit for system start by power up or watch dog reset.	32'h00000000

5.1.3 UART

Register Address	Bit Location	R/W	Function	Default Value
0xAF002000	31-24	R/W	Data port of UART, write to this data port for TX Read from this port for RX	32'h00000000
	23	R	RX buffer is ready to read	
0xAF002004	31:16	R/W	Baud rate counter: For 25MHz system clock (FPGA). 9600 baud: Baudrate = 0xa2c (2604) 115200 baud: Baudrate = 0xd9 (217)	0100001070
	15	R/W	TX interrupt enable, 1: enable	
	14	R/W	RX interrupt enable, 1: enable	
	13	R/W	Parity bit enable, 1: enable	
	12	R/W	1: even parity, 0: odd parity	
	11	R/W	0: 1 stop bit, 1: 2 stop bit	
	10	R/W	1: internal loop back enable	
	9	R/W	Current RX byte parity	
	8	R/W	Parity error	
	7	R/W	Framing error	
	6:4	R/W	Threshold for number of bytes to generate interrupt. RX will generate interrupt if RX data bytes bigger than RxThreshold or there are RX data and time out.	
	2	R	1: TX buffer empty	
	1	R	1: RX buffer ready to read	
	0	R	TX data is on going	

5.1.4 SMI control/Router Control Register

Register Address	Bit Location	R/W	Function	Default Value
0xAF003000	31	R/W	Start (self-clearing)	32'h00000000
	30	R/W	Write enable	
	28:24	R/W	Phy/Switch address (phy:0~4, sw:20~26)	
	20:16	R/W	Switch register address	
	15:0	R/W	Write/Read data to/from Switch	
0xAF003004	31:24	R/W	Set MDC clock period	32'h0d018000
	23	R/W	Enable external hardware descriptor	
	22:21	-	Reserve	
	20	R/W	Enable bandwidth control	
	19	R/W	Hash mode (1:direct mapping, 0:crc10)	
	18	R/W	Enable HMU cache function	
	17	R/W	Enable HMU	
	16	R/W	Generate reverse direction NAT Index	
	15	R/W	Disable NAT prefetch	
	14	R/W	NAT table size, 1:32B; 0:24B	
	13	R/W	Tx retry enable	
	12	R/W	TxDMA enable	
	11	R/W	Router look back	
	10	R/W	Bypass look up	
	9	R/W	Tx flow control enable	
	8	R/W	TXMAC enable	

Register Address	Bit Location	R/W	Function	Default Value
	7	R/W	Bypass NAT replacement	
	6	R/W	Send all receiving packet to CPU	
	5	R/W	Hardware NAT enable	
	4	R/W	RxDMA enable	
	3	R/W	Tx MAC enable	
	2	R/W	Rx Flow control enable	
	1	R/W	Rx MAC enable	
	0	R/W	Look back enable	
0xAF003008	23:0	R/W	Receive Descriptor based address	32'h00000000
0xAF00300C	23:0	R/W	External hardware descriptor based address	32'h00000000
0xAF003010	23:0	R/W	Indicate first buffer address	32'h00000000
0x AF003014	23:16	R/W	L3 header starting address	32'h00320004
	15:8	-	Reserve	
	7:0	R/W	Descriptor Length (unit : word)	
0xAF00301C	28	R/W	Indicate VLAN ID1 is Inbound or Outbound	32'h00000000
	27:16	R/W	VLAN ID1	
	12	R/W	Indicate VLAN ID0 is Inbound or Outbound	
	11:0	R/W	VLAN ID0	
0xAF003020	28	R/W	Indicate VLAN ID3 is Inbound or Outbound	32'h00000000
	27:16	R/W	VLAN ID3	
	12	R/W	Indicate VLAN ID2 is Inbound or Outbound	
	11:0	R/W	VLAN ID2	
0xAF003024	28	R/W	Indicate VLAN ID5 is Inbound or Outbound	32'h00000000
	27:16	R/W	VLAN ID5	
	12	R/W	Indicate VLAN ID4 is Inbound or Outbound	
	11:0	R/W	VLAN ID4	
0xAF003028	28	R/W	Indicate VLAN ID7 is Inbound or Outbound	32'h00000000
	27:16	R/W	VLAN ID7	
	12	R/W	Indicate VLAN ID7 is Inbound or Outbound	
	11:0	R/W	VLAN ID7	
0xAF00303C	31:0	R/W	Router MAC address0	32'h00000000
0xAF003040	15:0	R/W	Router MAC address0	32'h00000000
0xAF003044	31:0	R/W	Router MAC address1	32'h00000000
0xAF003048	15:0	R/W	Router MAC address1	32'h00000000
0xAF00304C	31	R/W	Buffer Auto-Polling On.	32'h00000000
	30:16	R/W	Setting Auto polling timer	
	5	R/W	SW descriptor auto-polling on	
	4	R/W	HW descriptor auto-polling on (Reserved)	
	2	R/W	Software inform RxDMA has software descriptor	
	1	R/W	Software inform RxDMA has hardware descriptor (Reserved)	

Register Address	Bit Location	R/W	Function	Default Value
	0	R/W	Software informs RxDMA has free buffer.	
0xAF003064	23:0	R/W	TxDMA software descriptor based address	32'h00000000
0xAF003080	14:8	R/W	SW can use this to control un-recognized packet's starting stored address	32'h00040e00
	3	R/W	L2TP support disable	
	2	R/W	TCP support disable	
	1	R/W	UDP support disable	
	0	R/W	GRE support disable	
0xAF0030C0	0	R/W	Software trigger TxDMA if there is packet to be transmitted	32'h00000000
0xAF0030D4	23:0	R/W	Last Buffer address in buffer link list	32'h00000000
0xAF0030D8	23:0	R/W	TxDMA current HW descriptor address	32'h00000000
0xAF0030DC	23:0	R/W	TxDMA current SW descriptor address	32'h00000000
0xAF003200	31:16	R	Total receiving packet number	32'h00000000
	15:0	R	Number of receiving packet to CPU	
0xAF003204	31:16	R	Tx HW packet counter	32'h00000000
	15:0	R	Tx SW packet counter	
0xAF003210	15:0	R	Rx from Switch counter	32'h00000000

5.1.5 Interrupt controller

Register Address	Bit Location	Read/ Write	Function	Default Value
0xAF004000	31-18	R	Current State of interrupt source	32'hFFFCFFFC
	15-2	R/W	write 1 to clear interrupt	
0xAF004004	31-18	R/W	If polarity is the same as cause and the mask is turned off, the interrupt is activated.	32'hFFFCFFFC
	15-2	R/W	Interrupt mask, set 0 to enable interrupt	
0xAF004008	31-28	R/W	Interrupt source selection 15	32'hFEDCBA98
	27-24	R/W	Interrupt source selection 14	
	23-20	R/W	Interrupt source selection 13	
	19-16	R/W	Interrupt source selection 12	
	15-12	R/W	Interrupt source selection 11	
	11-8	R/W	Interrupt source selection 10	
	7-4	R/W	Interrupt source selection 9	
	3-0	R/W	Interrupt source selection 8	
0xAF00400C	31-28	R/W	Interrupt source selection 7	32'h76543200
	27-24	R/W	Interrupt source selection 6	
	23-20	R/W	Interrupt source selection 5	
	19-16	R/W	Interrupt source selection 4	
	15-12	R/W	Interrupt source selection 3	
	11-8	R/W	Interrupt source selection 2	

5.1.6 GPIO

Register Address	Bit Location	Read/ Write	Function	Default Value
0xAF005000	19-0	R/W	GPIO Data. Writing “1” or “0” will force the corresponding I/O pin to the desired state if the corresponding bit is set to output mode.	32’h00000000
0x AF005004	19-0	R/W	GPIO Data. Writing “1” to the specified bit will force the corresponding I/O pin to “1”. Writing “0” will not change the I/O corresponding pin state. In the other word, an “OR” operation is executed to get the final state.	32’h00000000
0x AF005008	19-0	R/W	GPIO Data. Writing “1” to the specified bit will force the corresponding I/O pin to “0”. Writing “0” will not change the I/O corresponding pin state. In the other word, a “NOR” operation is executed to get the final state.	32’h00000000
0xAF00500C	19-0	R/W	Input/Output direction of GPIO. 1:outpit, 0:input	32’h00000000
0xAF005010	19-0	R/W	Shared pin selections. 1: GPIO mode, 0: normal function mode	32’h00000000
0xAF005018	1-0	R/W	Internal PLL selections {DC1,DC0}=00: Reserved {DC1,DC0}=01: Reserved {DC1,DC0}=10: CK_CPU=150MHz, CK_SYS = 150MHz {DC1,DC0}=11: CK_CPU=125MHz, CK_SYS = 125MHz	32’h00000003

5.2 MII Registers of PHY0~4

(Each PHY has its own MII registers with different PHY address)

PHY	MII	R/W	Description	Default
4~0	0.15	R/W SC	Reset The PHY is reset if user writes “1” to this bit. The reset period is around 2ms. User has to wait for at least 2ms to access the PHY part.	0
4~0	0.14	R/W	Loop back 1 = Loop back mode 0 = normal operation When this bit set, The PHY part will be isolated from the network media, that is, the assertion of TXEN at the MII will not transmit data on the network. All MII transmission data will be returned to MII receive data path in response to the assertion of TXEN. Bit 0.12 is cleared automatically, if this bit is set. User has to program bit 0.12 again after loop back test.	0
4~0	0.13	R/W	Speed Selection 1 = 100Mbps 0 = 10Mbps It is valid only if bit 0.12 is set to be 0.	1
4~0	0.12	R/W	Auto-Negotiation Enable 1 = Auto-Negotiation Enable 0 = Auto-Negotiation Disable	1
4~0	0.11	R/W	Power Down 1: power down mode 0: normal operation	0
4~0	0.10		Isolate The PHY part doesn’t support this function.	0
4~0	0.9	R/W SC	Restart Auto-Negotiation 1 = restart Auto-Negotiation process 0 = normal operation Setting this bit to logic high will cause THE PHY PART to restart an Auto-Negotiation cycle, but depending on the value of bit 0.12 (Auto-Negotiation Enable). If bit 0.12 is cleared then this bit has no effect, and it is Read Only. This bit is self-clearing after Auto-Negotiation process has been initiated.	0
4~0	0.8	R/W	Duplex mode 1 = full duplex 0 = half duplex It is valid only if bit 0.12 is set to be 0.	0
4~0	0.7	R/W	Collision test	0
4~0	0[6:0]	RO	Reserved	0
4~0	1.15	RO	100Base-T4 capable 1 = 100Base-T4 capable 0 = not 100Base-T4 capable THE PHY PART does not support 100Base-T4. This bit is fixed to be 0.	0
4~0	1.14	RO	100Base-X full duplex Capable 1 = 100Base-X full duplex capable 0 = not 100Base-X full duplex capable	1
4~0	1.13	RO	100Base-X half duplex Capable 1 = 100Base-X half duplex capable 0 = not 100Base-X half duplex capable	1

PHY	MII	R/W	Description	Default
4~0	1.12	RO	10Base-T full duplex Capable 1 = 10Base-T full duplex capable 0 = not 10Base-T full duplex capable	1
4~0	1.11	RO	10Base-T half duplex Capable 1 = 10Base-T half duplex capable 0 = not 10Base-T half duplex capable	1
4~0	1[10:7]	RO	Reserved	0
4~0	1.6	RO	MF preamble Suppression 1 = preamble may be suppressed 0 = preamble always required	1
4~0	1.5	RO	Auto-Negotiation Complete 1 = Auto-Negotiation complete 0 = Auto-Negotiation in progress When read as logic 1, indicates that the Auto-Negotiation process has been completed, and the contents of register 4 and 5 are valid. When read as logic 0, indicates that the Auto-Negotiation process has not been completed, and the contents of register 4 and 5 are meaningless. If Auto-Negotiation is disabled (bit 0.12 set to logic 0), then this bit will always read as logic 0.	0
4~0	1.4	RO LH	Remote fault 1 = remote fault detected 0 = not remote fault detected When read as logic 1, indicates that THE PHY PART has detected a remote fault condition. This bit is set until remote fault condition gone and before reading the contents of the register. This bit is cleared after THE PHY PART reset.	0
4~0	1.3	RO	Auto-Negotiation Ability 1 = Auto-Negotiation capable 0 = not Auto-Negotiation capable When read as logic 1, indicates that THE PHY PART has the ability to perform Auto-Negotiation.	1
4~0	1.2	RO LL	Link Status 1 = Link Pass 0 = Link Fail When read as logic 1, indicates that the PHY part has determined a valid link has been established. When read as logic 0, indicates the link is not valid. This bit is cleared until a valid link has been established and before reading the contents of this registers.	0
4~0	1.1		Jabber Detect 1 = jabber condition detected 0 = no jabber condition detected When read as logic 1, indicates that the PHY part has detected a jabber condition. This bit is always 0 for 100Mbps operation and is cleared after the PHY part reset. When the duration of TXEN exceeds the jabber timer (21ms), the transmission and loop back functions will be disabled and the COL is active. After TXEN goes low for more than 500 ms, the transmitter will be re-enabled.	0
4~0	1.0	RO	Extended capability 1 = Extended register capabilities 0 = No extended register capabilities The PHY part has extended register capabilities.	1
4~0	2	RO	The PHY part OUI (Organizationally Unique Identifier) ID, the MSB is	16'h0243

PHY	MII	R/W	Description	Default
			3rd bit of the PHY part OUI ID, and the LSB is 18th bit of the PHY part OUI ID. The PHY part OUI is 0090C3.	
4~0	3[15:10]	RO	PHY identifier The PHY part OUI ID, the MSB is 19th bit of the PHY part OUI ID, and LSB is 24th bit of the PHY part OUI ID.	6'h03
4~0	3[9:4]	RO	Manufacture's Model Number the PHY part model number	6'h18
4~0	3[3:0]	RO	Revision Number the PHY part revision number	0
4~0	4.15	RO	Next Page Not supported. This bit is fixed to be 0.	0
4~0	4.14	RO	Reserved by IEEE, write as 0, ignore on read	0
4~0	4.13	R/W	Remote Fault 1: Advertises that this port has detected a remote fault. 0: There is no remote fault.	0
4~0	4[12:11]	RO	Reserved for future IEEE use, write as 0, ignore on read	0
4~0	4.10	R/W	Pause 1 = Advertises that this port has implemented pause function 0 = No pause function supported	
4~0	4.9	RO	100BASE-T4 Not supported	0
4~0	4.8	R/W	100BASE-TX full duplex 1 = 100BASE-TX full duplex is supported 0 = 100BASE-TX full duplex is not supported	*

FORCE	FORCE100	FORCE_FULL	Default
0	Don't care	Don't care	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

4~0	4.7	R/W	100BASE-TX 1 = 100BASE-TX is supported 0 = 100BASE-TX is not supported	*

FORCE	FORCE100	FORCE_FULL	Default
0	Don't care	Don't care	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

4~0	4.6	R/W	10BASE-T full duplex 1 = 10BASE-T full duplex is supported 0 = 10BASE-T full duplex is not supported	*

FORCE	FORCE100	FORCE_FULL	Default
0	Don't care	Don't care	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

4~0	4.5	R/W	10BASE-T 1 = 10BASE-T is supported 0 = 10BASE-T is not supported	1

PHY	MII	R/W	Description	Default
4~0	4[4:0]	RO	Selector Field Use to identify the type of message being sent by Auto-Negotiation.	5'b00001
4~0	5.15	RO	Next Page 1 = Next Page ability is supported by link partner 0 = Next Page ability does not supported by link partner	0
4~0	5.14	RO	Acknowledge 1 = Link partner has received the ability data word 0 = Not acknowledge	0
4~0	5.13	RO	Remote Fault 1 = Link partner indicates a remote fault 0 = No remote fault indicate by link partner If this bit is set to logic 1, then bit 1.4 (Remote fault) will set to logic 1.	0
4~0	5[12:11]	RO	Reserved by IEEE for future use, write as 0, and read as 0.	0
4~0	5.10	R/W	Pause 1 = Link partner support IEEE802.3x 0 = Link partner does not support IEEE802.3x When Auto-negotiation enabled, this bit reflects link partner ability. (read only) When Auto-negotiation disabled, this bit can be set by SMI. (read/write) When in 100FX, this bit is set by X_EN or SMI.	0
4~0	5.9	RO	100BASE-T4 1 = Link partner support 100BASE-T4 0 = Link partner does not support 100BASE-T4	0
4~0	5.8	RO	100BASE-TX full duplex 1 = Link partner support 100BASE-TX full duplex 0 = Link partner does not support 100BASE-TX full duplex	0
4~0	5.7	RO	100BASE-TX 1 = Link partner support 100BASE-TX 0 = Link partner does not support 100BASE-TX For 100FX mode, this bit is set. When Auto-negotiation is disabled, this bit is set if register 0.13=1.	0
4~0	5.6	RO	10BASE-T full duplex 1 = Link partner support 10BASE-T full duplex 0 = Link partner does not support 10BASE-T full duplex	0
4~0	5.5	RO	10BASE-T 1 = Link partner support 10BASE-T 0 = Link partner does not support 10BASE-T When Auto-negotiation is disabled, this bit is set if register 0.13=0	0
4~0	5[4:0]	RO	Selector Field Protocol selector of the link partner	5'b00000
4~0	6[15:5]	RO	Reserved	0
4~0	6.4	RO	1: a fault has been detected via parallel detection function. 0: a fault has not been detected via parallel detection function.	0
4~0	6.3	RO	1= Link partner is next page able. 0= Link partner is not next page able.	0
4~0	6.2	RO	1: the PHY part next page able. 0: the PHY part is not next page able. This bit is fixed to be "0" in the PHY part	0
4~0	6.1	RO/ LH	1: A new page has been received. 0: A new page has not been received.	0

PHY	MII	R/W	Description	Default
4~0	6.0	RO	If Auto-negotiation is enabled, this bit means: 1: Link partner is Auto-Negotiation able. 0: Link partner is not Auto-Negotiation able. In 100FX or Auto-negotiation disabled, this bit always =0.	0 (100FX)
4~0	16.7	R/W	Link down power saving mode 1 = Enable LDPS mode 0 = Disable LDPS mode	1

5.3 Switch Control/Status Register

The register map is listed as the following tables.

PHY ID	MII Reg.	Description
20	0	Chip ID
	1	Reserved
	2	System Reset
	3	
	4	Force Mode
	5	Congestion Control
	6	Physical Port Status
	7	Illegal Packet Filter
	8	Packet ID
	9	
	10	
	11	
	12	Network Security
	13	Address Learning Control
	14	Aging Time Parameter
	15	
	16	Broadcast Storm Protection
	17	
	18	
	19	
	20	Port Mirroring
	21	
	22	Source Block Protection
	23	Reserved
	24	LED Control Register
	25	Reserved
	26	
	27	
	28	
	29	
	30	
	31	

PHY ID	MII Reg.	Description
21	0	Reserved
	1	
	2	
	3	
	4	
	5	IGMP Control
	6	
	7	
	8	Rate Control
	9	
	10	
	11	Reserved
	12	Rate Control
	13	Reserved
	14	Address Table Access
	15	
	16	
	17	
	18	
	19	
	20	CPU Interrupt
	21	
	22	Miscellaneous Control
	23	
	24	
	25	CRC Error Counter
	26	Reserved
	27	
	28	
	29	
	30	
	31	

PHY ID	MII Reg.	Description
22	0	VLAN Control
	1	
	2	
	3	
	4	
	5	
	6	
	7	
	8	
	9	
	10	
	11	VLAN Table
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20	
	21	
	22	
	23	
	24	
	25	
	26	
	27	
	28	
	29	
	30	Reserved
	31	

PHY ID	MII Reg.	Description
23	0	VLAN Table
	1	
	2	
	3	
	4	
	5	
	6	
	7	
	8	
	9	
	10	
	11	
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20	
	21	
	22	
	23	
	24	
	25	
	26	
	27	
	28	
	29	
	30	
	31	

PHY ID	MII Reg.	Description
24	0	VLAN Table
	1	
	2	
	3	
	4	Reserved
	5	
	6	
	7	
	8	
	9	
	10	
	11	
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20	
	21	
	22	
	23	
	24	
	25	
	26	
	27	
	28	
	29	
	30	
	31	

PHY ID	MII Reg.	Description
25	0	Priority Classification
	1	
	2	
	3	
	4	
	5	
	6	
	7	
	8	
	9	
	10	
	11	
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20	
	21	
	22	Queue Scheduling Mode
	23	
	24	Reserved
	25	
	26	
	27	
	28	
	29	
	30	
	31	

PHY ID	MII Reg.	Description
26	0	Multi-field Classification
	1	
	2	
	3	
	4	
	5	
	6	
	7	
	8	
	9	
	10	
	11	
	12	
	13	
	14	
	15	
	16	
	17	
	18	
	19	
	20	
	21	
	22	
	23	
	24	Reserved
	25	
	26	
	27	
	28	
	29	
	30	
	31	

PHY	MII	R/W	Description	Default
20	0[15:0]	RO	Reserved	175D
20	2[15:0]	R/W	SOFT_RESET[15:0] Software reset register The PHY part is reset if uses write hexadecimal “175D” to this register. It is self-cleared. The reset period is around 2ms. User has to wait for at least 2 ms to access the PHY part. When read this register, it shows the internal status of the switch part.	16’h00
	3[1:0]	R/W	TABLE_LOCK[1:0] Lock content of table. Bit[1]: Multi-Field table Bit[0]: Address table	2’b00
20	4.15	R/W	MAC5_FORCE_100 1: force MAC5 to be 100M 0: force MAC5 to be 10M	1
20	4.14	R/W	MAC4_FORCE_100 1: force MAC4 to be 100M 0: force MAC4 to be 10M	1
20	4.13	R/W	MAC5_FORCE_FULL 1: force MAC5 to be full duplex 0: force MAC5 to be half duplex	1
20	4.12	R/W	MAC4_FORCE_FULL 1: force MAC4 to be full duplex 0: force MAC4 to be half duplex	1
20	5[15:9]		RESERVED	
	5[8]	R/W	CONT_PAUSE To continuously send pause packet 1:enable 0:disable	1’b0
	5[7]	R/W	MOD_CARRIER_ALGORITHM Modified carrier based collision algorithm 1:enable 0:disable	1’b0
	5[6]	R/W	INPUT_FILTER 1: enable 0: disable	1’b0
	5[5]	R/W	DROP16 Drop input packet after 16 times collision in succession.	1’b0
	5[4]	R/W	MODBCK Modified backoff collision algorithm	1’b1
	5[3]	R/W	BP_KIND Backpressure Kind 0: carrier based 1: collision based	1’b0
	5[2]	R/W	BK_EN Backpressure enable 1: enable (default), 0: disable	*

PHY	MII	R/W	Description		Default
	5[1]	R/W	X_EN IEEE 802.3x flow control enable This signal is used as PAUSE_EN for digital parts. This register valid only if the pause capability of PHY is enabled. 1: enable (default), 0:disable		
	5[0]	R/W	MAC_X_EN Flow control enable of MII0-2 1: enable (default) 0: disable		
20	6[13:8]	R/W	FORWARD_EN[5:0] Frame forwarding capability enable for each port		6'h3F
			bit 5	1: enable frame forwarding capability of port 5 0: disable frame forwarding capability of port 5	
			bit 4	1: enable frame forwarding capability of port 4 0: disable frame forwarding capability of port 4	
			bit 3	1: enable frame forwarding capability of port 3 0: disable frame forwarding capability of port 3	
			bit 2	1: enable frame forwarding capability of port 2 0: disable frame forwarding capability of port 2	
			bit 1	1: enable frame forwarding capability of port 1 0: disable frame forwarding capability of port 1	
			bit 0	1: enable frame forwarding capability of port 0 0: disable frame forwarding capability of port 0	
	6[5:0]	R/W	LEARNING_EN[5:0] MAC address Learning capability enable for each port		6'h3F
			bit 5	1: enable address learning capability of port 5 0: disable address learning capability of port 5	
			bit 4	1: enable address learning capability of port 4 0: disable address learning capability of port 4	
			bit 3	1: enable address learning capability of port 3 0: disable address learning capability of port 3	

PHY	MII	R/W	Description		Default
			bit 2	1: enable address learning capability of port 2 0: disable address learning capability of port 2	
			bit 1	1: enable address learning capability of port 1 0: disable address learning capability of port 1	
			bit 0	1: enable address learning capability of port 0 0: disable address learning capability of port 0	
20	7[15:5]		RESERVED		
	7[4:3]	R/W	LONG_FRM[1:0] Max forwarded packet length 00: 1536 bytes (default) 01: 1552 bytes 10: 1792 bytes 11: reserved		2'b00
	7[2]	R/W	MC_SMC Filter Frame with multicast source MAC address		1'b0
	7[1]	R/W	NULL_MAC Filter Frame with null source or destination MAC address		1'b0
	7[0]	R/W	CRC_ERROR Filter CRC Frame		1'b1
20	8[15:14]	R/W	TRAP_RSVD_ADDR1[1:0] Reserved address range 1 Reserved MAC address is from 01:80:C2:00:00:11 to 01:80:C2:00:00:1F 00: forward (default) 01: forward to CPU 10: discard 11: reserved		2'b00
	8[13:12]	R/W	TRAP_ABM[1:0] All Bridges Multicast address defined by IEEE 802.1D Reserved MAC address is 01:80:C2:00:00:10 00: forward (default) 01: forward to CPU 10: discard 11: reserved		2'b00
	8[11:10]	R/W	TRAP_RSVD_ADDR0[1:0] Reserved address range 0 Reserved MAC address is from 01:80:C2:00:00:04 to 01:80:C2:00:00:0D, 01:80:C2:00:00:0F 00: forward (default) 01: forward to CPU 10: discard 11: reserved		2'b00

PHY	MII	R/W	Description	Default
	8[9:8]	R/W	TRAP_LLDP[1:0] Link Layer Discovery Protocol Reserved MAC address is 01:80:C2:00:00:0E LLDP Data Units (LLDPDUs) encoded with an Ethertype value of 0x88CC. 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
20	8[7:6]	R/W	TRAP_802P1X[1:0] IEEE 802.1X Port-Based Network Access Control Reserved MAC address is 01:80:C2:00:00:03 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	8[5:4]	R/W	TRAP_SP[1:0] IEEE 802 standard protocol – Slow Protocols Reserved MAC address is 01:80:C2:00:00:02 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	8[3]		RESERVED	
	8[2]	R/W	TRAP_PAUSE Point-to-Point Pause function Reserved MAC address is 01:80:C2:00:00:01 1: forward 0: discard (default)	1'b0
	8[1:0]	R/W	TRAP_BPDU[1:0] Standard Spanning Tree Protocol Reserved MAC address is 01:80:C2:00:00:00 00: forward (default) 01: forward to CPU 10: discard 11: reserved	*

PHY	MII	R/W	Description	Default
20	9[15:8]		RESERVED	
	9[7:6]	R/W	TRAP_RSVD_ADDR3[1:0] Reserved address range 3 Reserved MAC address is from 01:80:C2:00:00:30 to 01:80:C2:00:00:FF 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	9[5:4]	R/W	TRAP_RSVD_ADDR2[1:0] Reserved address range 2 Reserved MAC address is from 01:80:C2:00:00:22 to 01:80:C2:00:00:2F 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	9[3:2]	R/W	TRAP_GVRP[1:0] GVRP Address: 01-80-C2-00-00-21 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	9[1:0]	R/W	TRAP_GMRP[1:0] GMRP Address: 01-80-C2-00-00-20 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
20	10[15:14]	R/W	TRAP_ICMP Internet Control Message Protocol ICMPv4: TYPE=0x0800 and Protocol=1 ICMPv6: TYPE=0x86DD and Protocol=58 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	10[13:12]	R/W	TRAP_MLD_CTRL MLD Control Packet DMAC=33-33-XX-XX-XX-XX EtherType=0x86DD Version=6 Next Header=58 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00

PHY	MII	R/W	Description	Default
	10[11:10]	R/W	TRAP_MLD Multicast Listener Discovery DMAC=33-33-XX-XX-XX-XX EtherType=0x86DD Version=6 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	10[9:8]	R/W	TRAP_IPM_DATA IP Multicast Data Packet DMAC=01-00-5E-XX-XX-XX EtherType=0x0800 Version=4 DIP=224.0.1.0~239.225.225.225 Protocol is not IGMP 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	10[7:6]	R/W	TRAP_IPM_CTRL IP Multicast Control Packet DMAC=01-00-5E-XX-XX-XX EtherType=0x0800 Version=4 DIP=224.0.0.x Protocol is not IGMP 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	10[5:4]	R/W	TRAP_IGMP Internet Group Management Protocol DMAC=01-00-5E-XX-XX-XX EtherType=0x0800 Version=4 Protocol=2(IGMP) 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00

PHY	MII	R/W	Description	Default
	10[3:2]	R/W	TRAP_RARP[1:0] Reverse Address Resolution Protocol The destination MAC address is FF: FF: FF: FF: FF: FF and Ether-Type field is 0x8035 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	10[1:0]	R/W	TRAP_ARP[1:0] Address Resolution Protocol The destination MAC address is FF: FF: FF: FF: FF: FF and Ether-Type field is 0x0806 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
20	11[15:4]		RESERVED	
	11[3:2]	R/W	TRAP_BOOTP Bootstrap Protocol Port Number=16'd67 or 16'd68 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00
	11[1:0]	R/W	TRAP_PPPoE Point-to-Point Protocol over Ethernet Ether-Type=0x8863 or 0x8864 00: forward (default) 01: forward to CPU 10: discard 11: reserved	2'b00

PHY	MII	R/W	Description	Default
20	12[14]	R/W	ILL_SMAC_2CPU Illegal SMAC to CPU 0: If frame with illegal SMAC, discard it. 1: If frame with illegal SMAC, forward it to CPU.	1'b0

PHY	MII	R/W	Description	Default
	12[13:8]	R/W	ILL_SMAC_PROT[5:0] Illegal source MAC address protection 0: disable 1: enable. Bit[0]: port 0 Bit[1]: port 1 Bit[2]: port 2 Bit[3]: port 3 Bit[4]: port 4 Bit[5]: port 5	6'h00
	12[7:6]		RESERVED	
	12[5:0]	R/W	CHK_PORT[5:0] The frame is examined based on the combination of SMAC and ingress port number in address table. Bit[0]: port 0 Bit[1]: port 1 Bit[2]: port 2 Bit[3]: port 3 Bit[4]: port 4 Bit[5]: port 5 It is valid only if the corresponding ILL_SMAC_PROT bit is enabled	6'b111111
20	13[15:10]		RESERVED	
	13[9:8]	R/W	FILTER_MDMAC Filter unknown multicast DMAC 2'b00 : Flooding 2'b01 : Forward to CPU 2'b10 : Discard 2'b11 : Reserved Note : Multicast DMAC does not include broadcast DMAC	2'b00
	13[7:6]	R/W	FILTER_UDMAC Filter unknown unicast DMAC 2'b00 : Flooding 2'b01 : Forward to CPU 2'b10 : Discard 2'b11 : Reserved	2'b00
	13[5]	R/W	LEARN_DIS_PAUSE Learning disable because of PAUSE frame	1'b1
	13[4]	R/W	RESERVED	
	13[3]	R/W	AT_STR Address Table Structure 0: 2K Address Table for unicast frame (default) 1: 1K Address Table for unicast frame and 1K Address Table for multicast frame Note – We recommend clear address table once this bit is modified.	0
	13[2]		RESERVED	

PHY	MII	R/W	Description	Default
	13[1]	R/W	IGMP_OVER_VLAN 0 : Disable 1 : Enable It is valid only for LEARN_CONSTRAIN is enabled	0
	13[0]	R/W	LEARN_CONSTRAIN Learning Constraint 0 : VLAN information(FID) is not used to create a hash key 1 : VLAN information(FID) is used to create a hash key Note – We recommend clear address table once this bit is modified.	1'b0
20	14[15:7]		RESERVED	
	14[6:5]	R/W	AGE_TIME_UNIT 2'b00 : 1 minutes 2'b01 : 1 second 2'b10 : 10 ms 2'b11 : fast	2'b00
	14[4:0]	R/W	AGE_TIME_VLE Age Time Value. 5'h00: no aging AGE_TIME= AGE_TIME_UNIT * AGE_TIME_VLE	5'h05
	15[15:9]		RESERVED	
	15[8]	R/W	PID_EN If set, the aging module ages entries whose Port ID matches PID_VAL	1'b0
	15[7:5]	R/W	PID_VAL[2:0] Port ID Value 3'b000 : reserved (default) 3'b001 : port 0 3'b010 : port 1 3'b011 : port 2 3'b100 : port 3 3'b101 : port 4 3'b110 : port 5 (CPU port) other : reserved	3'b000
	15[4]	R/W	FID_EN If set, the aging module ages entries whose FID matches FID_VAL 0: Disable 1: Enable	1'b0
	15[3:0]	R/W	FID_VAL[3:0] FID Value	4'h0
20	16[15:14]		RESERVED	
	16[13:8]	R/W	BF_STM_EN[5:0] Broadcast storm enable 1: enable Drop the incoming packet if the number of queued broadcast packet is over the threshold. The threshold is defined in MII register 20.17~20.19 0: disable (default)	6'h0
	16[7:6]		RESERVED	

PHY	MII	R/W	Description	Default
	16[5:0]	R/W	BF_FFFF_ONLY[5:0] Multicast broadcast storm protection disable 1: “Broadcast storm protection” does not include multicast packets. the PHY part drops the packets with DA equals to 0xFFFFFFFF only when the broadcast threshold is reached (default), 0: “Broadcast storm protection” includes multicast packets. The PHY part drops the packets with DA equals to 0xFFFFFFFFF, or multi-cast address when the broadcast threshold is reached. “Broadcast storm protection” does not drop packets due to not learned address.	6’h3f
	17[15:8]	R/W	BF_STM_THR_1[7:0] Broadcast storm threshold setting for port 1	8’h08
	17[7:0]	R/W	BF_STM_THR_0[7:0] Broadcast storm threshold setting for port 0 Threshold setting range is from 1 to 255 packets/10ms for 100Mbps connection or 1 to 255 packets/100ms for 10Mbps connection	8’h08
	18[15:8]	R/W	BF_STM_THR_3[7:0] Broadcast storm threshold setting for port 3	8’h08
	18[7:0]	R/W	BF_STM_THR_2[7:0] Broadcast storm threshold setting for port 2	8’h08
	19[15:8]	R/W	BF_STM_THR_5[7:0] Broadcast storm threshold setting for port 5	8’h08
	19[7:0]	R/W	BF_STM_THR_4[7:0] Broadcast storm threshold setting for port 4	8’h08

PHY	MII	R/W	Description	Default
20	20[15]	R/W	PORT_MIRROR_EN	1’b0
	20[14:13]	R/W	PORT_MIRROR_MODE[1:0] Select a mirror mode to monitor 2’b00: mirror one port of RX (default) 2’b01: mirror one port of TX 2’b10: mirror source-destination pair (port of TX and RX must be the different) 2’b11: mirror one port of TX and RX (port of TX and RX must be the same)	2’b00
	20[12:6]		RESERVED	
	20[5:0]	R/W	SEL_RX_PORT_MIRROR[5:0] Select the source (receive) port to be mirrored 6’b00_0000: reserved (default) 6’b00_0001: port 0 6’b00_0010: port 1 6’b00_0100: port 2 6’b00_1000: port 3 6’b01_0000: port 4 6’b10_0000: port 5 (MII0) other: reserved	6’h00
	21[15]		RESERVED	

PHY	MII	R/W	Description	Default
	21[14:12]	R/W	SEL_MIRROR_PORT[2:0] Select a mirror port to monitor any other port 3'b000: port 0 3'b001: port 1 3'b010: port 2 3'b011: port 3 3'b100: port 4 3'b101: port 5 (MII0)(default) other: reserved	3'b101
	21[11:6]		RESERVED	
	21[5:0]	R/W	SEL_TX_PORT_MIRROR[5:0] Select the destination (transmit) port to be mirrored 6'b00_0000: reserved (default) 6'b00_0001: port 0 6'b00_0010: port 1 6'b00_0100: port 2 6'b00_1000: port 3 6'b01_0000: port 4 other: reserved	6'h00

PHY	MII	R/W	Description	Default
20	22[15:7]		RESERVED	
	22[6]	R/W	SBP_EN Source Block Protection Enable	1'b0
	22[5:0]	R (SC)	SBP_STATUS[5:0] Source Block Protection Status Bit[0]: port 0 Bit[1]: port 1 Bit[2]: port 2 Bit[3]: port 3 Bit[4]: port 4 Bit[5]: port 5 Self-clear after read	6'h00
20	24[2:0]	R/W	Reserved.	
21	1[15:0]	RO	Reserved	
21	2[15:0]	RO	Reserved	
21	3[15:0]	R/W	Reserved	
21	3[4:0]	R/W	Reserved	
21	4[2:0]	R/W	Reserved	
21	5[15:11]		RESERVED	
	5[10]	R/W	FAST_LEAVE	1'b1
	5[9]	R/W	MG_INCLUDE_RP Multicast group include router port	1'b0
	5[8]	R/W	FLOOD_UNIGMP Flood Unknown IGMP Unknown IGMP is not one of following: 1. General Query 2. Group-Specific Query 3. IGMP Report 4. IGMP Leave	1'b0
	5[7]	R/W	FLOOD_IPM_CTRL Flood IP Multicast Control Packet Note – IP multicast control packet: DMAC=01-00-5e-xx-xx-xx, DIP= 224.0.0.x and non-IGMP	1'b0
	5[6:5]	R/W	UNIPM_MODE[1:0] Unknown IP Multicast Data Mode 2'b00 : discard 2'b01 : forward to CPU 2'b10 : flood packet 2'b11 : forward to router port Note – IP multicast data packet: DMAC=01-00-5e-xx-xx-xx and DIP=outside 224.0.0.x	2'b11
	5[4]	R/W	DISCARD_LEAVE Discard IGMP leave message	1'b0
	5[3]	R/W	FLOOD_RPT Flood report message to other ports 0:Disabled 1:Enabled	1'b0

PHY	MII	R/W	Description	Default
	5[2]	R/W	LRP_NULL_SIP Learn router port even if source IP address is 0.0.0.0 0:Disable 1:Enable It is valid only if LEARN_RP is enabled	1'b0
	5[1]	R/W	LEARN_RP Learn Router Port 0: Disable (default) 1: Enable	0
	5[0]	R/W	HW_IGMP_EN Hardware IGMP Enable 0:Disable (default) 1:Enable	0
21	6[15:8]	R/W	ROUTER_TIMEOUT_VLE[7:0] Router Timeout Value Router Timeout = ROUTER_TIMEOUT_UNIT * ROUTER_TIMEOUT_VLE	8'h00
	6[7:6]	R/W	ROUTER_TIMEOUT_UNIT[1:0] 2'b00: 1 second 2'b01: 2 second 2'b10: 4 second 2'b11: 8 second	2'b00
	6[5:0]	R/W	Reserved	6'b000000
21	7[15:8]	R/W	IGMP_TIMEOUT_VLE[7:0] IGMP Timeout Value IGMP Timeout = IGMP_TIMEOUT_UNIT * IGMP_TIMEOUT_VLE	8'h00
	7[1:0]	R/W	IGMP_TIMEOUT_UNIT[1:0] IGMP Timeout Unit 2'b00: 1 second 2'b01: 2 second 2'b10: 4 second 2'b11: 8 second	2'b00

PHY	MII	R/W	Description	Default
21	8[7:0]	R/W	BW_TI[7:0] Rate control time interval. Only used by egress port and output queue unit : millisecond	8'h01
	9[15:0]	R/W	BW_MBS[15:0] Rate control Maximum Burst Size Expressed in byte.	16'h 0000
	10[15:0]	R/W	BW_CREDIT_SIZE[15:0] Credit size to accumulate the bucket in per time interval. Expressed in byte.	16'h 0000
21	12[2:0]	R/W	BW_PORT[2:0] Port number for setting bandwidth rate.	3'h0
	12[3]	R/W	BW_IOE Bandwidth rate setting is on ingress or egress port 0: ingress port (default) 1: egress port	1'b0
	12[5:4]	R/W	BW_QUEUE[1:0] Assign the egress output queue number for setting rate control value 2'b00:egress port (default) 2'b01:queue 1 2'b10:queue 2 2'b11:queue 3	2'b00
	12[8]	R/W	BW_RW Rate control data read/write signal 0: read rate control data (default) 1: write rate control data	1'b0
	12[9]	R/W (SC)	BW_RW_START Indicates start read/write rate control data of a port, when write a logical "1" to this register. A self cleared register after read/write data done.	1'b0
21	14[15]	R/W (SC)	START/DONE To initiate a read or write command when set as 1. Self-cleared after read or write command is finished 1: start access the address table 0: access operation is completed	1'b0
	14[14]		RESERVED	1'b0
	14[13]	RO	DATA_VALID Data Valid the PHY part will set this bit to1 to indicate the data is available in "Data Buffer Register" for read operation	1'b0
	14[12:11]	R/W	COMMAND[1:0] Address Table Command 2'b00: reserved 2'b01: single write 2'b10: single read 2'b11: reserved	2'b00
	14[10:0]	R/W	INDEX The index selects one of address table entries.	11'h000
21	15[15:0]	R/W	MAC_ADDR[15:0]	16'h0000
	16[15:0]	R/W	MAC_ADDR[31:16]	16'h0000

PHY	MII	R/W	Description	Default
	17[15:0]	R/W	MAC_ADDR[47:32]	16'h0000
	18[15:14]	R/W	FILTER_INFO	2'b00
	18[13:10]	R/W	PRI_INFO	4'h0
	18[9:6]	R/W	Field ID(FID)	4'h0
	18[5:3]	R/W	PORT_ID Note: If PORT_ID set to all zero, frame's DMAC matched this entry is discarded.	3'b000
	18[2:0]	R/W	AGE Note: Entry is aged out or invalid if this field is all zero.	3'b000
	19[15:2]		RESERVED	
	19[1]	R/W	STATIC Entry is static and can not be aged out.	1'b0
	19[0]	R/W	RESERVED	
21	15[15:0]	R/W	MAC_ADDR[15:0]	16'h0000
	16[15:0]	R/W	MAC_ADDR[31:16]	16'h0000
	17[15:0]	R/W	MAC_ADDR[47:32]	16'h0000
	18[15:14]	R/W	FILTER_INFO	2'b00
	18[13:10]	R/W	PRI_INFO	4'h0
	18[9:6]	R/W	Field ID(FID)	4'h0
	18[5:0]	R/W	PORT_MAP Note –If PORT_MAP set to all zero, frame's DMAC matched this entry is discarded.	6'h0
	19[15:2]		RESERVED	
	19[1]	R/W	VALID Entry is valid.	1'b0
	19[0]	R/W	IGMP This bit shall set to 0.	1'b0
21	15[15:0]	R/W	MAC_ADDR[15:0]	16'h0000
	16[15:14]	R/W	TIMEOUT_P2[1:0]	2'b00
	16[13:11]	R/W	TIMEOUT_P1[2:0]	3'b000
	16[10:8]	R/W	TIMEOUT_P0[2:0]	3'b000
	16[7]	R/W	MAC_ADDR[23] This bit shall be set to 0.	1'b0
	16[6:0]	R/W	MAC_ADDR[22:16]	7'h0
	17[15:10]		RESERVED	
	17[9:7]	R/W	TIMEOUT_P5[2:0]	3'b000
	17[6:4]	R/W	TIMEOUT_P4[2:0]	3'b000
	17[3:1]	R/W	TIMEOUT_P3[2:0]	3'b000
	17[0]	R/W	TIMEOUT_P2[2]	1'b0
	18[15:14]	R/W	FILTER_INFO	2'b00
	18[13:10]	R/W	PRI_INFO	4'h0
	18[9:6]	R/W	Field ID(FID)	4'h0
	18[5:0]	R/W	PORT_MAP Note – If PORT_MAP set to all zero, frame's DMAC matched this entry is discarded.	6'h0
	19[15:2]		RESERVED	
	19[1]	R/W	VALID Entry is valid.	1'b0
	19[0]	R/W	IGMP This bit shall set to 1.	1'b1

PHY	MII	R/W	Description	Default
21	20[15]	R/W	INIT_HIGH Interrupt signal is active high. 1: active high 0: active low	1'b0
21	20[7]	R/W	VLAN_VIO_INT_EN Enable VLAN violation interrupt	1'b0
	20[6]	R/W	AT_UNICAST_VIO_INT_EN Enable address table violation interrupt for unicast frame	1'b0
	20[5]	R/W	AT_MULTICAST_VIO_INT_EN Enable address table violation interrupt for multicast frame	1'b0
	20[4]	R/W	AT_IGMP_VIO_INT_EN Enable address table violation interrupt for IP multicast frame	1'b0
	20[3]	R/W	SEC_VIO_INT_EN Enable security violation interrupt	1'b0
	20[2]	R/W	LEARN_VIO_INT_EN Enable learning violation interrupt	1'b0
	20[1]	R/W	SBP_INT_EN Enable source blocking protection interrupt	1'b0
	20[0]	R/W	MF_CNT_OF_INT_EN Enable Multi-Field counter overflow interrupt	1'b0
21	21[7]	RO (SC)	VLAN_VIO_INT Violates the VLAN rule interrupt	1'b0
	21[6]	RO (SC)	AT_UNICAST_VIO_INT Address table violation interrupt for unicast frame	1'b0
	21[5]	RO (SC)	AT_MULTICAST_VIO_INT Address table violation interrupt for multicast frame	1'b0
	21[4]	RO (SC)	AT_IGMP_VIO_INT Address table violation interrupt for IP multicast frame	1'b0
	21[3]	RO (SC)	SEC_VIO_INT Security violation interrupt	1'b0
	21[2]	RO (SC)	LEARN_VIO_INT Learning violation interrupt	1'b0
	21[1]	RO (SC)	SBP_INT Source blocking protection interrupt	1'b0
	21[0]	RO (SC)	MF_CNT_OF_INT Multi-Field counter overflow interrupt	1'b0
21	22[15]	R/W	MDIX_FORCE 1: enable (default), 0: disable	1'b1
	22[14]	R/W	REDUCE_IPG This function reduce the IPG by random from 0~20 PPM 1: enable 0: disable Default Value Pin 113 MII2_EN=1 / Pin 113 MII2_EN=0 0 / Pin 97(1)	*
	22[13]	R/W	TWOPARTD Reset the inter-frame-gap counter to zero, if the CRS signal asserted during the two third of IPG period. 1: enable 0 disable	1'b1

PHY	MII	R/W	Description	Default
	22[12]	R/W	HP_DIS_FLOW_EN High priority packet to disable flow control 1: a port will disable its flow control function for 2 sec if it receives a high priority packet. 0: the function is disabled	1'b0
	22[11:10]	R/W	DRIVE[1:0] Pad driving capability selection 00: 4 mA 01: 8 mA 10: 12 mA 11: 16 mA	2'b01
	22[9:8]	R/W	PS_MODE Power saving mode	2'b00
	22[3]	R/W	LINK_Q_EN,LINK quality enable 1:enable (default) 0:disable	pin_101(1)
	22[2]	R/W	Reserved	1'b0
	22[1]	R/W	STAG_TX_EN Special tagging for TX enable 1: enable 0: disable	1'b0
	22[0]	R/W	STAG_RX_EN Special tagging for RX enable 1: enable 0: disable	1'b0

PHY	MII	R/W	Description	Default
21	25[15:8]		RESERVED	
	25 [7:0]	RO (SC)	CRC_COUNTER[7:0] CRC counter which accumulates the CRC number of all ports. Any port received a frame with CRC error will increase this counter by 1. Self-clear after read.	8'h00
22	0[15]	R/W (SC)	VLAN_TABLE_CLR Clear the contents of VLAN TABLE register 1: clear register 0: do nothing (default) Self-clear after set and register cleared	1'b0
	0[14]		RESERVED	
	0[13:12]	R/W	UNVID_MODE[1:0] Unknown-VID Mode 2'b00 : discard 2'b01 : forward to CPU 2'b10 : flood packet 2'b11 : reserved	2'b00

PHY	MII	R/W	Description	Default
	0[11:6]	R/W	VLAN_CLS[5:0] VLAN Classification associated with each port Only active at tagged-based VLAN 0 : use VID to classify VLAN -use VID to search VLAN table if tag packet -use PVID to search VLAN table if untag packet 1 : use PVID to classify VLAN -always use PVID to search VLAN table	6'h00
	0[5:0]	R/W	VLAN_MODE[5:0] VLAN Mode setting associated with each port 0 : Port-based VLAN (default) 1 : Tagged-based VLAN	6'h00
22	1[15:12]		RESERVED	
	1[11]	R/W	VLAN_DROP_CFI Drop incoming frame, if the CFI field is not equal to zero.	1'b0
	1[10:8]	R/W	RSVD_VID[2:0] Reserved VID Bit 0: The null VID. If set, frames with null VID (priority-tagged frame) treat as untagged frames. 0: disable (default) 1: enable Bit 1: VID=1 (default VID) Replace default VID with PVID 0: disable (default) 1: enable Bit 2: VID=FFF Discard frame if the VID is the value FFF 0: disable 1: enable (default)	3'b100
	1[7:6]	R/W	ACCEPTABLE_FRM_TYPE[1:0] Acceptable Frame Type 2'b00 Admit all frames (default) 2'b01 Admit VLAN-tagged frames 2'b10 Admit Untagged frames 2'b11 Reserved	2'b00
	1[5:0]	R/W	VLAN_INGRESS_FILTER[5:0] VLAN Ingress Filter associated with each port If ingress filter for a given port is set, frame shall discard on that port whose VLAN classification does not include that port in it member set.	6'h3F
22	2[15:12]		RESERVED	
	2[11:6]	R/W	IGMP_IGNORE_MEMBER[5:0] IGMP Ignore member set Ignore member set for frame with DMAC inside 01-00-5e-xx-xx-xx	6'b000000
	2[5:0]	R/W	KEEP_TAG[5:0] Keep VLAN Tag Header 0: Disabled 1: Keep VLAN tag header from frame. If frames transmission on a egress port tags frame, the frame may contain two tag headers	6'h00
22	3[15:0]	R/W	TPID_VALUE[15:0]	16'h8100

PHY	MII	R/W	Description	Default
			802.1Q Tag Protocol Type	
22	4[15:0]	R/W	VLAN_INFO_0. Port 0 default VLAN information value	16'h0001
	5[15:0]	R/W	VLAN_INFO_1. Port 1 default VLAN information value	16'h0001
	6[15:0]	R/W	VLAN_INFO_2. Port 2 default VLAN information value	16'h0001
	7[15:0]	R/W	VLAN_INFO_3. Port 3 default VLAN information value	16'h0001
	8[15:0]	R/W	VLAN_INFO_4. Port 4 default VALN information value	16'h0001
	9[15:0]	R/W	VLAN_INFO_5. Port 5 default VALN information value	16'h0001
22	10[15:0]	R/W	VLAN_VALID[15:0] VALN filter is valid. The VALN filter entry X is valid associated with the VID_X.	16'h 0000
	11[15:0]	R/W	QU_NUM_EN[15:0] Assign new queue number enable Assign a new queue number which defined in PRI_NUM_X register associated with the VID_X.	16'h0000
	12[15:0]	R/W	STP_IDX_EN[15:0] Spanning Tree Protocol Index Enable	16'h0000
	13[15:0]	R/W	REW_VLAN_PRI_EN[15:0] Re-write VLAN priority field Enable	16'h0000
22	14[15:12]	R/W	FID_0[3:0] VLAN field identifier associated with VALN 0.	4'h0
	14[11:0]	R/W	VID_0[11:0] VLAN identifier associated with VALN 0.	12'h001
	15[15:12]	R/W	FID_1[3:0] VLAN field identifier associated with VALN 1.	4'h0
	15[11:0]	R/W	VID_1[11:0] VLAN identifier associated with VALN 1.	12'h002
	16[15:12]	R/W	FID_2[3:0] VLAN field identifier associated with VALN 2.	4'h0
	16[11:0]	R/W	VID_2[11:0] VLAN identifier associated with VALN 2.	12'h003
	17[15:12]	R/W	FID_3[3:0] VLAN field identifier associated with VALN 3.	4'h0
	17[11:0]	R/W	VID_3[11:0] VLAN identifier associated with VALN 3.	12'h004
	18[15:12]	R/W	FID_4[3:0] VLAN field identifier associated with VALN 4.	4'h0
	18[11:0]	R/W	VID_4[11:0] VLAN identifier associated with VALN 4.	12'h005
	19[15:12]	R/W	FID_5[3:0] VLAN field identifier associated with VALN 5.	4'h0
	19[11:0]	R/W	VID_5[11:0] VLAN identifier associated with VALN 5.	12'h006
	20[15:12]	R/W	FID_6[3:0] VLAN field identifier associated with VALN 6.	4'h0

PHY	MII	R/W	Description	Default
	20[11:0]	R/W	VID_6[11:0] VLAN identifier associated with VALN 6.	12'h007
	21[15:12]	R/W	FID_7[3:0] VLAN field identifier associated with VALN 7.	4'h0
	21[11:0]	R/W	VID_7[11:0] VLAN identifier associated with VALN 7.	12'h008
	22[15:12]	R/W	FID_8[3:0] VLAN field identifier associated with VALN 8.	4'h0
	22[11:0]	R/W	VID_8[11:0] VLAN identifier associated with VALN 8.	12'h009
	23[15:12]	R/W	FID_9[3:0] VLAN field identifier associated with VALN 9.	4'h0
	2311:0]	R/W	VID_9[11:0] VLAN identifier associated with VALN 9.	12'h00A
22	24[15:12]	R/W	FID_A[3:0] VLAN field identifier associated with VALN A.	4'h0
	24[11:0]	R/W	VID_A[11:0] VLAN identifier associated with VALN A.	12'h00B
	25[15:12]	R/W	FID_B[3:0] VLAN field identifier associated with VALN B.	4'h0
	25[11:0]	R/W	VID_B[11:0] VLAN identifier associated with VALN B.	12'h00C
	26[15:12]	R/W	FID_C[3:0] VLAN field identifier associated with VALN C.	4'h0
	26[11:0]	R/W	VID_C[11:0] VLAN identifier associated with VALN C.	12'h00D
	27[15:12]	R/W	FID_D[3:0] VLAN field identifier associated with VALN D.	4'h0
	27[11:0]	R/W	VID_D[11:0] VLAN identifier associated with VALN D.	12'h00E
	28[15:12]	R/W	FID_E[3:0] VLAN field identifier associated with VALN E.	4'h0
	28[11:0]	R/W	VID_E[11:0] VLAN identifier associated with VALN E.	12'h00F
	29[15:12]	R/W	FID_F[3:0] VLAN field identifier associated with VALN F.	4'h0
	29[11:0]	R/W	VID_F[11:0] VLAN identifier associated with VALN F.	12'h010
23	0[5:0]	R/W	VLAN_MEMBER_0[5:0] VLAN member port VLAN member port associated with the VID_0.	6'h3F
	0[13:8]	R/W	VLAN_MEMBER_1[5:0] VLAN member port VLAN member port associated with the VID_1.	6'h3F
	1[5:0]	R/W	VLAN_MEMBER_2[5:0] VLAN member port VLAN member port associated with the VID_2.	6'h3F
	1[13:8]	R/W	VLAN_MEMBER_3[5:0] VLAN member port VLAN member port associated with the VID_3.	6'h3F

PHY	MII	R/W	Description	Default
	2[5:0]	R/W	VLAN_MEMBER_4[5:0] VLAN member port VLAN member port associated with the VID_4.	6'h3F
	2[13:8]	R/W	VLAN_MEMBER_5[5:0] VLAN member port VLAN member port associated with the VID_5.	6'h3F
23	3[5:0]	R/W	VLAN_MEMBER_6[5:0] VLAN member port VLAN member port associated with the VID_6.	6'h00
	3[13:8]	R/W	VLAN_MEMBER_7[5:0] VLAN member port VLAN member port associated with the VID_7.	6'h00
	4[5:0]	R/W	VLAN_MEMBER_8[5:0] VLAN member port VLAN member port associated with the VID_8.	6'h00
	4[13:8]	R/W	VLAN_MEMBER_9[5:0] VLAN member port VLAN member port associated with the VID_9.	6'h00
	5[5:0]	R/W	VLAN_MEMBER_A[5:0] VLAN member port VLAN member port associated with the VID_A.	6'h00
	5[13:8]	R/W	VLAN_MEMBER_B[5:0] VLAN member port VLAN member port associated with the VID_B.	6'h00
	6[5:0]	R/W	VLAN_MEMBER_C[5:0] VLAN member port VLAN member port associated with the VID_C.	6'h00
	6[13:8]	R/W	VLAN_MEMBER_D[5:0] VLAN member port VLAN member port associated with the VID_D.	6'h00
	7[5:0]	R/W	VLAN_MEMBER_E[5:0] VLAN member port VLAN member port associated with the VID_E.	6'h00
	7[13:8]	R/W	VLAN_MEMBER_F[5:0] VLAN member port VLAN member port associated with the VID_F.	6'h00
23	8[5:0]	R/W	ADD_TAG_0[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_0.	6'b 000000
			Bit 0: 1: port 0 adds a VLAN tag to each outgoing packet. 0: port 0 doesn't add a VLAN tag.	
			Bit 1: 1: port 1 adds a VLAN tag to each outgoing packet. 0: port 1 doesn't add a VLAN tag.	
			Bit 2: 1: port 2 adds a VLAN tag to each outgoing packet. 0: port 2 doesn't add a VLAN tag.	
			Bit 3: 1: port 3 adds a VLAN tag to each outgoing packet. 0: port 3 doesn't add a VLAN tag.	
			Bit 4: 1: port 4 adds a VLAN tag to each outgoing packet. 0: port 4 doesn't add a VLAN tag.	

PHY	MII	R/W	Description		Default
			Bit 5	1: port 5 adds a VLAN tag to each outgoing packet. 0: port 5 doesn't add a VLAN tag.	
23	8[13:8]	R/W	ADD_TAG_1[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_1.		6'b 000000
	9[5:0]	R/W	ADD_TAG_2[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_2.		6'b 000000
	9[13:8]	R/W	ADD_TAG_3[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_3.		6'b 000000
	10[5:0]	R/W	ADD_TAG_4[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_4.		6'b 000000
	10[13:8]	R/W	ADD_TAG_5[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_5.		6'b 000000
	11[5:0]	R/W	ADD_TAG_6[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_6.		6'b 000000
	11[13:8]	R/W	ADD_TAG_7[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_7.		6'b 000000
	12[5:0]	R/W	ADD_TAG_8[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_8.		6'b 000000
	12[13:8]	R/W	ADD_TAG_9[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_9.		6'b 000000
	13[5:0]	R/W	ADD_TAG_A[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_A.		6'b 000000
	13[13:8]	R/W	ADD_TAG_B[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_B.		6'b 000000
23	14[5:0]	R/W	ADD_TAG_C[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_C.		6'b 000000

PHY	MII	R/W	Description	Default
	14[13:8]	R/W	ADD_TAG_D[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_D.	6'b 000000
	15[5:0]	R/W	ADD_TAG_E[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_E.	6'b 000000
	15[13:8]	R/W	ADD_TAG_F[5:0] Add VLAN tag Port Y adds a VLAN tag defined in VLAN_TAG_Y to each outgoing packet associated with the VID_F.	6'b 000000
23	16[5:0]	R/W	REMOVE_TAG_0[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_0.	6'b 000000
			Bit 0: 1: port 0 removes the VLAN tag of each outgoing packet. 0: port 0 doesn't remove the VLAN tag of each outgoing packet.	
			Bit 1: 1: port 1 removes the VLAN tag of each outgoing packet. 0: port 1 doesn't remove the VLAN tag of each outgoing packet.	
			Bit 2: 1: port 2 removes the VLAN tag of each outgoing packet. 0: port 2 doesn't remove the VLAN tag of each outgoing packet.	
			Bit 3: 1: port 3 removes the VLAN tag of each outgoing packet. 0: port 3 doesn't remove the VLAN tag of each outgoing packet.	
			Bit 4: 1: port 4 removes the VLAN tag of each outgoing packet. 0: port 4 doesn't remove the VLAN tag of each outgoing packet.	
			Bit 5: 1: port 5 removes the VLAN tag of each outgoing packet. 0: port 5 doesn't remove the VLAN tag of each outgoing packet.	
	16[13:8]	R/W	REMOVE_TAG_1[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_1.	6'b 000000
	17[5:0]	R/W	REMOVE_TAG_2[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_2.	6'b 000000
	17[13:8]	R/W	REMOVE_TAG_3[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_3.	6'b 000000
	18[5:0]	R/W	REMOVE_TAG_4[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_4.	6'b 000000
	18[13:8]	R/W	REMOVE_TAG_5[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_5.	6'b 000000
	19[5:0]	R/W	REMOVE_TAG_6[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_6.	6'b 000000

PHY	MII	R/W	Description	Default
	19[13:8]	R/W	REMOVE_TAG_7[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_7.	6'b 000000
	20[5:0]	R/W	REMOVE_TAG_8[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_8.	6'b 000000
	20[13:8]	R/W	REMOVE_TAG_9[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_9.	6'b 000000
	21[5:0]	R/W	REMOVE_TAG_A[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_A.	6'b 000000
	21[13:8]	R/W	REMOVE_TAG_B[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_B.	6'b 000000
	22[5:0]	R/W	REMOVE_TAG_C[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_C.	6'b 000000
	22[13:8]	R/W	REMOVE_TAG_D[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_D.	6'b 000000
	23[5:0]	R/W	REMOVE_TAG_E[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_E.	6'b 000000
	23[13:8]	R/W	REMOVE_TAG_F[5:0] Remove VLAN tag Port Y removes VLAN tag to each outgoing packet associated with the VID_F.	6'b 000000
23	24[7:0]	R/W	VLAN_MISC_0[7:0] VLAN Miscellaneous Registers 0	8'h00
			Bit 1-0: STP_IDX[1:0] Spanning Tree Index This registers is effective only STP_IDX_EN[0] is enabled	
			Bit 3-2: QU_NUM[1:0] Priority Queue Number This registers is effective only QU_NUM_EN[0] is enabled	
			Bit 4: LEARN_DIS Learning Disable	
			Bit 7-5: REW_VLAN_PRI[2:0] Rewrite VLAN priority value This registers is effective only REW_VLAN_PRI_EN[0] is enabled	
	24[15:8]	R/W	VLAN_MISC_1[7:0] VLAN Miscellaneous Registers 1	8'h00

PHY	MII	R/W	Description	Default
	25[7:0]	R/W	VLAN_MISC_2[7:0] VLAN Miscellaneous Registers 2	8'h00
	25[15:8]	R/W	VLAN_MISC_3[7:0] VLAN Miscellaneous Registers 3	8'h00
	26[7:0]	R/W	VLAN_MISC_4[7:0] VLAN Miscellaneous Registers 4	8'h00
	26[15:8]	R/W	VLAN_MISC_5[7:0] VLAN Miscellaneous Registers 5	8'h00
	27[7:0]	R/W	VLAN_MISC_6[7:0] VLAN Miscellaneous Registers 6	8'h00
	27[15:8]	R/W	VLAN_MISC_7[7:0] VLAN Miscellaneous Registers 7	8'h00
	28[7:0]	R/W	VLAN_MISC_8[7:0] VLAN Miscellaneous Registers 8	8'h00
	28[15:8]	R/W	VLAN_MISC_9[7:0] VLAN Miscellaneous Registers 9	8'h00
	29[7:0]	R/W	VLAN_MISC_A[7:0] VLAN Miscellaneous Registers A	8'h00
	29[15:8]	R/W	VLAN_MISC_B[7:0] VLAN Miscellaneous Registers B	8'h00
	30[7:0]	R/W	VLAN_MISC_C[7:0] VLAN Miscellaneous Registers C	8'h00
23	30[15:8]	R/W	VLAN_MISC_D[7:0] VLAN Miscellaneous Registers D	8'h00
	31[7:0]	R/W	VLAN_MISC_E[7:0] VLAN Miscellaneous Registers E	8'h00
	31[15:8]	R/W	VLAN_MISC_F[7:0] VLAN Miscellaneous Registers F	8'h00
24	0[13:8]	R/W	STP_FORWARD_EN_0[5:0] Spanning Tree packet Forwarding capability for each port associate with STP_IDX	6'b111111
	0[5:0]	R/W	STP_LEARNING_EN_0[5:0] Spanning Tree packet Learning capability for each port associate with STP_IDX	6'b111111
	1[13:8]	R/W	STP_FORWARD_EN_1[5:0] Spanning Tree packet Forwarding capability for each port associate with STP_IDX	6'b111111
	1[5:0]	R/W	STP_LEARNING_EN_1[5:0] Spanning Tree packet Learning capability for each port associate with STP_IDX	6'b111111
	2[13:8]	R/W	STP_FORWARD_EN_2[5:0] Spanning Tree packet Forwarding capability for each port associate with STP_IDX	6'b111111
	2[5:0]	R/W	STP_LEARNING_EN_2[5:0] Spanning Tree packet Learning capability for each port associate with STP_IDX	6'b111111
	3[13:8]	R/W	STP_FORWARD_EN_3[5:0] Spanning Tree packet Forwarding capability for each port associate with STP_IDX	6'b111111

PHY	MII	R/W	Description	Default
	3[5:0]	R/W	STP_LEARNING_EN_3[5:0] Spanning Tree packet Learning capability for each port associate with STP_IDX	6'b111111
25	0[15]	R/W	LP_OVER_DSCP Logical port takes a high precedence than DSCP priority.	1'b0
	0[14]	R/W	TOS_OVER_VLAN_PRI IP frame take a higher precedence than VLAN priority. That is the IP frame's priority is over the frame with VLAN tagged.	1'b0
	0[12:8]	R/W	COS_EN[4:0] Class of service enable for each port 1: enable 0: disabled (default)	5'h00
	0[7]	R/W	USER_DEF_PRI User Define Priority	1'b0
	0[6]		RESERVED	
	0[5:0]	R/W	PORT_PRI_EN[5:0] Port based priority function enable control registers for each port.	6'h00
25	1[1:0]	R/W	P0_PRI[1:0] Port 0 port-based priority output queue number. 00: assign packets to queue 0 01: assign packets to queue 1 10: assign packets to queue 2 11: assign packets to queue 3 (default)	2'b11
	1[3:2]	R/W	P1_PRI[1:0] Port 1 port-based priority output queue number. 00: assign packets to queue 0 01: assign packets to queue 1 10: assign packets to queue 2 11: assign packets to queue 3 (default)	2'b11
	1[5:4]	R/W	P2_PRI[1:0] Port 2 port-based priority output queue number. 00: assign packets to queue 0 01: assign packets to queue 1 10: assign packets to queue 2 11: assign packets to queue 3 (default)	2'b11
	1[7:6]	R/W	P3_PRI[1:0] Port 3 port-based priority output queue number. 00: assign packets to queue 0 01: assign packets to queue 1 10: assign packets to queue 2 11: assign packets to queue 3 (default)	2'b11
25	1[9:8]	R/W	P4_PRI[1:0] Port 4 port-based priority output queue number. 00: assign packets to queue 0 01: assign packets to queue 1 10: assign packets to queue 2 11: assign packets to queue 3 (default)	2'b11

PHY	MII	R/W	Description	Default
	1[11:10]	R/W	P5_PRI[1:0] Port 0 port-based priority output queue number. 00: assign packets to queue 0 01: assign packets to queue 1 10: assign packets to queue 2 11: assign packets to queue 3 (default)	2'b11
25	2[15:14]	R/W	VLAN_PRI7 Priority map when the VLAN priority is 7	2'b00
	2[13:12]	R/W	VLAN_PRI6 Priority map when the VLAN priority is 6	2'b00
	2[11:10]	R/W	VLAN_PRI5 Priority map when the VLAN priority is 5	2'b00
	2[9:8]	R/W	VLAN_PRI4 Priority map when the VLAN priority is 4	2'b00
	2[7:6]	R/W	VLAN_PRI3 Priority map when the VLAN priority is 3	2'b00
	2[5:4]	R/W	VLAN_PRI2 Priority map when the VLAN priority is 2	2'b00
	2[3:2]	R/W	VLAN_PRI1 Priority map when the VLAN priority is 1	2'b00
	2[1:0]	R/W	VLAN_PRI0 Priority map when the VLAN priority is 0	2'b00
25	3[15:14]	R/W	DSCP_7 Priority map when the DSCP field is 7	2'b00
	3[13:12]	R/W	DSCP_6 Priority map when the DSCP field is 6	2'b00
	3[11:10]	R/W	DSCP_5 Priority map when the DSCP field is 5	2'b00
	3[9:8]	R/W	DSCP_4 Priority map when the DSCP field is 4	2'b00
	3[7:6]	R/W	DSCP_3 Priority map when the DSCP field is 3	2'b00
	3[5:4]	R/W	DSCP_2 Priority map when the DSCP field is 2	2'b00
	3[3:2]	R/W	DSCP_1 Priority map when the DSCP field is 1	2'b00
	3[1:0]	R/W	DSCP_0 (Best Effort) Priority map when the DSCP field is 0	2'b00
	4[15:14]	R/W	DSCP_F Priority map when the DSCP field is F	2'b00
	4[13:12]	R/W	DSCP_E (AF13) Priority map when the DSCP field is E	2'b00
	4[11:10]	R/W	DSCP_D Priority map when the DSCP field is D	2'b00
	4[9:8]	R/W	DSCP_C (AF12) Priority map when the DSCP field is C	2'b00
25	4[7:6]	R/W	DSCP_B Priority map when the DSCP field is B	2'b00
	4[5:4]	R/W	DSCP_A (AF11) Priority map when the DSCP field is A	2'b11

PHY	MII	R/W	Description	Default
	4[3:2]	R/W	DSCP_9 Priority map when the DSCP field is 9	2'b00
	4[1:0]	R/W	DSCP_8 (CS1) Priority map when the DSCP field is 8	2'b00
	5[15:14]	R/W	DSCP_17 Priority map when the DSCP field is 17	2'b00
	5[13:12]	R/W	DSCP_16 (AF23) Priority map when the DSCP field is 16	2'b00
	5[11:10]	R/W	DSCP_15 Priority map when the DSCP field is 15	2'b00
	5[9:8]	R/W	DSCP_14 (AF22) Priority map when the DSCP field is 14	2'b00
	5[7:6]	R/W	DSCP_13 Priority map when the DSCP field is 13	2'b00
	5[5:4]	R/W	DSCP_12 (AF21) Priority map when the DSCP field is 12	2'b11
	5[3:2]	R/W	DSCP_11 Priority map when the DSCP field is 11	2'b00
	5[1:0]	R/W	DSCP_10 (CS2) Priority map when the DSCP field is 10	2'b00
	6[15:14]	R/W	DSCP_1F Priority map when the DSCP field is 1F	2'b00
	6[13:12]	R/W	DSCP_1E (AF33) Priority map when the DSCP field is 1E	2'b00
	6[11:10]	R/W	DSCP_1D Priority map when the DSCP field is 1D	2'b00
	6[9:8]	R/W	DSCP_1C (AF32) Priority map when the DSCP field is 1C	2'b00
	6[7:6]	R/W	DSCP_1B Priority map when the DSCP field is 1B	2'b00
	6[5:4]	R/W	DSCP_1A (AF31) Priority map when the DSCP field is 1A	2'b11
	6[3:2]	R/W	DSCP_19 Priority map when the DSCP field is 19	2'b00
	6[1:0]	R/W	DSCP_18 (CS3) Priority map when the DSCP field is 18	2'b00
	7[15:14]	R/W	DSCP_27 Priority map when the DSCP field is 27	2'b00
	7[13:12]	R/W	DSCP_26 (AF43) Priority map when the DSCP field is 26	2'b00
	7[11:10]	R/W	DSCP_25 Priority map when the DSCP field is 25	2'b00
	7[9:8]	R/W	DSCP_24 (AF42) Priority map when the DSCP field is 24	2'b00
25	7[7:6]	R/W	DSCP_23 Priority map when the DSCP field is 23	2'b00
	7[5:4]	R/W	DSCP_22 (AF41) Priority map when the DSCP field is 22	2'b11
	7[3:2]	R/W	DSCP_21 Priority map when the DSCP field is 21	2'b00

PHY	MII	R/W	Description	Default
	7[1:0]	R/W	DSCP_20 (CS4) Priority map when the DSCP field is 20	2'b00
	8[15:14]	R/W	DSCP_2F Priority map when the DSCP field is 2F	2'b00
	8[13:12]	R/W	DSCP_2E (EF) Priority map when the DSCP field is 2E	2'b11
	8[11:10]	R/W	DSCP_2D Priority map when the DSCP field is 2D	2'b00
	8[9:8]	R/W	DSCP_2C Priority map when the DSCP field is 2C	2'b00
	8[7:6]	R/W	DSCP_2B Priority map when the DSCP field is 2B	2'b00
	8[5:4]	R/W	DSCP_2A Priority map when the DSCP field is 2A	2'b00
	8[3:2]	R/W	DSCP_29 Priority map when the DSCP field is 29	2'b00
	8[1:0]	R/W	DSCP_28 (CS5) Priority map when the DSCP field is 28	2'b00
	9[15:14]	R/W	DSCP_37 Priority map when the DSCP field is 37	2'b00
	9[13:12]	R/W	DSCP_36 Priority map when the DSCP field is 36	2'b00
	9[11:10]	R/W	DSCP_35 Priority map when the DSCP field is 35	2'b00
	9[9:8]	R/W	DSCP_34 Priority map when the DSCP field is 34	2'b00
	9[7:6]	R/W	DSCP_33 Priority map when the DSCP field is 33	2'b00
	9[5:4]	R/W	DSCP_32 Priority map when the DSCP field is 32	2'b00
	9[3:2]	R/W	DSCP_31 Priority map when the DSCP field is 31	2'b00
	9[1:0]	R/W	DSCP_30 (CS6) Priority map when the DSCP field is 30	2'b11
	10[15:14]	R/W	DSCP_3F Priority map when the DSCP field is 3F	2'b00
	10[13:12]	R/W	DSCP_3E Priority map when the DSCP field is 3E	2'b00
	10[11:10]	R/W	DSCP_3D Priority map when the DSCP field is 3D	2'b00
25	10[9:8]	R/W	DSCP_3C Priority map when the DSCP field is 3C	2'b00
	10[7:6]	R/W	DSCP_3B Priority map when the DSCP field is 3B	2'b00
	10[5:4]	R/W	DSCP_3A Priority map when the DSCP field is 3A	2'b00
	10[3:2]	R/W	DSCP_39 Priority map when the DSCP field is 39	2'b00
	10[1:0]	R/W	DSCP_38 (CS7) Priority map when the DSCP field is 38	2'b11

PHY	MII	R/W	Description	Default
25	11[15:8]		RESERVED	
	11[7:6]	R/W	LP_TYPE Logical Port Type 2'b00 – Logic port priority disable 2'b01 – Source logic port priority enable 2'b10 – Destination logic port priority enable 2'b11 – Source or destination logic port priority enable	2'b11
	11[5:4]	R/W	USERDEF_RANGE_EN[1:0] User defined logic port range enable. bit[1]: user define range 1 register enable bit[0]: user define range 0 register enable	2'b11
	11[3:0]	R/W	PREDEF_PORT_EN[3:0] Pre-defined logic port number enable. bit[3]: logic port 3 enable, port 6000 bit[2]: logic port 2 enable, port 3389 bit[1]: logic port 1 enable, port 443 bit[0]: logic port 0 enable, port 22	4'hF
	12[15:0]	R/W	PREDEF_PORT_0[15:0] Pre-defined logical port 0. The default value is SSH protocol.	16'd22
	13[15:0]	R/W	PREDEF_PORT_1[15:0] Pre-defined logical port 1. The default value is HTTPs protocol.	16'd443
	14[15:0]	R/W	PREDEF_PORT_2[15:0] Pre-defined logical port 2. The default value is RDP (Windows Remote Desktop Protocol) protocol.	16'd 3389
	15[15:0]	R/W	PREDEF_PORT_3[15:0] Pre-defined logical port 3. The default value is XWIN protocol.	16'd 6000
	16[15:0]	R/W	USERDEF_RANGE0_LOW User defined logic port range 0 low limit	16'd23
	17[15:0]	R/W	USERDEF_RANGE0_HIGH User defined logic port range 0 high limit The default value is TELNET protocol.	16'd23
	18[15:0]	R/W	USERDEF_RANGE1_LOW User defined logic port range 1 low limit	16'd 5800
25	19[15:0]	R/W	USERDEF_RANGE1_HIGH User defined logic port range 1 high limit The default value is VNC protocol.	16'd 5800
	20[15:12]		RESERVED	
	20[11:10]	R/W	USERDEF_RANGE_1Q[1:0] User defined logic port range 1 transmit priority queue mapping.	2'b10
	20[9:8]	R/W	USERDEF_RANGE_0Q[1:0] User defined logic port range 0 transmit priority queue mapping.	2'b10
	20[7:6]	R/W	PREDEF_PORT_3Q[1:0] Pre-defined port 3 transmit priority queue mapping.	2'b10
	20[5:4]	R/W	PREDEF_PORT_2Q[1:0] Pre-defined port 2 transmit priority queue mapping.	2'b10
	20[3:2]	R/W	PREDEF_PORT_1Q[1:0] Pre-defined port 1 transmit priority queue mapping.	2'b10

PHY	MII	R/W	Description	Default
	20[1:0]	R/W	PREDEF_PORT_0Q[1:0] Pre-defined port 0 transmit priority queue mapping.	2'b10
	21[15:6]		RESERVED	
	21[5:2]	R/W	PREDEF_PORT_DROP[3:0] Pre-defined logic port drop packet. Drop the incoming packets that match the TCP/UDP port number defined in PREDEF_PORT_0[15:0] to PREDEF_PORT_3[15:0]. Drop ability has the precedence over the frame classify priority. [0] drop packet port number matches PREDEF_PORT_0[15:0] [1] drop packet port number matches PREDEF_PORT_1[15:0] [2] drop packet port number matches PREDEF_PORT_2[15:0] [3] drop packet port number matches PREDEF_PORT_3[15:0]	4'h0
	21[1:0]	R/W	USERDEF_RANGE_DROP[1:0] User defined logic port drop packet. Drop the incoming packets that match the TCP/UDP port number defined in port range register. [0] USERDEF_RANGE0_LOW~ USERDEF_RANGE0_HIGH [1] USERDEF_RANGE1_LOW~ USERDEF_RANGE1_HIGH Drop ability has the precedence over the frame classify priority.	2'b00
25	22[13]	R/W	QOS_OVER_FC QoS over Flow Control	1'b0
	22[12]		RESERVED	
	22[11:10]	R/W	SCH_TYPE_5[1:0] Queue scheduling configuration of port 5. Q3 Q2 Q1 Q0 2'b00: WRR WRR WRR WRR 2'b01: WFQ WFQ WFQ WFQ(BE) 2'b10: SP WFQ WFQ BE 2'b11: SP SP SP SP WRR: Weight Round Robin WFQ: Weight Far Queuing BE: Best Effort SP: Strictly Priority	2'b00
	22[9:8]	R/W	SCH_TYPE_4[1:0] Queue scheduling configuration of port 4.	2'b00
	22[7:6]	R/W	SCH_TYPE_3[1:0] Queue scheduling configuration of port 3.	2'b00
	22[5:4]	R/W	SCH_TYPE_2[1:0] Queue scheduling configuration of port 2.	2'b00
	22[3:2]	R/W	SCH_TYPE_1[1:0] Queue scheduling configuration of port 1.	2'b00
	22[1:0]	R/W	SCH_TYPE_0[1:0] Queue scheduling configuration of port 0.	2'b00

PHY	MII	R/W	Description	Default
25	23[15:12]	R/W	Q3_WEIGHT Output queue 3 Weighted Round-Robin scheduling control registers 4'b1111: 15 packets 4'b1110: 14 packets …….. …….. 4'b0010: 2 packets 4'b0001: 1 packet 4'b0000: reserved	4'b1000
	23[11:8]	R/W	Q2_WEIGHT Output queue 2 Weighted Round-Robin scheduling control registers 4'b1111: 15 packets 4'b1110: 14 packets …….. …….. 4'b0010: 2 packets 4'b0001: 1 packet 4'b0000: reserved	4'b0100
25	23[7:4]	R/W	Q1_WEIGHT Output queue 1 Weighted Round-Robin scheduling control registers 4'b1111: 15 packets 4'b1110: 14 packets …….. …….. 4'b0010: 2 packets 4'b0001: 1 packet 4'b0000: reserved	4'b0010
	23[3:0]	R/W	Q0_WEIGHT Output queue 0 Weighted Round-Robin scheduling control registers 4'b1111: 15 packets 4'b1110: 14 packets …….. …….. 4'b0010: 2 packets 4'b0001: 1 packet 4'b0000: reserved	4'b0001

PHY	MII	R/W	Description	Default
26	0[15]	R/W	MF_QOS_EN Multi-Field QoS access control function enabled. When this bit is enabled, switch engine will use Multi-Field registers to classify the incoming frame.	1'b0
	0[10]	R/W (SC)	MF_REG_CLR Clear the contents of Multi-Field classification register and Multi-Filed table QOS rate control register. This bit is for programming convenience consideration. When set it will clear all the multi-field registers to zero, excepts for the IP mask registers – MF_IP_SA_MASK[3:0] & MF_IP_DA_MASK[3:0]. 1: clear registers 0: do nothing (default) A self-cleared register after set and registers cleared.	1'b0

PHY	MII	R/W	Description	Default
	0[9]	R/W (SC)	MF_CNT_RESET Multi-Field counter reset. When reset, it will reference the setting of MF_RESET_EN register. 1: enable 0: disable	1'b0
	0[8]	R/W (SC)	MF_ENTRY_RESET Multi-Field entry reset. When reset, it will reference the setting of MF_RESET_EN register. 1: enable 0: disable	1'b0
	0[7:0]	R/W	MF_RESET_EN[7:0] Multi-Filed reset enables for each entry or counter. 1: enable 0: disable	8'h00
26	1[15:14]	R/W	MF_CTRL[1:0] Multi-Field entry control registers bit[1]: Filtering/Forwarding - 0: Forward - 1: Filter bit[0]: Traffic Conditioning	2'b00
	1[12]	R/W	MF_IP_RANGE Enable the IP address range monitoring function. When enabled, the source and destination IP address register is used as an IP address range monitor register. MF_IM_SA will be a IP address monitor start number MF_IM_DA will be a IP address monitor stop number { MF_IM_DIP, MF_IM_SIP } Monitor type 00 reserved 01 source address 10 destination address 11 source or dest. addr	1'b0
	1[11]	R/W	MF_IM_SA_EN IP/MAC source address field enable.	1'b0
	1[10]	R/W	MF_IM_SIP IP/MAC source address field is used as an IP address.	1'b0
	1[9:6]	R/W	MF_IP_SA_MASK[3:0] IP source address subnet mask. The IP address can be grouped into four groups, each group contains eight bits and represented in decimal format (known as dotted decimal notation). This register is used as a mask to extract the IP address.	4'hF
	1[5]	R/W	MF_IM_DA_EN IP/MAC destination address field enable.	1'b0
	1[4]	R/W	MF_IM_DIP IP/MAC destination address field is used as an IP address.	1'b0
	1[3:0]	R/W	MF_IP_DA_MASK[3:0] IP destination address subnet mask.	4'hF

PHY	MII	R/W	Description	Default
	2[15:0] 3[15:0] 4[15:0]	R/W	MF_IM_SA[47:0] IP/MAC source address. When IP address is in using, only the 32-bits of LSB part will be referenced and ignore the rest. phy26.2= MF_IM_SA[15:0] phy26.3= MF_IM_SA[31:16] phy26.4= MF_IM_SA[47:32]	48'h0
	5[15:0] 6[15:0] 7[15:0]	R/W	MF_IM_DA[47:0] IP/MAC destination address. When IP address is in using, only the 32-bits of LSB part will be referenced and ignore the rest. phy26.5= MF_IM_DA[15:0] phy26.6= MF_IM_DA[31:16] phy26.7= MF_IM_DA[47:32]	48'h0
	8[15:0]	R/W	MF_ET_VALUE[15:0] EtherType value	16'h0000
	9[15]	R/W	MF_ET_EN EtherType field enable	1'b0
	9[14]		RESERVED	
	9[13:12]	R/W	MF_FW_CTRL[1:0] Forward or copy packet to specific port when Multi_Field entry hit 2'b00: Disable 2'b01: Forward to CPU 2'b10: Copy to mirror port 2'b11: Reserved	2'b00
	9[11:9]	R/W	MF_PRI_CTRL[2:0] Forward packet to specific queue when Multi_Field entry hit 3'b000: Disable 3'b100: Forward to queue 0 3'b101: Forward to queue 1 3'b110: Forward to queue 2 3'b111: Forward to queue 3 Other: Reserved	3'b000
	9[8]	R/W	MF_PTL_EN IP protocol number field enable.	1'b0
	9[7:0]	R/W	MF_PTL_NUM[7:0] IP protocol number field.	8'h00
	10[15:5]		RESERVED	

PHY	MII	R/W	Description	Default
	10[4]	R/W	MF_LG_RANGE Enable the TCP/UDP port range monitoring function. When enabled, the source and destination port register is used as a port range monitor register. MF_LG_SP_NUM will be a port monitor start number MF_LG_DP_NUM will be a port monitor stop number {MF_LG_DP_TYPE, MF_LG_SP_TYPE} Monitor type 00 reserved 01 TCP 10 UDP 11 TCP or UDP {MF_LG_DP_EN, MF_LG_SP_EN} Monitor type 00 reserved 01 source port 10 destination port 11 source or dest. port	1'b0
26	10 [3]	R/W	MF_LG_SP_EN TCP/UDP source port field enable.	1'b0
	10[2]	R/W	MF_LG_SP_TYPE Indicates the MF_LG_SP_NUM field is a TCP or UDP port. 0: TCP port 1: UDP port	1'b0
	10[1]	R/W	MF_LG_DP_EN TCP/UDP destination port field enable.	1'b0
	10[0]	R/W	MF_LG_DP_TYPE Indicates the MF_LG_DP_NUM field is a TCP or UDP port. 0: TCP port 1: UDP port	1'b0
	11[15:0]	R/W	MF_LG_SP_NUM[15:0] TCP/UDP source port number to be monitored.	16'h0
	12[15:0]	R/W	MF_LG_DP_NUM[15:0] TCP/UDP destination port number to be monitored.	16'h0
	13[15]	R/W	MF_SP_EN Physical source port field enable	1'b0
	13[14:10]	R/W	MF_SP_NUM[4:0] Physical source port number (port 0 ~ 4) bit[4]: port 4 bit[3]: port 3 bit[2]: port 2 bit[1]: port 1 bit[0]: port 0	5'h00
	13[9:0]		RESERVED	
	14[7]	R/W	MF_BA_EN Behavior Aggregate function enable	1'b0
	14[6]	R/W	MF_BA_TYPE Behavior Aggregate function type 0: DSCP (ipv4 TOS or ipv6 DSCP) 1: VLAN priority	1'b0

PHY	MII	R/W	Description	Default
	14[5:0]	R/W	MF_BA_VALUE[5:0] Behavior Aggregate value For DSCP, using whole 6-bits, but the upper 3-bit for VLAN priority reference.	6'h00
26	16[15:0]	R/W	MF_MBS[15:0] Maximum Burst Size Expressed in byte.	16'h 0000
	17[15:0]	R/W	MF_CREDIT_SIZE[15:0] Credit size to accumulate the bucket in per time interval. Expressed in byte.	16'h 0000
26	19[7:0]	R/W	MF_VALID[7:0] Multi-Field function valid for each entry.	8'h00
	20[2:0]	R/W	MF_ENTRY[2:0] Multi-Field entry number. 8-entry is used MF QoS function,	3'h0
	20[3]	R/W	MF_RW Multi-field data read/write signal 0: read Multi-Field data 1: write Multi-Field data	1'b0
	20[4]	R/W (SC)	MF_RW_START Indicates start read/write Multi-Field of an entry, when write a logical "1" to this register. A self cleared register after read/write data done.	1'b0
	20[5]	R/W	MF_OVERFLOW_THR MF counter overflow threshold index 1: 32'hFFFF_0000 0: 32'hFF00_0000	1'b0
	20[6]	R/W (SC)	MF_CNT_READ Indicates start read Multi-Field counter content of an entry, when write a logical "1" to this register. A self cleared register after read counter done.	1'b0
	21[15:0]	RO (SC)	MF_CNT_LSB[15:0] Multi-Field counter content after data read, LSB part.	16'h0000
	22[15:0]	RO (SC)	MF_CNT_MSB[31:16] Multi-Field counter content after data read, MSB part.	16'h0000
26	23[7:0]	RO (SC)	MF_OVERFLOW[7:0] Multi-Field counter overflow for each entry	8'h00

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Stresses exceed those values listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage	-0.3V to 4.0V
Input Voltage	-0.3V to 5.0V
Storage Temperature	-65℃ to 150℃
Ambient Operating Temperature (Ta)	0℃ to 70℃

6.2 DC Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	AVCC	1.85	1.95	2.05	V	
Supply Voltage	VCC_C	1.85	1.95	2.05	V	
Supply Voltage	VCC_IO	3.13	3.3	3.46	V	
Supply Voltage	VCC33	3.13	3.3	3.46	V	
Input low-to-high threshold	V_{IH}	2.05				
Input high-to-low threshold	V_{IL}			0.9		
Output Low Voltage	V_{OL}			0.4	V	IOH=4mA, VCC_O_x=3.3V
Output High Voltage	V_{OH}	0.7*VCC_IO			V	IOL=4mA, VCC_O_x=3.3V
Supply current	I_{AVCC}		15		mA	VCC=1.85V
Supply current	I_{VCC_C}		900		mA	VCC_C=1.85V
Supply current	I_{VCC_IO}		100		mA	VCC_IO=3.3V
X1 Input Low Voltage	V_{IL}			0.6	V	AVCC=1.85V
X1 Input High Voltage	V_{IH}	1.5			V	AVCC=1.85V
RESET_N Threshold Voltage	V_{rst}	0.4*VCC_IO		0.6*VCC_IO	V	
Fiber Rx common mode Voltage	V_{FRC}		0.6*AVCC		V	
Fiber Rx differential mode Voltage	V_{FRD}	0.4			V	
FXSD Input Voltage for Fiber mode	V_{FXSD}	1.2		VCC33	V	
FXSD Input Voltage for Fiber linkup		1.9		2.3	V	For 3.3V Fiber module
		3.4		3.8	V	For 5V Fiber module
FXSD Input Voltage for TP mode		0		0.5	V	

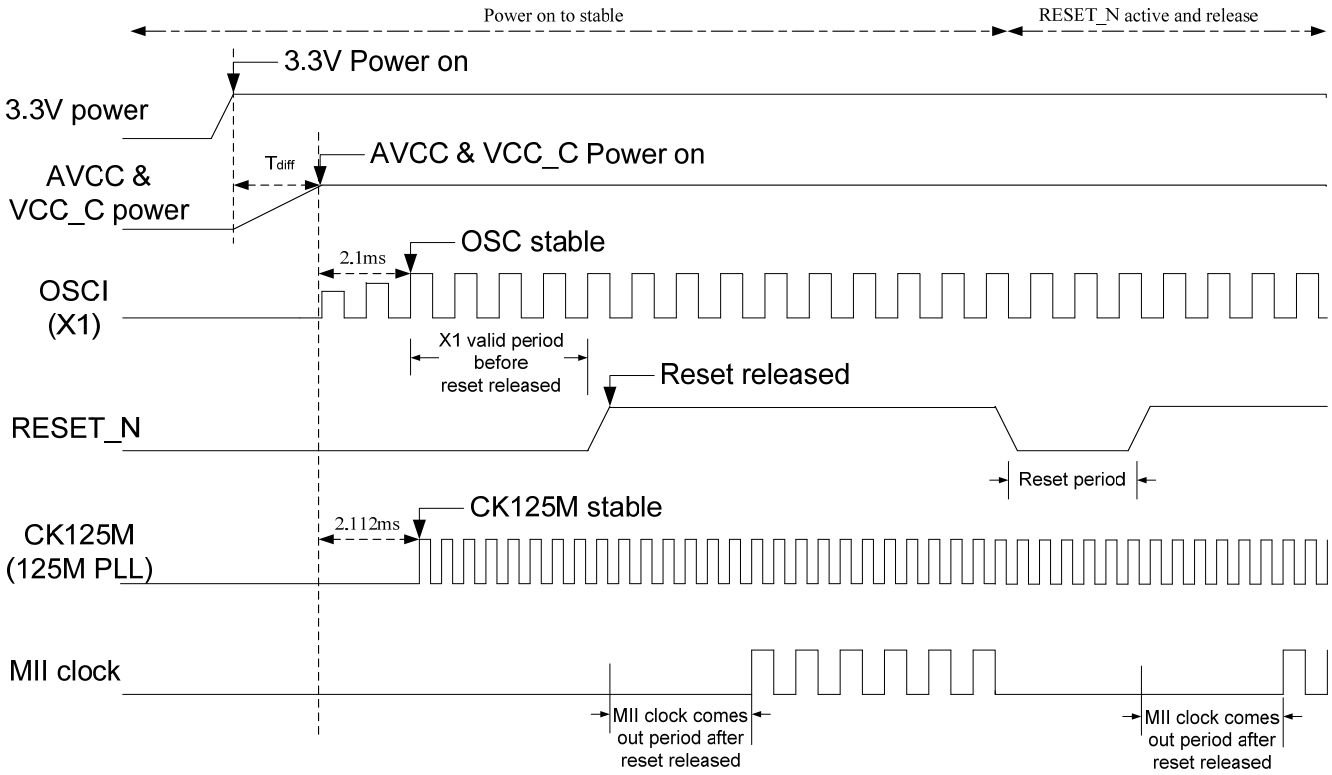
6.3 AC Characteristics

Input Clock

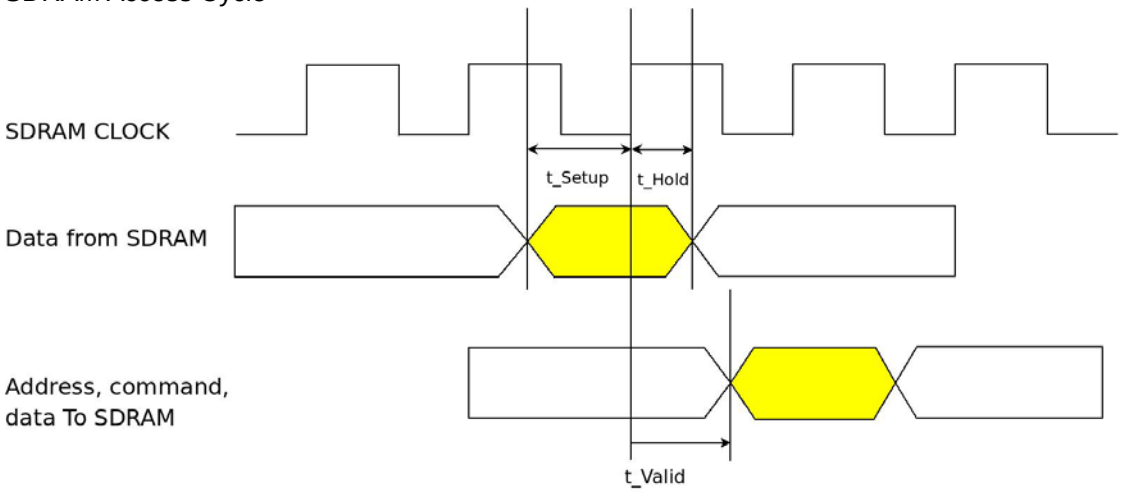
Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Frequency			25		MHz	
Frequency Tolerance		-50		+50	ppm	

Power On Sequence and Reset Timing

Description	Min.	Typ.	Max.	Unit
X1 valid period before reset released	10	-	-	ms
Reset period	10	-	-	ms
All power source ready before reset released	10			ms
Time difference between VCC3.3 and AVCC&VCC_C (Tdiff)	-2			ms
MII clock comes out period after reset released	-	1	-	µs



SDRAM Access Cycle



Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
RAM Clock Cycle			125/150		MHz	
Data input Setup time from SDRAM	t_Setup	1.5			ns	
Data input Hold time from SDRAM	t_Hold	1.5			ns	
Output valid (Address, command, data)	t_Valid	1.5		4.6	ns	

Note: All parameters are measured on the following condition: loading capacitor 6.5pf.

6.4 Thermal Parameters

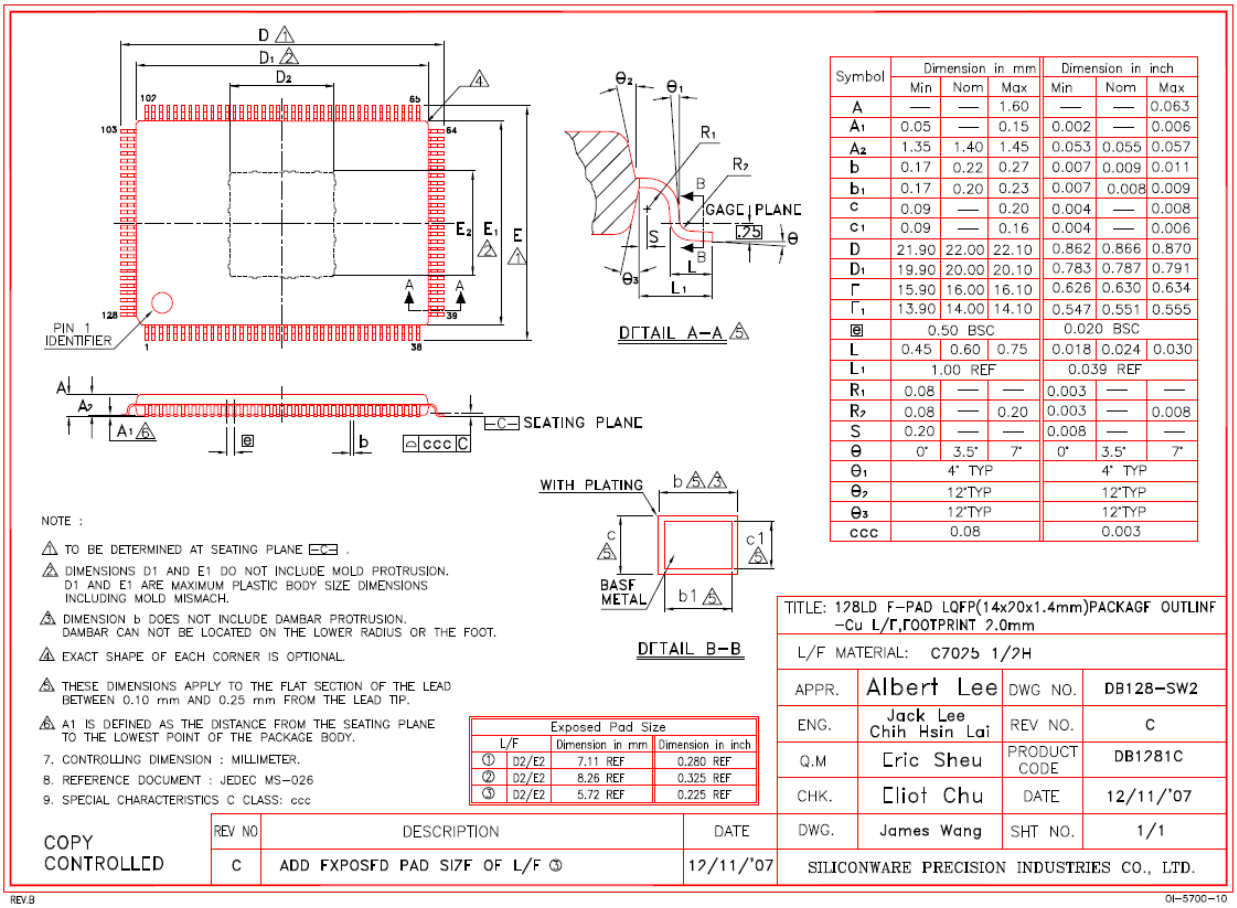
Theta Ja	Theta Jc	Conditions	Units
30.6	**24.3**	(1) 2 Layer PCB, (2) Air flow @ 0m/S. (3) PCB size: 3”X4.5”	°C/W
11.5	**10.9**	(1) 4 Layer PCB, (2) Air flow @ 0m/S (3) PCB size: 3”X4.5”	°C/W

7. Order Information

Part No.	Package	Notice
IP3210ALF	128-PIN LQFP	-

8. Package Detail

128 LQFP Outline Dimensions



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	21.90	22.00	22.10	0.862	0.866	0.870
D1	19.90	20.00	20.10	0.783	0.787	0.791
E	15.90	16.00	16.10	0.626	0.630	0.634
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	4° TYP			4° TYP		
θ2	12°TYP			12°TYP		
θ3	12°TYP			12°TYP		
ccc	0.08			0.003		

IC Plus Corp.

Headquarters
10F, No.47, Lane 2, Kwang-Fu Road, Sec. 2,
Hsin-Chu City, Taiwan 300, R.O.C.
TEL：886-3-575-0275 FAX：886-3-575-0475
Website: www.icplus.com.tw

Sales Office
4F, No. 106, Hsin-Tai-Wu Road, Sec.1,
Hsi-Chih, Taipei Hsien, Taiwan 221, R.O.C.
TEL：886-2-2696-1669 FAX：886-2-2696-2220