

CS8221

Micropower 5.0 V, 100 mA Low Dropout Linear Regulator

The CS8221 is a precision 5.0 V, 100 mA micropower voltage regulator with very low quiescent current (60 μ A typical at 100 μ A load). The 5.0 V output is accurate within $\pm 2.0\%$ and supplies 100 mA of load current with a maximum dropout voltage of only 600 mV.

The regulator is protected against reverse battery, short circuit, overvoltage, and over temperature conditions. The device can withstand 74 V peak transients making it suitable for use in automotive environments. The CS8221 is pin for pin compatible with the LM2931.

Features

- Low Quiescent Current (60 μ A @ 100 μ A Load)
- 5.0 V $\pm 2.0\%$ Output
- 100 mA Output Current Capability
- Internally Fused Leads in SO-8 Package
- Fault Protection
 - +74 V Peak Transient Voltage
 - -15 V Reverse Voltage
 - Short Circuit
 - Thermal Shutdown
- Pb-Free Package Is Available

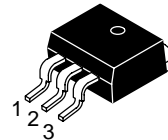


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<http://onsemi.com>

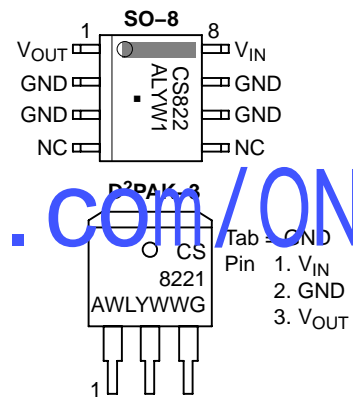


SO-8
DF SUFFIX
CASE 751



D²PAK-3
DP SUFFIX
CASE 418AB

PIN CONNECTIONS AND MARKING DIAGRAM



CS8221 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

ORDERING INFORMATION*

| Device | Package | Shipping† |
|--------------|----------------------|------------------|
| CS8221YDF8 | SO-8 | 95 Units/Rail |
| CS8221YDFR8 | SO-8 | 2500/Tape & Reel |
| CS8221YDFR8G | SO-8 (Pb-Free) | 2500/Tape & Reel |
| CS8221YDP3 | D ² PAK-3 | 50 Units/Rail |
| CS8221YDPR3 | D ² PAK-3 | 750/Tape & Reel |

*Contact your local sales representative for TO-92 package option.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

CS8221

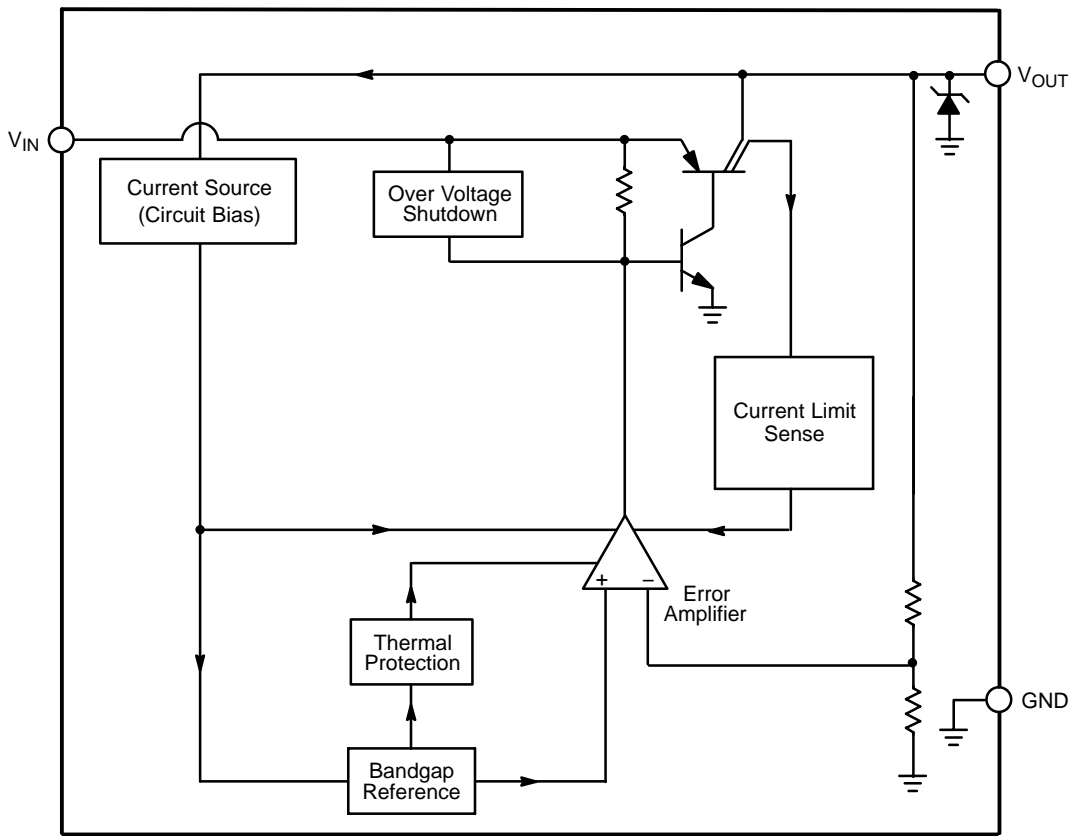


Figure 1. Block Diagram

<http://www.BDTIC.com/ON>

ABSOLUTE MAXIMUM RATINGS*

| Rating | Value | Unit |
|--|--------------------|----------|
| Junction Temperature Range, T_J | -40 to +150 | °C |
| Storage Temperature Range, $T_{STORAGE}$ | -55 to +150 | °C |
| Power Dissipation | Internally Limited | - |
| Peak Transient Voltage (60 V Load Dump @ $V_{IN} = 14 V$) | -15, 74 | V |
| Input Operating Range | -0.5 to 26 | V |
| Output Current | Internally Limited | - |
| Electrostatic Discharge (Human Body Model) | 2.0 | kV |
| Lead Temperature Soldering: | Reflow (Note 1) | 230 peak |

1. 60 seconds maximum above 183°.

*The maximum package power dissipation must be observed.

CS8221

ELECTRICAL CHARACTERISTICS (6.0 ≤ V_{IN} ≤ 26 V, I_{OUT} = 1.0 mA, -40°C ≤ T_J ≤ 125°C unless otherwise noted.)

| Characteristic | Test Conditions | Min | Typ | Max | Unit |
|---|--|-------------|-----------------|------------------|----------------|
| Output Stage | | | | | |
| Output Voltage, V _{OUT} | 9.0 V < V _{IN} < 26 V, 100 μA ≤ I _{OUT} ≤ 100 mA 6.0 V ≤ V _{IN} ≤ 26 V, 100 μA ≤ I _{OUT} ≤ 100 mA | 4.9 4.85 | 5.0 5.0 | 5.1 5.15 | V V |
| Dropout Voltage (V _{IN} - V _{OUT}) | I _{OUT} = 100 mA I _{OUT} = 100 μA | - - | 400 100 | 600 150 | mV mV |
| Load Regulation | V _{IN} = 14 V, 100 μA ≤ I _{OUT} ≤ 100 mA, | - | 5.0 | 50 | mV |
| Line Regulation | 6.0 V < V < 26 V, I _{OUT} = 1.0 mA | - | 5.0 | 50 | mV |
| Quiescent Current, (I _Q) | I _{OUT} = 100 μA, V _{IN} = 6.0 V I _{OUT} = 50 mA I _{OUT} = 100 mA | - - - | 60 4.0 12 | 120 6.0 20 | μA mA mA |
| Ripple Rejection | 7.0 ≤ V _{IN} ≤ 17 V, I _{OUT} = 100 mA, f = 120 Hz | 60 | 75 | - | dB |
| Current Limit | - | 125 | 200 | - | mA |
| Short Circuit Output Current | V _{OUT} = 0 V | 40 | 125 | - | μA |
| Thermal Shutdown (Note 2) | - | 150 | 180 | - | °C |
| Overshoot Shutdown | V _{OUT} ≤ 1.0 V | 30 | 34 | 38 | V |

2. This parameter is guaranteed by design, but not parametrically tested in production.

PACKAGE LEAD DESCRIPTION

| PACKAGE LEAD # | | LEAD SYMBOL | FUNCTION |
|----------------|---------|------------------|------------------------------|
| SO-8 | DIPAK-3 | | |
| 1 | 3 | V _{OUT} | 5.0 V, ±2.0%, 100 mA Output. |
| 2, 3, 6, 7 | 2 | GND | Ground. |
| 4 | - | NC | No Connection. |
| 5 | - | NC | No Connection. |
| 8 | 1 | V _{IN} | Input Voltage. |

TYPICAL PERFORMANCE CHARACTERISTICS

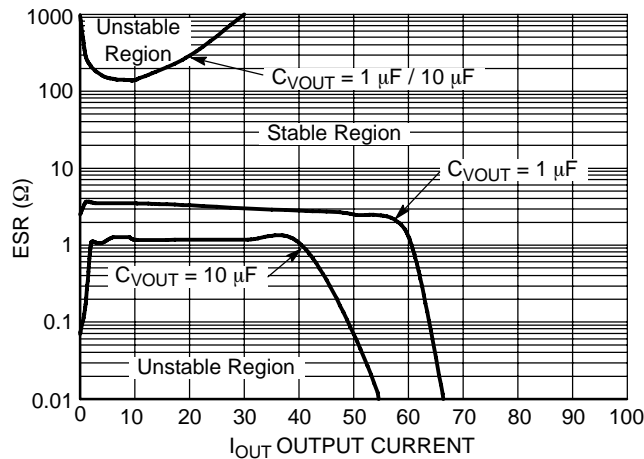


Figure 2. CS8221 Output Stability

CIRCUIT DESCRIPTION

VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 3).

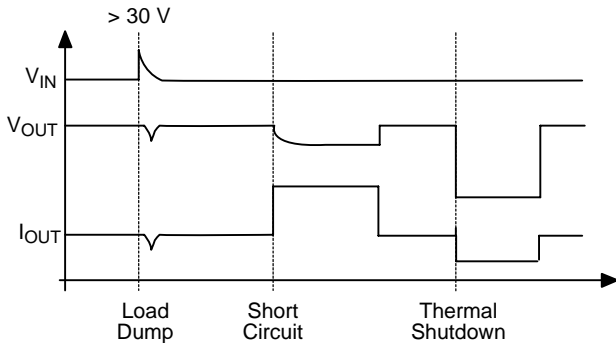
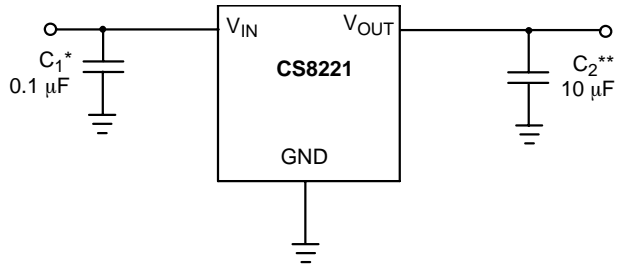


Figure 3. Typical Circuit Waveforms for Output Stage Protection

If the input voltage rises above 30 V, the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Should the junction temperature of the power device exceed 180°C (typ) the power transistor is turned off. Thermal shutdown is an effective means to prevent die overheating since the power transistor is the principle heat source in the IC.



*C₁ is required if regulator is far from the power source filter.

**C₂ is required for stability.

Figure 4. Application and Test Diagram

APPLICATION NOTES

STABILITY CONSIDERATIONS

The output compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (–25°C to –40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_{OUT} shown in Figure 4 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_{OUT} for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Increase the temperature to your highest operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of $\pm 20\%$ so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 5) is:

$$P_{D(max)} = (V_{IN(max)} - V_{OUT(min)})I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

- $V_{IN(max)}$ is the maximum input voltage,
- $V_{OUT(min)}$ is the minimum output voltage,
- $I_{OUT(max)}$ is the maximum output current for the application, and
- I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ\text{C} - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

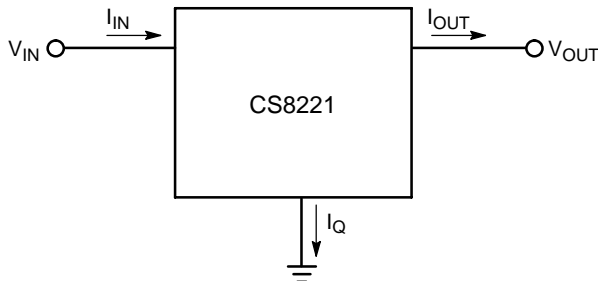


Figure 5. Single Output Regulator With Key Performance Parameters Labeled

HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

- $R_{\theta JC}$ = the junction-to-case thermal resistance,
- $R_{\theta CS}$ = the case-to-heatsink thermal resistance, and
- $R_{\theta SA}$ = the heatsink-to-ambient thermal resistance.

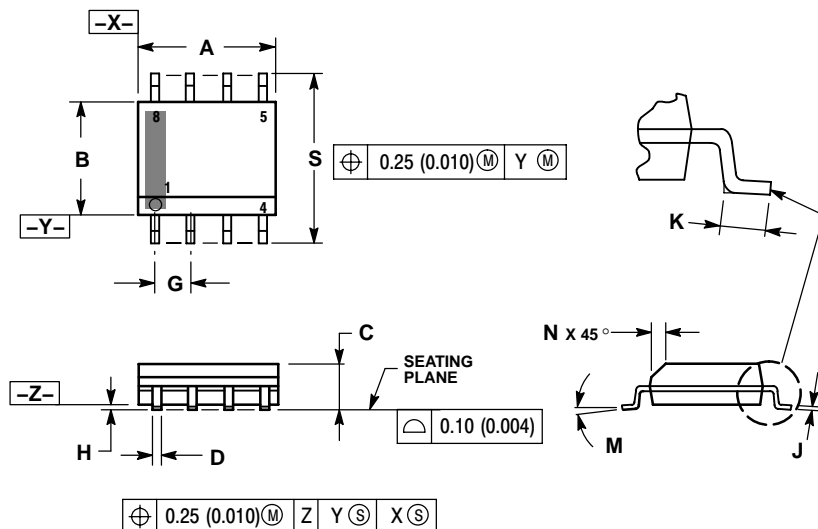
$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

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PACKAGE DIMENSIONS

SO-8
DF SUFFIX
CASE 751-07
ISSUE AG



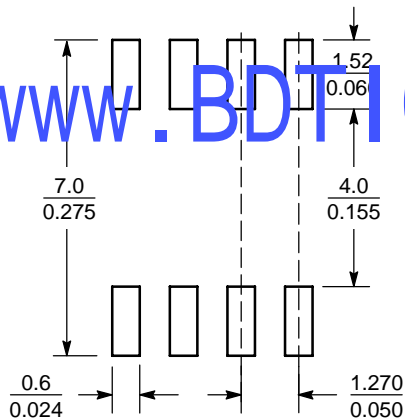
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

SOLDERING FOOTPRINT*

<http://www.BDTIC.com/ON>



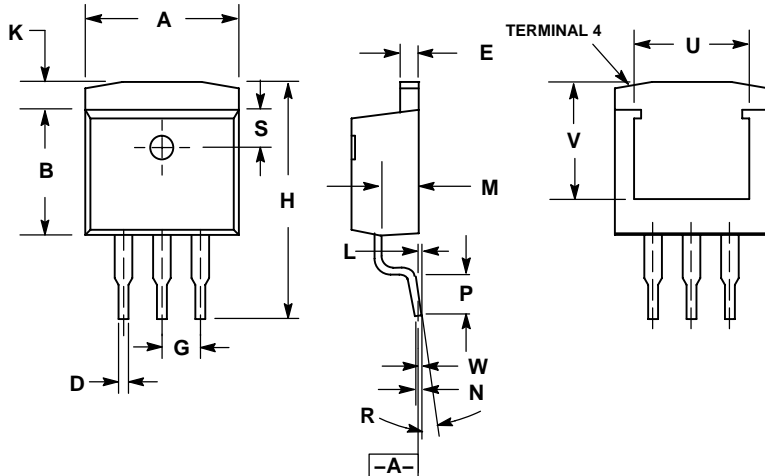
SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

CS8221

PACKAGE DIMENSIONS

D²PAK-3 DP SUFFIX CASE 418AB-01 ISSUE O



NOTES:

1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH AND METAL BURRS.
4. PACKAGE OUTLINE INCLUSIVE OF PLATING THICKNESS.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A AND LEAD SURFACE.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.396 | 0.406 | 10.05 | 10.31 |
| B | 0.330 | 0.340 | 8.38 | 8.64 |
| C | 0.170 | 0.180 | 4.31 | 4.57 |
| D | 0.026 | 0.036 | 0.66 | 0.91 |
| E | 0.045 | 0.055 | 1.14 | 1.40 |
| G | 0.100 REF | | 2.54 REF | |
| H | 0.580 | 0.620 | 14.73 | 15.75 |
| K | 0.055 | 0.066 | 1.40 | 1.68 |
| L | 0.000 | 0.010 | 0.00 | 0.25 |
| M | 0.098 | 0.108 | 2.49 | 2.74 |
| N | 0.017 | 0.023 | 0.43 | 0.58 |
| P | 0.090 | 0.110 | 2.29 | 2.79 |
| R | 0° | 8° | 0° | 8° |
| S | 0.095 | 0.105 | 2.41 | 2.67 |
| U | 0.30 REF | | 7.62 REF | |
| V | 0.305 REF | | 7.75 REF | |
| W | 0.010 | | 0.25 | |

<http://www.BDTIC.com/ON>

PACKAGE THERMAL DATA

| Parameter | | SO-8 | D ² PAK-3 | Unit |
|------------------|---------|------|----------------------|------|
| R _{θJC} | Typical | 25 | 4.2 | °C/W |
| R _{θJA} | Typical | 110 | 10-50* | °C/W |

* Depending on thermal properties of substrate. R_{θJA} = R_{θJC} = R_{θCA}

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