

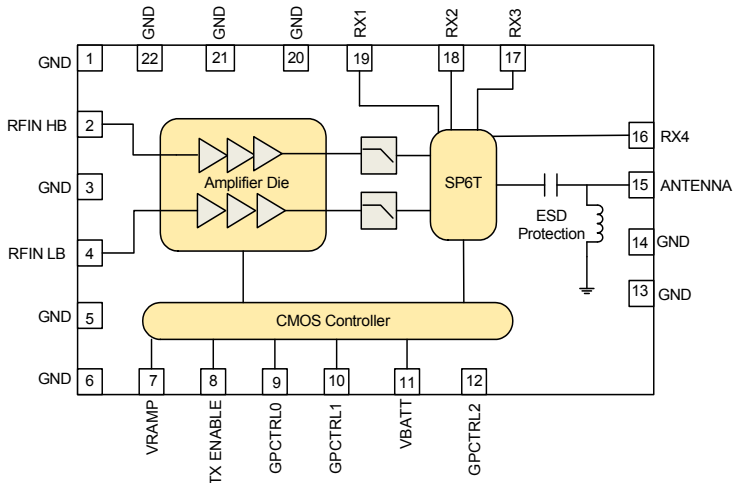


Features

- Proven PowerStar® Architecture
- High Efficiency at Rated P_{OUT}
 $V_{BATT} = 3.5V$
 GSM850/EGSM900 = 41%
 DCS1800/PCS1900 = 38%
- Integrated Power Flattening Circuit for Lower Power Variation under Mismatch Conditions
- Integrated V_{BATT} Tracking Circuit for Improved Switching Spectrum under Low V_{BATT} Conditions
- Integrated V_{RAMP} Filter
- Digital Bias Control
- EDGE Low Current Mode
- No External Routing
- Symmetrical RX Ports
- High Gain Supports Low Drive Level
- Pin Compatible with RF716x GPRS, TxM Family, and Dual-Band RF9801
- Robust 8kV ESD Protection at Antenna Port

Applications

- GSM850/EGSM900/DCS1800/PCS1900 Products
- 3V Quad-Band GSM/GPRS/EDGE Handsets
- Mobile GPRS/EDGE Data Products
- Portable Battery-Powered Equipment
- GPRS Class 12 Compliant Products



Functional Block Diagram

Product Description

The RF9802 is a quad band (GSM850/EGSM900/DCS1800/PCS1900) GSM/GPRS/Linear EDGE, Class 12-compliant Transmit Module with two symmetrical receive ports. This transmit module builds upon RFMD's successful RF716x family, incorporating full EDGE capability while maintaining a common footprint for ease of phone platform design. The RF9802 continues to build upon RFMD's leading patented PowerStar® Architecture to include such features as Power Flattening, V_{RAMP} Filtering, V_{BATT} Tracking, and EDGE Low Power Mode. The module includes a multi-function CMOS controller, GaAs HBT power amplifier, and pHEMT front end antenna switch. RF9802 is designed to operate either in saturated mode for GMSK or linear mode for EDGE 8PSK signaling. The highly integrated transmit module simplifies the phone design by eliminating the need for complicated control loop design, output RF spectrum (ORFS) optimization, harmonic filtering, and component matching, all of which combine to provide best in class RF performance, solution size, and ease of implementation for cellular phone systems. The RF ports are 50Ω matched and the antenna port includes ESD protection circuitry which meets the stringent 8kV industry standards, requiring no additional components. All of these eliminated factors help to improve the customer's product time to market.

Ordering Information

RF9802	Quad-Band GSM850/EGSM900/DCS1800/PCS1900 Transmit Module
RF9802SB	Transmit Module 5-Piece Sample Pack
RF9802PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

- | | | | |
|--|--------------------------------------|--|-----------------------------------|
| <input checked="" type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input checked="" type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS | <input checked="" type="checkbox"/> Si CMOS | <input type="checkbox"/> RF MEMS |
| <input type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si BJT | <input type="checkbox"/> LDMOS |

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.3 to +6.0	V
Power Control Voltage (V _{RAMP})	-0.3 to +3.0	V
Input RF Power	+10	dBm
Max Duty Cycle	50	%
Output Load VSWR	20:1	
Operating Temperature	-30 to +85	°C
Storage Temperature	-55 to +150	°C



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Conditions					
ESD					
ESD RX Pins			1000	V	HBM, JESD22-A114
			500	V	CDM, JESD22-C101C
ESD Antenna Pin			8	kV	IEC 61000-4-2
ESD All Other Pins			1000	V	HBM, JESD22-A114
			500	V	CDM, JESD22-C101C
Overall Power Control V_{RAMP}					
V _{RAMP,MAX} GMSK Mode			1.8	V	Max. P _{OUT}
V _{RAMP,MIN} GMSK Mode		0.25		V	Min. P _{OUT}
V _{RAMP,MAX} High Power EDGE Mode	1.25		3	V	
V _{RAMP,MIN} Low Power EDGE Mode	0		0.5	V	
V _{RAMP} Input Capacitance			10	pF	DC to 200kHz
V _{RAMP} Input Current			10	μA	V _{RAMP} = V _{RAMP,MAX}
Power Control Range		50		dB	V _{RAMP} = 0.25V to V _{RAMP,MAX}
Overall Power Supply					
Power Supply Voltage	3.2	3.5	4.2	V	Operating Limits
Power Supply Current			10	μA	P _{IN} < -30 dBm, TX Enable = Low, V _{RAMP} = 0.25V, Temp = -20°C to +85°C, V _{BATT} = 4.2V
Overall Control Signals					
GpCtrl0, GpCtrl1, GpCtrl2 "Low"	0	0	0.5	V	
GpCtrl0, GpCtrl1, GpCtrl2 "High"	1.25	2.0	3.0	V	
GpCtrl0, GpCtrl1, GpCtrl2 "Input Current"			10	μA	
TX Enable "Low"	0	0	0.5	V	
TX Enable "High"	1.25	2.0	3.0	V	
TX Enable "Input Current"			10	μA	
RF Port Input and Output Impedance		50		Ω	

Module Control and Antenna Switch Logic

TX Enable	GpCtrl2	GpCtrl1	GpCtrl0	VRAMP	Mode
0	0	0	0	0	Standby
0	1	0	0	X	RX1
0	0	1	0	X	RX2
0	0	1	1	X	RX3
0	0	0	1	X	RX4
1	0	1	0	Ramp	Low Band GMSK
1	0	1	1	Ramp	High Band GMSK
1	0	0	0	1	Low Band 8PSK (High Gain)
1	0	0	0	0	Low Band 8PSK (Low Gain)
1	0	0	1	1	High Band 8PSK (High Gain)
1	0	0	1	0	High Band 8PSK (Low Gain)

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
GSM850 Band GMSK Mode					Nominal test conditions unless otherwise stated. $V_{BATT}=3.5V$, $V_{RAMP}=V_{RAMP, MAX}$ GMSK Mode, $P_{IN}=1dBm$, Temp= $+25^{\circ}C$, Duty Cycle=25%, Pulse Width=1154 μs ., All unused ports=50 Ω . Refer to logic table for mode of operation.
Operating Frequency Range	824		849	MHz	
Input Power	-2	+1	+4	dBm	Full P_{OUT} guaranteed at minimum drive level.
Input VSWR		2:1	2.5:1		Over P_{OUT} range (5 dBm to 33 dBm)
Maximum Output Power	33.0	34		dBm	
	31.0			dBm	$V_{BATT}=3.2V$ to 4.2V, $P_{IN}=-2dBm$ to +4 dBm, Temp= $-20^{\circ}C$ to $+85^{\circ}C$.
Minimum Power Into 3:1 VSWR	30.0			dBm	Minimum power delivered to the load over 360 $^{\circ}$ phase sweep.
PAE (Max P_{OUT})	37	45		%	Max P_{OUT}
PAE (Rated P_{OUT})	34	41		%	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$
Peak Supply Current (Max P_{OUT})		1750	2250	mA	Max P_{OUT}
Peak Supply Current (Rated P_{OUT})		1400	1700	mA	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$
2nd Harmonic		-40	-33	dBm	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$.
3rd Harmonic		-40	-33	dBm	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$.
All other harmonics up to 12.75GHz		-40	-33	dBm	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$
Forward Isolation 1		-56	-41	dBm	TX Enable=Low, $P_{IN}=4dBm$, $V_{RAMP}=0.25V$
Forward Isolation 2		-28	-15	dBm	TX Enable=High, $P_{IN}=4dBm$, $V_{RAMP}=0.25V$
Output Noise Power					
	869MHz to 894MHz	-87	-83	dBm	$V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$,
	1930MHz to 1990MHz	-117	-77	dBm	RBW=100 kHz
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=10:1; all phase angles (Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}\leq 33dBm$ into 50 Ω load; load switched to VSWR=10:1), $V_{BATT}=3.2V$ to 4.2V, $P_{IN}=-2dBm$ to +4 dBm, Temp= $-20^{\circ}C$ to $+85^{\circ}C$, RBW=3MHz, no oscillations
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=20:1; all phase angles (Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$ into 50 Ω load; load switched to VSWR=20:1), $V_{BATT}=3.2V$ to 4.2V, $P_{IN}=-2dBm$ to +4 dBm, Temp= $-30^{\circ}C$ to $+85^{\circ}C$

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
GSM850 Band 8PSK Mode					Nominal test conditions unless otherwise stated. $V_{BATT}=3.5V$, $V_{RAMP}=V_{RAMP, MAX}$ High Power EDGE Mode, Temp = +25 °C, Duty Cycle = 25%, Pulse Width = 1154 μ s. Pin adjusted for required P_{OUT} . All unused ports = 50 Ω . Refer to logic table for mode of operation.
Operating Frequency Range	824		849	MHz	
Input VSWR		2:1	3:1		
Maximum Output Power Meeting EVM and ACPR Spectrum	27	28.0		dBm	
	26.0			dBm	$V_{BATT}=3.2V$ to 4.2V, Temp = -20 °C to +85 °C.
	13.0	19.0		dBm	$V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
Gain, High Power Mode	32		38	dB	$P_{OUT}=27$ dBm
Gain, Low Power Mode	30		36	dB	$P_{OUT}=13$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
Peak Supply Current, High Power Mode		850	1500	mA	$P_{OUT}=27$ dBm
Peak Supply Current, Low Power Mode		270	1000	mA	$P_{OUT}=13$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
PAE, High Power Mode	10	17		%	$P_{OUT}=27$ dBm
PAE, Low Power Mode	0	2		%	$P_{OUT}=13$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
ACPR and Spectrum Mask, High Power Mode		-63	-57	dBc	At 400kHz in 30kHz BW, $P_{OUT}=27$ dBm
ACPR and Spectrum Mask, Low Power Mode		-63	-57	dBc	At 400kHz in 30kHz BW, $P_{OUT}=13$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
EVM RMS, High Power Mode		2	5	%	$P_{OUT}=27$ dBm
EVM RMS, Low Power Mode		2	5	%	$P_{OUT}=13$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
Output Noise Power					
869MHz to 894MHz		-85	-83	dBm	$P_{OUT}=5$ dBm to 27 dBm
1930MHz to 1990MHz		-117	-77	dBm	$P_{OUT}=5$ dBm to 27 dBm
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	Load VSWR = 10:1; all phase angles (Set $P_{OUT}=27$ dBm into 50 Ω load; load switched to VSWR = 10:1), $V_{BATT}=3.2V$ to 4.2V, Temp = -20 °C to +85 °C, RBW = 3MHz, no oscillations

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
EGSM900 Band GMSK Mode					Nominal test conditions unless otherwise stated. $V_{BATT}=3.5V$, $V_{RAMP}=V_{RAMP, MAX}$ GMSK Mode, $P_{IN}=1dBm$, Temp= $+25^{\circ}C$, Duty Cycle=25%, Pulse Width=1154 μs . All unused ports = 50Ω . Refer to logic table for mode of operation.
Operating Frequency Range	880		915	MHz	
Input Power	-2	+1	+4	dBm	Full P_{OUT} guaranteed at minimum drive level.
Input VSWR		2:1	2.5:1		Over P_{OUT} range (5 dBm to 33 dBm)
Maximum Output Power	33.0	34		dBm	
	31.0			dBm	$V_{BATT}=3.2V$ to $4.2V$, $P_{IN}=-2dBm$ to $+4dBm$, Temp= $-20^{\circ}C$ to $+85^{\circ}C$.
Minimum Power Into 3:1 VSWR	30.0			dBm	Minimum power delivered to the load over 360° phase sweep.
PAE (Max P_{OUT})	36	44		%	Max P_{OUT}
PAE (Rated P_{OUT})	33	40		%	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$
Peak Supply Current (Max P_{OUT})		1800	2300	mA	Max P_{OUT}
Peak Supply Current (Rated P_{OUT})		1450	1750	mA	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$
2nd Harmonic		-40	-33	dBm	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$.
3rd Harmonic		-40	-33	dBm	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$.
All other harmonics up to 12.75GHz		-40	-33	dBm	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$
Forward Isolation 1		-56	-41	dBm	TX Enable=Low, $P_{IN}=4dBm$, $V_{RAMP}=0.25V$
Forward Isolation 2		-28	-15	dBm	TX Enable=High, $P_{IN}=4dBm$, $V_{RAMP}=0.25V$
Output Noise Power					
925MHz to 935MHz		-83	-77	dBm	$V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$, RBW=100 kHz
935MHz to 960MHz		-87	-83	dBm	
1805MHz to 1880MHz		-117	-77	dBm	
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=10:1; all phase angles (Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}\leq 33dBm$ into 50Ω load; load switched to VSWR=10:1), $V_{BATT}=3.2V$ to $4.2V$, $P_{IN}=-2dBm$ to $+4dBm$, Temp= $-20^{\circ}C$ to $+85^{\circ}C$, RBW=3MHz, no oscillations
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=20:1; all phase angles (Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=33dBm$ into 50Ω load; load switched to VSWR=20:1), $V_{BATT}=3.2V$ to $4.2V$, $P_{IN}=-2dBm$ to $+4dBm$, Temp= $-30^{\circ}C$ to $+85^{\circ}C$

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
EGSM900 Band 8PSK Mode					Nominal test conditions unless otherwise stated. $V_{BATT}=3.5V$, $V_{RAMP}=V_{RAMP, MAX}$ High Power EDGE Mode, Temp= $+25^{\circ}C$, Duty Cycle=25%, Pulse Width=1154 μs , Pin adjusted for required P_{OUT} . All unused ports =50 Ω . Refer to logic table for mode of operation.
Operating Frequency Range	880		915	MHz	
Input VSWR		2:1	3:1		
Maximum Output Power Meeting EVM and ACPR Spectrum	27	28.0		dBm	
	26.0			dBm	$V_{BATT}=3.2V$ to 4.2V, Temp= $-20^{\circ}C$ to $+85^{\circ}C$.
	13.0	19.0		dBm	$V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
Gain, High Power Mode	32		38	dB	$P_{OUT}=27$ dBm
Gain, Low Power Mode	30		36	dB	$P_{OUT}=13$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
Peak Supply Current, High Power Mode		870	1500	mA	$P_{OUT}=27$ dBm
Peak Supply Current, Low Power Mode		270	1000	mA	$P_{OUT}=13$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
PAE, High Power Mode	9.5	16.5		%	$P_{OUT}=27$ dBm
PAE, Low Power Mode	0	2		%	$P_{OUT}=13$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
ACPR and Spectrum Mask, High Power Mode		-63	-57	dBc	At 400kHz in 30kHz BW, $P_{OUT}=27$ dBm
ACPR and Spectrum Mask, Low Power Mode		-63	-57	dBc	At 400kHz in 30kHz BW, $P_{OUT}=13$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
EVM RMS, High Power Mode		2	5	%	$P_{OUT}=27$ dBm
EVM RMS, Low Power Mode		2	5	%	$P_{OUT}=13$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
Output Noise Power					
925MHz to 935MHz		-83	-77	dBm	$P_{OUT}=5$ dBm to 27 dBm
935MHz to 960MHz		-85	-83	dBm	$P_{OUT}=5$ dBm to 27 dBm
1805MHz to 1880MHz		-117	-77	dBm	$P_{OUT}=5$ dBm to 27 dBm
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	Load VSWR=10:1;all phase angles (Set $P_{OUT}=27$ dBm into 50 Ω load; load switched to VSWR=10:1), $V_{BATT}=3.2V$ to 4.2V, Temp= $-20^{\circ}C$ to $+85^{\circ}C$, RBW=3MHz, no oscillations

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DCS1800 Band GMSK Mode					Nominal test conditions unless otherwise stated. $V_{BATT}=3.5V$, $V_{RAMP}=V_{RAMP,MAX}$ GMSK Mode, $P_{IN}=1dBm$, Temp= $+25^{\circ}C$, Duty Cycle=25%, Pulse Width=1154 μs . All unused ports=50 Ω . Refer to logic table for mode of operation.
Operating Frequency Range	1710		1785	MHz	
Input Power	-2	+1	+4	dBm	Full P_{OUT} guaranteed at minimum drive level.
Input VSWR		2:1	2.5:1		Over P_{OUT} range (0dBm to 30dBm)
Maximum Output Power	30.0	31.5		dBm	
	28.0			dBm	$V_{BATT}=3.2V$ to 4.2V, $P_{IN}=-2dBm$ to +4 dBm, Temp= $-20^{\circ}C$ to $+85^{\circ}C$
Minimum Power Into 3:1 VSWR	27.0			dBm	Minimum power delivered to the load over 360 $^{\circ}$ phase sweep
PAE (Max P_{OUT})	32	40		%	Max P_{OUT}
PAE (Rated P_{OUT})	32	38		%	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$
Peak Supply Current (Max P_{OUT})		1100	1600	mA	Max P_{OUT}
Peak Supply Current (Rated P_{OUT})		750	1000	mA	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$
2nd Harmonic		-40	-33	dBm	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$
3rd Harmonic		-36	-33	dBm	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$
All other harmonics up to 12.75GHz		-40	-33	dBm	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$
Forward Isolation 1		-62	-53	dBm	TX Enable=Low, $P_{IN}=4dBm$, $V_{RAMP}=0.25V$
Forward Isolation 2		-31	-15	dBm	TX Enable=High, $P_{IN}=4dBm$, $V_{RAMP}=0.25V$
Output Noise Power					
925MHz to 935MHz		-100	-81	dBm	$V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$, RBW=100 kHz
935MHz to 960MHz		-100	-85	dBm	
1805MHz to 1880MHz		-90	-77	dBm	
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=10:1; all phase angles (Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}\leq 30dBm$ into 50 Ω load; load switched to VSWR=10:1), $V_{BATT}=3.2V$ to 4.2V, $P_{IN}=-2dBm$ to +4 dBm, Temp= $-20^{\circ}C$ to $+85^{\circ}C$, RBW=3 MHz, no oscillations
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=20:1; all phase angles (Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$ into 50 Ω load; load switched to VSWR=20:1), $V_{BATT}=3.2V$ to 4.2V, $P_{IN}=-2dBm$ to +4 dBm, Temp= $-30^{\circ}C$ to $+85^{\circ}C$

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
DCS1800 Band 8PSK Mode					Nominal test conditions unless otherwise stated. $V_{BATT} = 3.5V$, $V_{RAMP} = V_{RAMP, MAX}$ High Power EDGE Mode, Temp = +25 °C, Duty Cycle = 25%, Pulse Width = 1154µs. All unused ports = 50Ω. Refer to logic table for mode of operation.
Operating Frequency Range	1710		1785	MHz	
Input VSWR		2:1	2.5:1		
Maximum Output Power Meeting EVM and ACPR Spectrum	26.5	27.0		dBm	
	25.0			dBm	$V_{BATT} = 3.2V$ to 4.2V, Temp = -20 °C to +85 °C.
	12.0	18.0		dBm	$V_{RAMP} = V_{RAMP, MIN}$ Low Power EDGE Mode
Gain, High Power Mode	31.5		37.5	dB	$P_{OUT} = 26.5$ dBm
Gain, Low Power Mode	29		35	dB	$P_{OUT} = 12$ dBm, $V_{RAMP} = V_{RAMP, MIN}$ Low Power EDGE Mode
Peak Supply Current, High Power Mode		830	1500	mA	$P_{OUT} = 26.5$ dBm
Peak Supply Current, Low Power Mode		200	1000	mA	$P_{OUT} = 12$ dBm, $V_{RAMP} = V_{RAMP, MIN}$ Low Power EDGE Mode
PAE, High Power Mode	8	15		%	$P_{OUT} = 26.5$ dBm
PAE, Low Power Mode	0	2		%	$P_{OUT} = 12$ dBm, $V_{RAMP} = V_{RAMP, MIN}$ Low Power EDGE Mode
ACPR and Spectrum Mask, High Power Mode		-67	-57	dBc	At 400kHz in 30kHz BW, $P_{OUT} = 26.5$ dBm
ACPR and Spectrum Mask, Low Power Mode		-67	-57	dBc	At 400kHz in 30kHz BW, $P_{OUT} = 12$ dBm, $V_{RAMP} = V_{RAMP, MIN}$ Low Power EDGE Mode
EVM RMS, High Power Mode		3	5	%	$P_{OUT} = 26.5$ dBm
EVM RMS, Low Power Mode		1	5	%	$P_{OUT} = 12$ dBm, $V_{RAMP} = V_{RAMP, MIN}$ Low Power EDGE Mode
Output Noise Power					
925MHz to 935MHz		-95	-81	dBm	$P_{OUT} = 0$ dBm to 26.5 dBm
935MHz to 960MHz		-95	-85	dBm	$P_{OUT} = 0$ dBm to 26.5 dBm
1805MHz to 1880MHz		-85	-77	dBm	$P_{OUT} = 0$ dBm to 26.5 dBm
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR = 10:1; all phase angles (Set $P_{OUT} = 27.5$ dBm into 50Ω load; load switched to VSWR = 10:1), $V_{BATT} = 3.2V$ to 4.2V, Temp = -20 °C to +85 °C, RBW = 3 MHz, no oscillations

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
PCS1900 Band GMSK Mode					Nominal test conditions unless otherwise stated. $V_{BATT}=3.5V$, $V_{RAMP}=V_{RAMP, MAX}$ GMSK Mode, $P_{IN}=1dBm$, Temp= $+25^{\circ}C$, Duty Cycle=25%, Pulse Width=1154 μs . All unused ports=50 Ω . Refer to logic table for mode of operation.
Operating Frequency Range	1850		1910	MHz	
Input Power	-2	+1	+4	dBm	Full P_{OUT} guaranteed at minimum drive level.
Input VSWR		2:1	2.5:1		Over P_{OUT} range (0dBm to 30dBm)
Maximum Output Power	30.0	31.5		dBm	
	28.0			dBm	$V_{BATT}=3.2V$ to 4.2V, $P_{IN}=-2dBm$ to +4 dBm, Temp= $-20^{\circ}C$ to $+85^{\circ}C$
Minimum Power Into 3:1 VSWR	27.0			dBm	Minimum power delivered to the load over 360 $^{\circ}$ phase sweep
PAE (Max P_{OUT})	32	39		%	Max P_{OUT}
PAE (Rated P_{OUT})	32	38		%	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$
Peak Supply Current (Max P_{OUT})		1100	1600	mA	Max P_{OUT}
Peak Supply Current (Rated P_{OUT})		750	1000	mA	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$
2nd Harmonic		-40	-33	dBm	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$
3rd Harmonic		-40	-33	dBm	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$
All other harmonics up to 12.75GHz		-40	-33	dBm	Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$
Forward Isolation 1		-60	-53	dBm	TX Enable=Low, $P_{IN}=4dBm$, $V_{RAMP}=0.25V$
Forward Isolation 2		-30	-15	dBm	TX Enable=High, $P_{IN}=4dBm$, $V_{RAMP}=0.25V$
Output Noise Power					
869MHz to 894MHz		-100	-85	dBm	$V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$, RBW=100 kHz
1930MHz to 1990MHz		-90	-77	dBm	
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR=10:1; all phase angles (Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}\leq 30dBm$ into 50 Ω load; load switched to VSWR=10:1), $V_{BATT}=3.2V$ to 4.2V, $P_{IN}=-2dBm$ to +4 dBm, Temp= $-20^{\circ}C$ to $+85^{\circ}C$, RBW=3MHz, no oscillations
Output Load VSWR Ruggedness	No damage or permanent degradation to device				VSWR=20:1; all phase angles (Set $V_{RAMP}=V_{RAMP}$ rated for $P_{OUT}=30dBm$ into 50 Ω load; load switched to VSWR=20:1), $V_{BATT}=3.2V$ to 4.2V, $P_{IN}=-2dBm$ to +4 dBm, Temp= $-30^{\circ}C$ to $+85^{\circ}C$

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
PCS1900 Band 8PSK Mode					Nominal test conditions unless otherwise stated. $V_{BATT}=3.5V$, $V_{RAMP}=V_{RAMP, MAX}$ High Power EDGE Mode, Temp = +25 °C, Duty Cycle = 25%, Pulse Width = 1154 μ s. Pin adjusted for required P_{OUT} . All unused ports = 50 Ω . Refer to logic table for mode of operation.
Operating Frequency Range	1850		1910	MHz	
Input VSWR		2:1	2.5:1		
Maximum Output Power Meeting EVM and ACPR Spectrum	26.5	27.0		dBm	
	25.0			dBm	$V_{BATT}=3.2V$ to 4.2V, Temp = -20 °C to +85 °C.
	12.0	18.0		dBm	$V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
Gain, High Power Mode	31.5		37.5	dB	$P_{OUT}=26.5$ dBm
Gain, Low Power Mode	29		35	dB	$P_{OUT}=12$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
Peak Supply Current, High Power Mode		830	1500	mA	$P_{OUT}=26.5$ dBm
Peak Supply Current, Low Power Mode		200	1000	mA	$P_{OUT}=12$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
PAE, High Power Mode	8	15		%	$P_{OUT}=26.5$ dBm
PAE, Low Power Mode	0	2		%	$P_{OUT}=12$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
ACPR and Spectrum Mask, High Power Mode		-67	-57	dBc	At 400kHz in 30kHz BW, $P_{OUT}=26.5$ dBm
ACPR and Spectrum Mask, Low Power Mode		-67	-57	dBc	At 400kHz in 30kHz BW, $P_{OUT}=12$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
EVM RMS, High Power Mode		3	5	%	$P_{OUT}=26.5$ dBm
EVM RMS, Low Power Mode		1	5	%	$P_{OUT}=12$ dBm, $V_{RAMP}=V_{RAMP, MIN}$ Low Power EDGE Mode
Output Noise Power					
869MHz to 894MHz		-95	-85	dBm	$P_{OUT}=0$ dBm to 26.5 dBm
1930MHz to 1990MHz		-85	-77	dBm	$P_{OUT}=0$ dBm to 26.5 dBm
Output Load VSWR Stability (Spurious Emissions)			-36	dBm	VSWR = 10:1; all phase angles (Set $P_{OUT}=27.5$ dBm into 50 Ω load; load switched to VSWR = 10:1), $V_{BATT}=3.2V$ to 4.2V, Temp = -20 °C to +85 °C, RBW = 3MHz, no oscillations

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RX Section					Nominal test conditions unless otherwise stated. V _{BATT} = 3.5V, Temp = +25 °C, Duty Cycle = 25%, Pulse Width = 1154 μs, V _{RAMP} = V _{RAMP, MIN} . All unused ports = 50Ω. Refer to logic table for mode of operation.
Insertion Loss GSM850 ANT-RX1/RX2/RX3/RX4		1.0	1.3	dB	Freq = 869 MHz to 894 MHz. See Note 1.
In-Band Ripple GSM850 ANT-RX1/RX2/RX3/RX4			0.2	dB	Freq = 869 MHz to 894 MHz
Input VSWR GSM850 ANT-RX1/RX2/RX3/RX4		1.2:1	1.5:1		Freq = 869 MHz to 894 MHz
Insertion Loss EGSM900 ANT-RX1/RX2/RX3/RX4		1.0	1.3	dB	Freq = 925 MHz to 960 MHz. See note 1.
In-Band Ripple EGSM900 ANT-RX1/RX2/RX3/RX4			0.2	dB	Freq = 925 MHz to 960 MHz
Input VSWR EGSM900 ANT-RX1/RX2/RX3/RX4		1.2:1	1.5:1		Freq = 925 MHz to 960 MHz
Insertion Loss DCS1800 ANT-RX1/RX2/RX3/RX4		1.3	1.7	dB	Freq = 1805 MHz to 1880 MHz. See Note 1.
In-Band Ripple DCS1800 ANT-RX1/RX2/RX3/RX4			0.2	dB	Freq = 1805 MHz to 1880 MHz
Input VSWR DCS1800 ANT-RX1/RX2/RX3/RX4		1.8:1	2:1		Freq = 1805 MHz to 1880 MHz
Insertion Loss PCS1900 ANT-RX1/RX2/RX3/RX4		1.6	1.9	dB	Freq = 1930 MHz to 1990 MHz. See note 1.
In-Band Ripple PCS1900 ANT-RX1/RX2/RX3/RX4			0.2	dB	Freq = 1930 MHz to 1990 MHz
Input VSWR PCS1900 ANT-RX1/RX2/RX3/RX4		1.9:1	2.1:1		Freq = 1930 MHz to 1990 MHz
TX Section					
TX Leakage to RX Ports (RX1/RX2/RX3/RX4) GSM850		-3	4.0	dBm	LB TX mode: Freq = 824 MHz to 849 MHz, V _{RAMP} = V _{RAMP} rated for P _{OUT} = 33 dBm at Antenna port. See Note 2.
TX Leakage to RX Ports (RX1/RX2/RX3/RX4) EGSM900		-2	4.0	dBm	LB TX mode: Freq = 880 MHz to 915 MHz, V _{RAMP} = V _{RAMP} rated for P _{OUT} = 33 dBm at Antenna port. See Note 2.
TX Leakage to RX Ports (RX1/RX2/RX3/RX4) DCS1800		1.0	5.0	dBm	HB TX mode: Freq = 1710 MHz to 1785 MHz, V _{RAMP} = V _{RAMP} rated for P _{OUT} = 30 dBm at Antenna port. See Note 2.
TX Leakage to RX Ports (RX1/RX2/RX3/RX4) PCS1900		2.5	5.0	dBm	HB TX mode: Freq = 1850 MHz to 1910 MHz, V _{RAMP} = V _{RAMP} rated for P _{OUT} = 30 dBm at Antenna port. See Note 2.

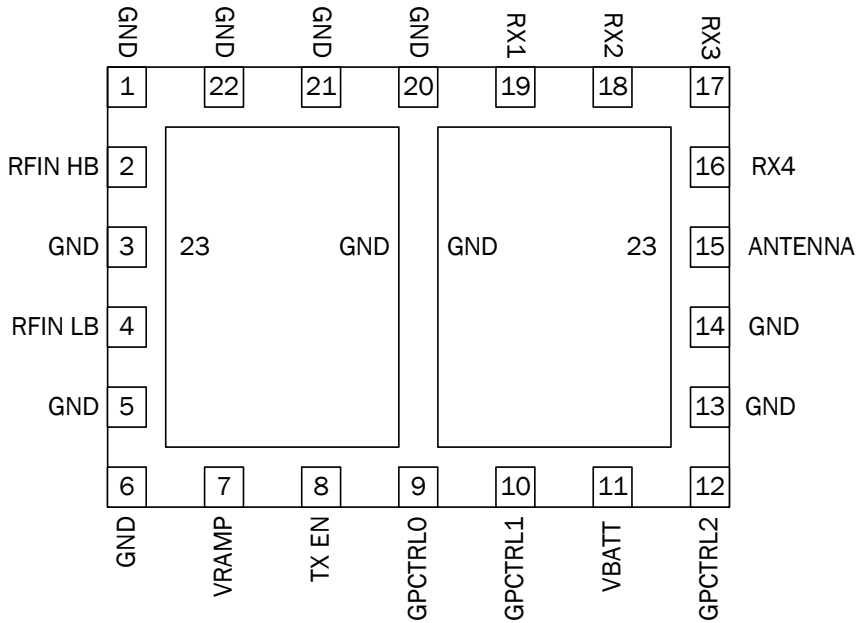
Note 1: The insertion loss values listed are the values guaranteed at the DUT port reference plane (i.e. excludes external mismatch and resistive trace losses).

Note 2: Isolation specification set to ensure at least the following isolation at rated P_{OUT}:

Calculation Example using typical values: Isolation = P_{OUT} at Antenna - P_{OUT} at RX Port. Isolation LB = 33 - 3 = 30 dB, Isolation HB = 30 - 3 = 27 dB.

Pin	Function	Description
1	GND	Pin connected to module Ground.
2	RFIN HB	RF input to the DCS1800/PCS1900 band. This is a 50Ω input.
3	GND	Pin connected to module Ground.
4	RFIN LB	RF input to the GSM850/EGSM900 band. This is a 50Ω input.
5	GND	Pin connected to module Ground.
6	GND	Pin connected to module Ground.
7	VRAMP	V _{RAMP} ramping signal from DAC. A simple RC filter is integrated into the RF9802 module. V _{RAMP} may or may not require additional filtering depending on the baseband selected.
8	TX ENABLE	This signal enables the PA module for operation with a logic high. The switch is put in TX mode determined by GpCtrl0 and GpCtrl1.
9	GPCTRL0	Control pin that together with GpCtrl1 and GpCtrl2 selects mode of operation.
10	GPCTRL1	Control pin that together with GpCtrl0 and GpCtrl2 selects mode of operation.
11	VBATT	Power supply for the module. This should be connected to the battery terminal using as wide a trace as possible.
12	GPCTRL2	Control pin that together with GpCtrl0 and GpCtrl1 selects mode of operation.
13	GND	Pin connected to module Ground.
14	GND	Pin connected to module Ground.
15	ANTENNA	Antenna port.
16	RX4	RX4 port of antenna switch. This is a 50Ω output. RX4 is interchangeable with RX1, RX2, RX3.
17	RX3	RX3 port of antenna switch. This is a 50Ω output. RX3 is interchangeable with RX1, RX2, RX4.
18	RX2	RX2 port of antenna switch. This is a 50Ω output. RX2 is interchangeable with RX1, RX3, RX4.
19	RX1	RX1 port of antenna switch. This is a 50Ω output. RX1 is interchangeable with RX2, RX3, RX4.
20	GND	Pin connected to module Ground.
21	GND	Pin connected to module Ground.
22	GND	Pin connected to module Ground.
23	GND	Pin connected to module Ground.

Pin Out (Top View)



Theory of Operation

Overview

The RF9802 is designed for use as the final portion of the transmit section in mobile phones covering the GSM850/EGSM900 and DCS1800/PCS1900 frequency bands. The RF9802 is a high power, dual mode GSM/EDGE, power amplifier module containing RFMD's patented PowerStar® Architecture. The module includes a multi-function CMOS controller, GaAs HBT power amplifier, and pHEMT front end antenna switch. The integrated power control loop can be driven directly from the baseband DAC to provide a very predictable power output which enables handset manufacturers to achieve simple and efficient phone calibration in production.

Additional Features

Power Flattening Circuit

When a mismatch is presented to the antenna of the phone, the output impedance presented to the PA also varies resulting in variation of output power and current. This can compromise the PA's ability to maintain the minimum output power required for calls, and limit the total radiated power (TRP), to meet the requirements of governmental agencies and cellular service providers. The PFC sets a reference voltage into 50Ω and the Internal feedback loop corrects for impedance variation by reducing the power and current variation into mismatch conditions.

V_{RAMP} Filtering

The V_{RAMP} control voltage is received from the Baseband DAC. The DAC signal is usually in the form of a staircase waveform related to the DAC bit resolution and the timing of the power steps. The staircase waveform usually requires some filtering to smooth out the waveform and reduce any unwanted spectral components showing up in the switching spectra of the RF output signal. A simple RC filter may be integrated into the Baseband, Transmit module or with discrete components between the two.

V_{BATT} Tracking/V_{RAMP} Limiter

This circuit monitors the relationship of the battery voltage and V_{RAMP}/V_{CC} used to control the PA. At low V_{BATT} levels the FET pass-device which controls V_{CC} can enter into a saturation region which can increase switching transients. The saturation detection circuit automatically monitors the battery voltage and produces a correction so that V_{CC} is reduced, thus preventing the power control loop from reaching saturation and inducing switching transients.

EDGE Low Power Option

In EDGE mode the PA operates in the linear region and the P_{OUT} is controlled by the P_{IN} . Since the phone tends to operate most of its time in the lower to mid power ranges the bias can be adjusted to optimize efficiency. The RF9802 quiescent current can be changed in the power amplifier when operating at lower output power levels by setting V_{RAMP} to 0.5V which will change high power mode to low power mode.

Modes of Operation: Saturated GMSK and Linear EDGE

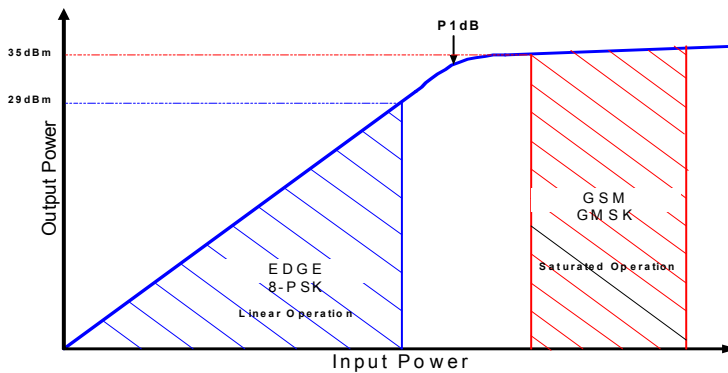
The design of a dual mode power amplifier module is a challenging process involving many circuit compromises and performance tradeoffs to allow best performance in both the saturated and linear operating regions. This is most demanding in achieving best performance between GSM efficiency and EDGE linearity requirements.

In GSM mode, the GMSK modulation is a constant envelope and the useful data is entirely included in the phase of the signal. Since the constant envelope is not sensitive to amplitude non-linearities caused by the PA, the amplifier can operate in saturation mode (deep class AB or class C) for optimum efficiency.

In EDGE mode, the 8PSK signal has information encoded in both amplitude and phase, which requires a linear power amplifier (Class A) to transfer the 8PSK modulation with minimal distortion.

In a dual mode module, tuning of the load line must be balanced between GSM efficiency and EDGE linearity. The result is slightly lower GSM efficiency than a single mode (saturated only) power amplifier module. Figure 1 shows the Power Amplifier operating regions in GSM and EDGE mode.

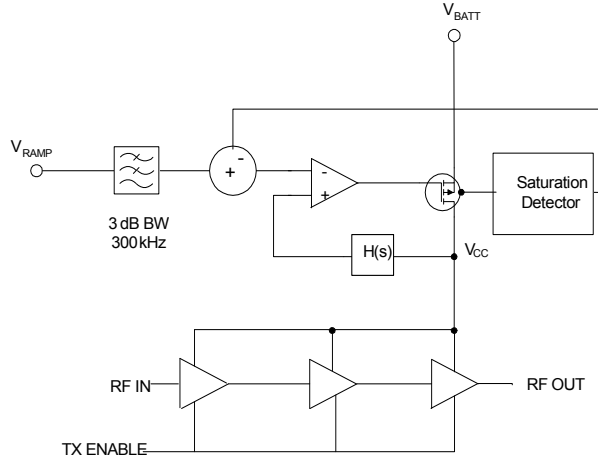
Power Amplifier Operating Regions in GSM/EDGE Mode



GSM (saturated) MODE:

In GSM mode, RF9802 operates as a traditional PowerStar® module.

Basic PowerStar® Circuit Diagram



The control circuit receives a DAC voltage (V_{RAMP}) to set the required output power for the phone. The PowerStar® I architectures multiplies the V_{RAMP} voltage level and regulates it at the collector (V_{CC}) of all three stages of the amplifier, holding the stages in saturation. The base bias is fixed at a point that is at least deep class AB or class C. By holding the PA in saturation, performance sensitivity is essentially eliminated to temperature, frequency, voltage and input drive level ensuring robust performance within the ETSI power vs time mask.

The regulation of power is demonstrated in Equation 1. The equation shows that load impedance affects output power, but to a lesser degree than the V_{CC} supply variations. Since the architecture regulates V_{CC} , the dominant cause of power variation is eliminated. The control loop provides a very linear relationship between V_{RAMP} and P_{OUT} .

$$P_{OUT} = 10 \log \frac{(2 \cdot V_{CC} - V_{SAT})^2}{8 \cdot R_L \cdot 10^{-3}}$$

Equation 1. Output Power versus Voltage Relationship

The RF signal applied at the RFIN pin must be a constant amplitude signal and should be high enough to saturate the amplifier in the GSM mode. The input power (P_{IN}) range is indicated in the specifications. Power levels below this range will result in reduced maximum output power and the potential for more variation of output power over extreme conditions. Higher input power is unnecessary and will require more current in the circuitry driving the power amplifier further into saturation which could also result in lower output power.

EDGE (Linear) MODE

In EDGE mode, V_{ramp} is fixed and the output power is directly controlled by input power.

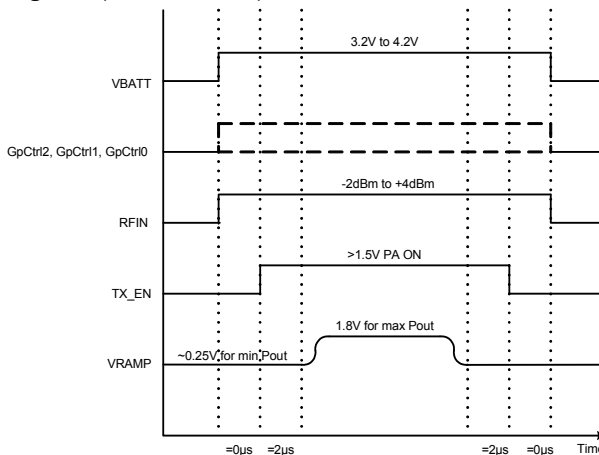
The RF signal applied to the RFIN pin must be accurately controlled to produce the desired output amplitude and burst ramping. The RFIN power must be maintained so that the amplifier is operating in its linear region. If the input drive is too high, the amplifier will begin to saturate causing the ACPR and EVM performance to degrade. The most sensitive of these is typically the +/-400kHz offset ACPR. As the amplifier approaches saturation, this will be the first parameter to show significant degradation.

Since the PAM operates as a gain block in EDGE mode, gain variation over extreme conditions must be considered when determining the output power that a specific input power will produce. Special attention must be given to ensure that the output power of the PA does not go higher than the maximum linear output that the PA can provide with acceptable EVM and ACPR performance.

A large portion of the total current in a linear amplifier is necessary to bias the transistors so that the output remains in the linear region. In an EDGE system where there is a range of power control levels, an amplifier biased to operate at a high power will be very inefficient at low power levels. Conversely, an amplifier biased to operate at a low power will not be linear at high power levels. Refer to the low power mode feature.

Power On (Timing) Sequence

In the Power-On Sequence, there are some important set-up times associated with the control signals of the TxM. Refer to the logic table for control signal functions. One of the critical relationships is the settling time between TXEN going high and when VRAMP can begin to increase. This time is often referred to as the "pedestal" and is required so that the internal power control loop and bias circuitry can settle after being turned on. The PowerStar® architecture usually requires approximately 1µs to 2µs for proper settling of the power control loop.

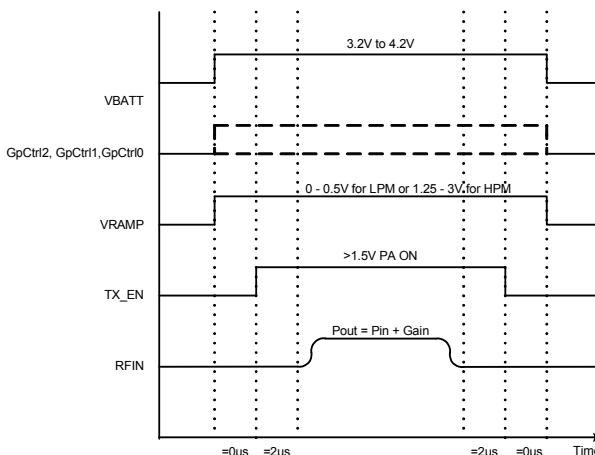


GMSK Power On Sequence:

1. Apply VBATT
2. Apply GpCtrl2, GpCtrl1, GpCtrl0
3. Apply minimum VRAMP (~0.25V)
4. Apply TX_EN
5. Apply VRAMP for desired output power

RFIN can be applied at any time. For good transient response it must be applied before power ramp begins.

The Power Down Sequence is the reverse order of the Power On Sequence.



8PSK Power On Sequence:

1. Apply VBATT
2. Apply GpCtrl2, GpCtrl1, GpCtrl0
3. Apply TX_EN
4. Ramp RFIN amplitude for desired output power

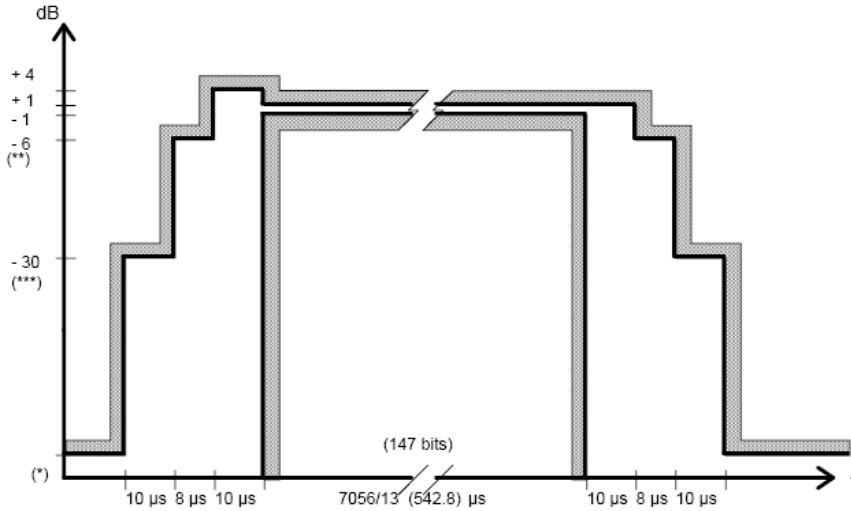
VRAMP is a constant DC input and can be applied anytime after Vbatt

The Power Down Sequence is the reverse order of the Power On Sequence.

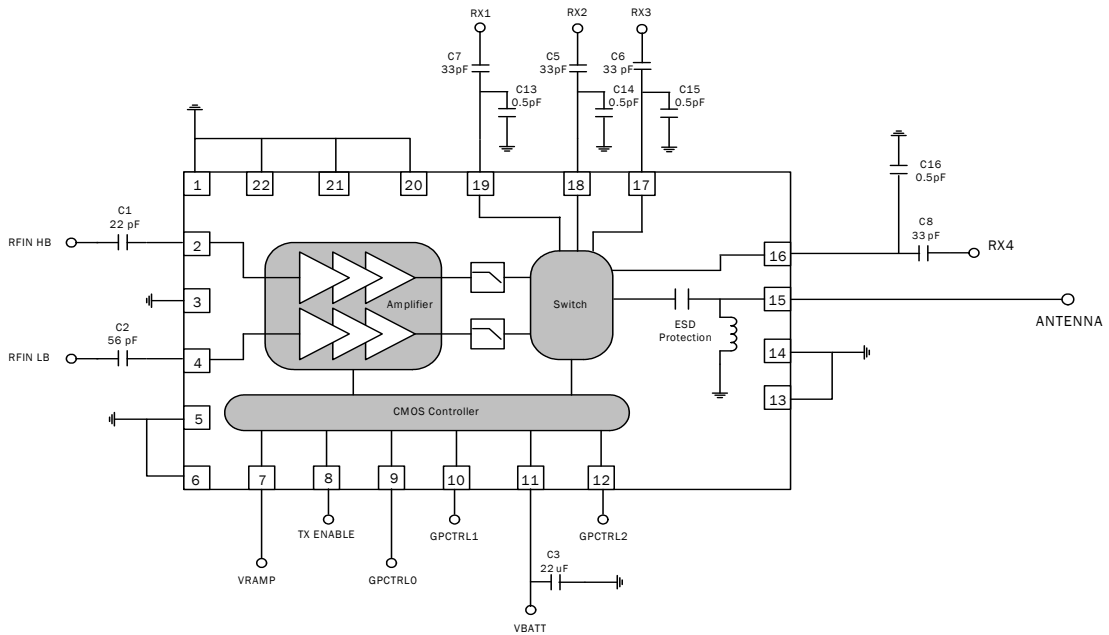
Power Ramping

The V_{RAMP} waveform must be created such that the output power falls into the ETSI power versus time mask. The ability to ramp the RF output power to meet ETSI switching transient and time mask requirements partially depends upon the predictability of output power versus V_{RAMP} response of the power amplifier. The PowerStar[®] control loop is very capable of meeting switching transient requirements with the proper raised cosine waveform applied to the V_{RAMP} input. Ramps usually fall within the 12 μ s to 14 μ s time to control switching transients at high power levels. Faster ramps usually have a steeper transition creating higher transients. Slower ramps may have difficulty meeting the time mask. Optimization needs to include all power levels as the time mask requirements change with P_{OUT} levels.

The diagram below is the ETSI time mask for a single GSM timeslot.



Application Schematic



*All input, output, and antenna traces are 50Ω microstrip.

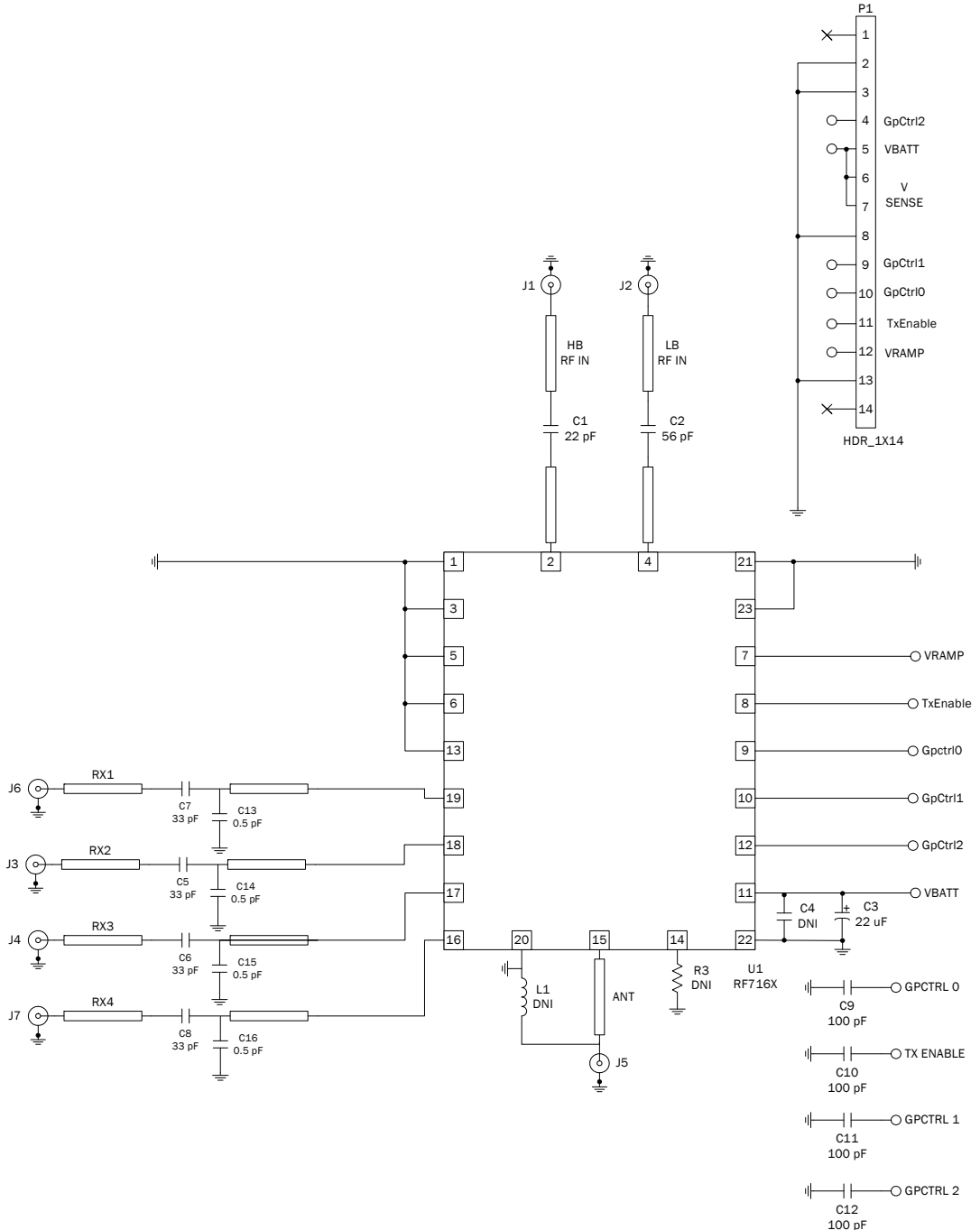
**VBATT capacitor value may change depending on application.

***Series capacitors C5 - C8 are required to block the DC voltage that is present on the RX pins. RX ports usually connect to SAW filters. C13 - C16 will be useful to provide the most flexibility for optimally matching the RX ports to the SAW filter for best RX performance. It may not be needed depending on application.

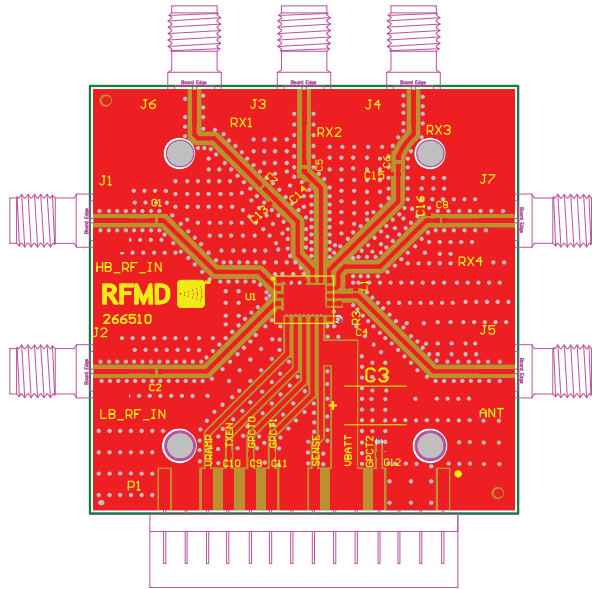
****The recommended ordering of the RX ports for transceiver layout compatibility and isolation requirements is as follows: RX1=GSM850, RX2=EGSM900, RX3=DCS1800, and RX4=PCS1900.

*****If placing an attenuation network on the input to the power amplifier, ensure that it is positioned on the transceiver side of the capacitor C1 (or C2) to prevent adversely affecting the base biasing of the power amplifier.

Evaluation Board Schematic

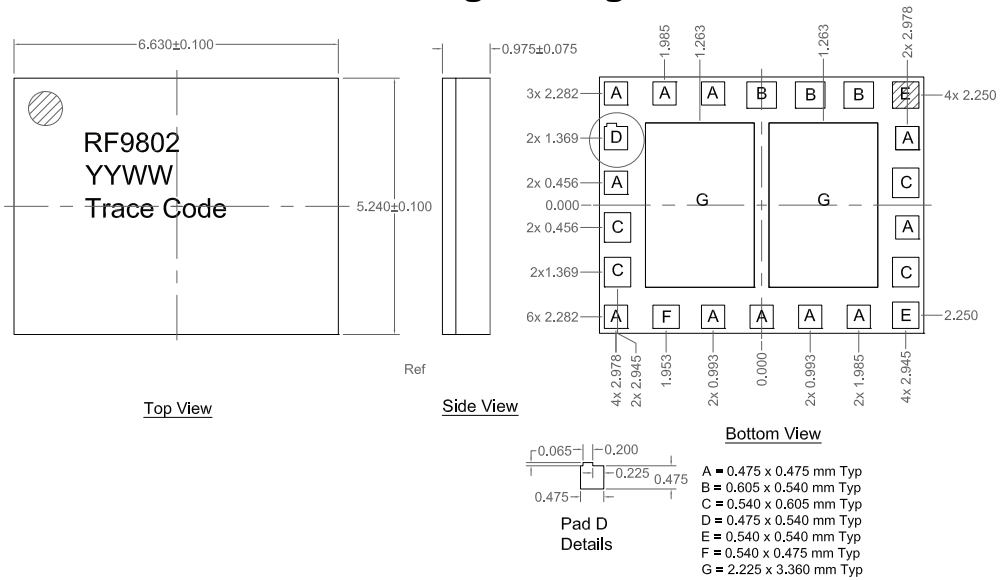


Evaluation Board Layout Board Size 2.0" x 2.0"



Notes: All inputs, outputs, and antenna traces are 50Ω micro strip.

Package Drawing



Notes: Shaded area represents Pin 1 location. YY indicates year, WW indicates work week, and Trace Code is a sequential number assigned at device assembly.

PCB Design Requirements

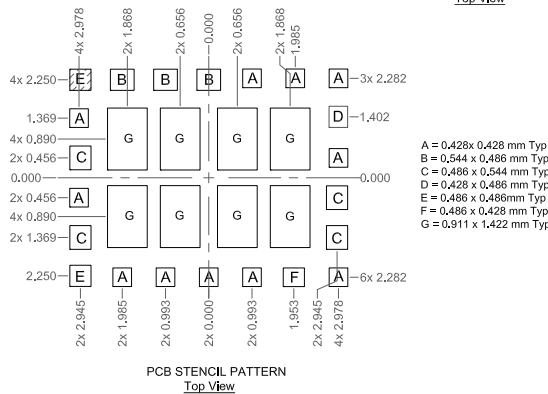
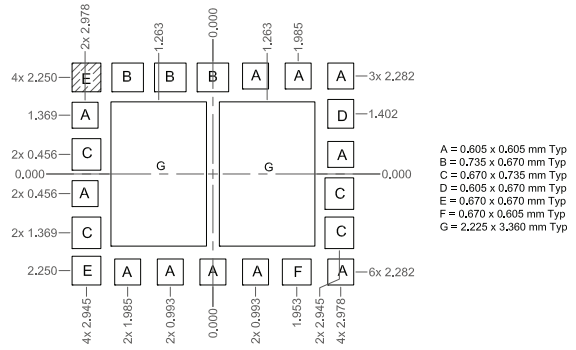
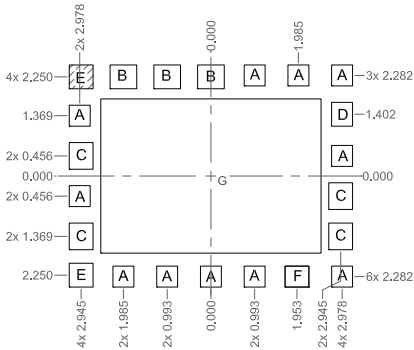
PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land and Solder Mask Pattern



Note: Shaded area represents pin 1 location.

Tape and Reel

Carrier tape basic dimensions are based on EIA 481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

Carrier tape is wound or placed onto a shipping reel either 330mm (13 inches) in diameter or 178mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier ESD bag with the appropriate units of desiccant and a humidity indicator card, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125 °C. If baking is required, devices may be baked according to section 4, table 4-1, of Joint Industry Standard IPC/JEDEC J-STD-033.

The table below provides information for carrier tape and reels used for shipping the devices described in this document.

Tape and Reel

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
RF9802TR13	13 (330)	4 (102)	12	8	Single	2500
RF9802TR7	7 (178)	2.4 (61)	12	8	Single	750

Unless otherwise specified, all dimension tolerances per EIA-481.

