EMIF08-VID01C2

8 line low capacitance EMI filter and ESD protection

Main product characteristics

Where EMI filtering in ESD sensitive equipment is required:

- LCD and camera for mobile phones
- Computers and printers
- Communication systems
- MCU Boards

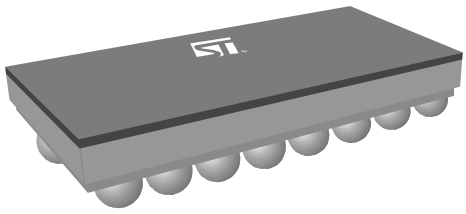
Description

The EMIF08-VID01C2 is an 8 line highly integrated device designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interference. The Flip-Chip packaging means the package size is equal to the die size.

This filter includes ESD protection circuitry, which prevents damage to the application when it is subjected to ESD surges up to 15 kV.

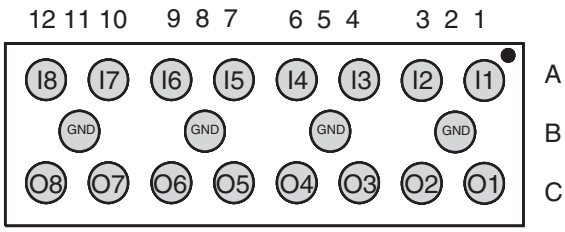
Benefits

- High efficiency EMI filter (-33 dB @ 900 MHz)
- Low line capacitance suitable for high speed data bus
- Low serial resistance for camera impedance adaptation
- Optimized PCB space consuming: 1.29 mm x 3.92 mm
- Very thin package: 0.695 mm
- Coating resin on back side and lead free package
- High efficiency in ESD suppression on inputs pins (IEC 61000-4-2 level 4).
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging.



Coated Flip-Chip package

Pin configuration (Bump side)



Complies with following standards:

IEC 61000-4-2

level 4 input pins	15 kV	(air discharge)
	8 kV	(contact discharge
level 1 output pins	2 kV	(air discharge)
	2 kV	(contact discharge

MIL STD 883E - Method 3015-6 Class 3

1 Characteristics

Figure 1. Basic cell configuration

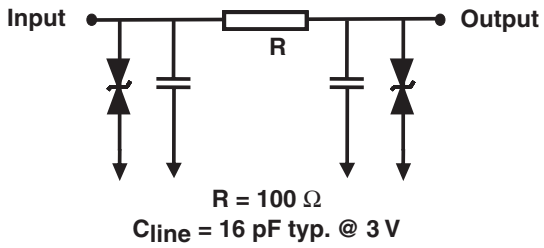
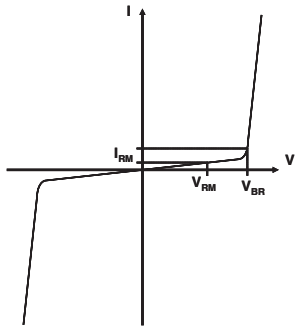


Table 1. Absolute ratings (limiting values)

Symbol	Parameter	Value	Unit
V_{pp}	ESD discharge IEC 61000-4-2 air discharge ESD discharge IEC 61000-4-2 contact discharge	15 8	kV kV
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	-40 to +85	°C
T_{stg}	Storage temperature range	-55 to +150	°C

Table 2. Electrical characteristics (T_{amb} = 25° C)

Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
R	Series resistance between input and output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	I_R = 1 mA	6	8	10	V
I_{RM}	V_{RM} = 3 V per line			500	nA
$R_{I/O}$	I = 10 mA	80	100	120	Ω
C_{line}	V_R = 3 V DC, 1 MHz		16	19	pF

Figure 2. S21 (dB) attenuation measurement

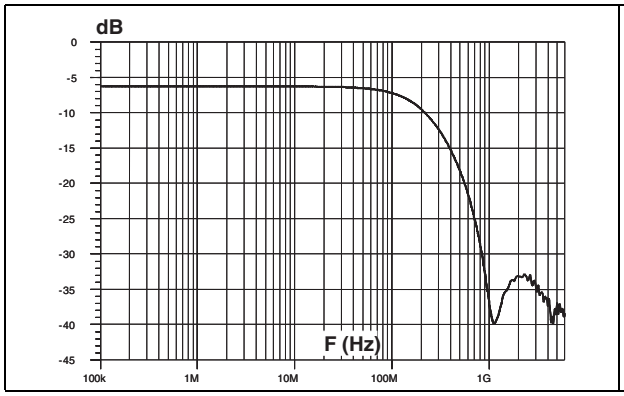


Figure 3. Analog crosstalk measurement

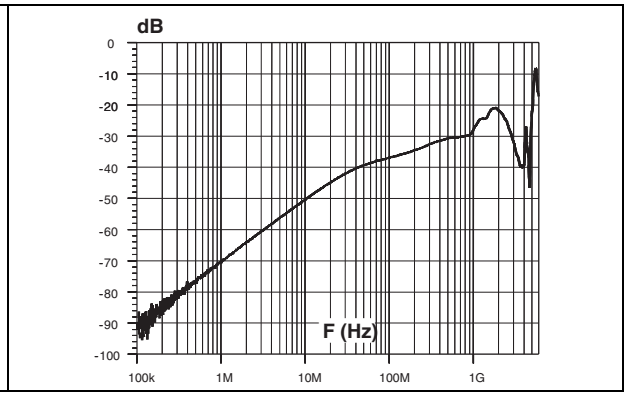


Figure 4. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input V_{in} and one output V_{out}

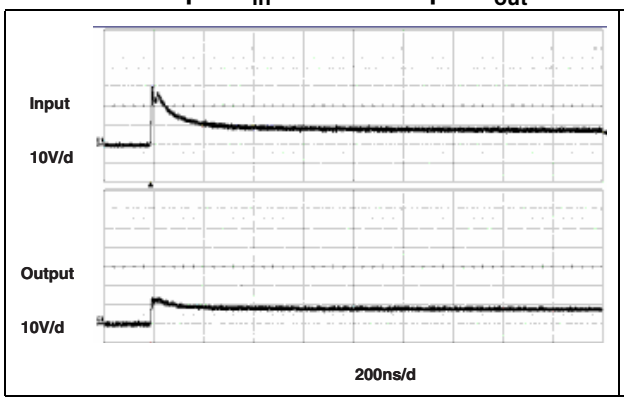


Figure 5. ESD response to IEC 61000-4-2 (- 15 kV air discharge) on one input V_{in} and one output V_{out}

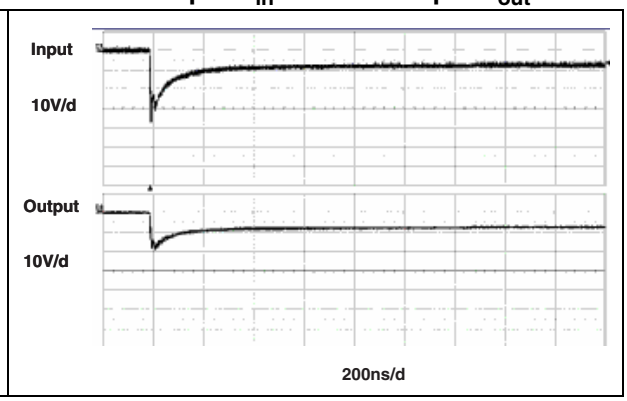
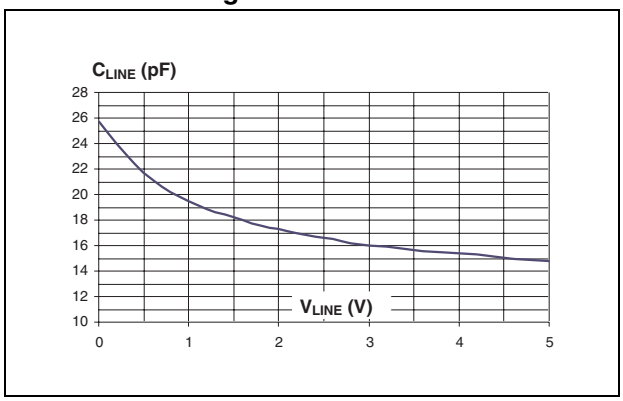
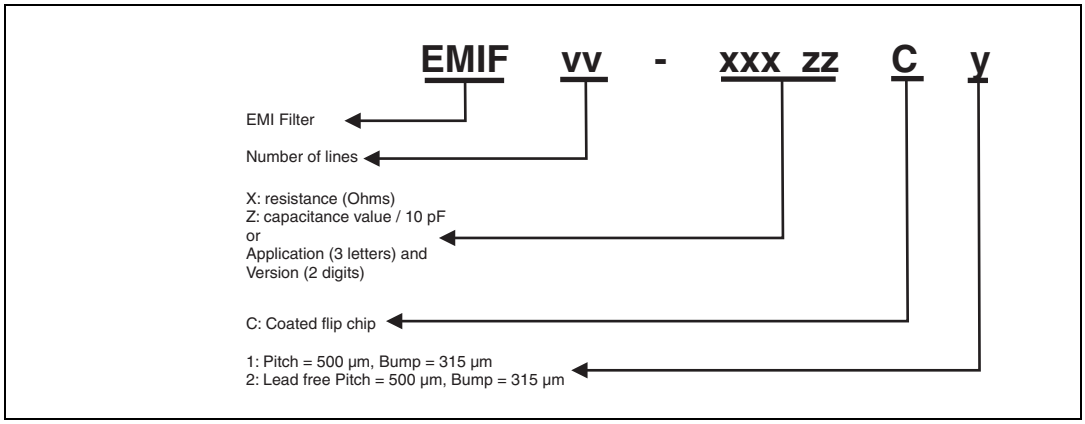


Figure 6. Line capacitance versus applied voltage



2 Ordering information scheme



3 Package information

Figure 7. Flip-Chip Dimensions

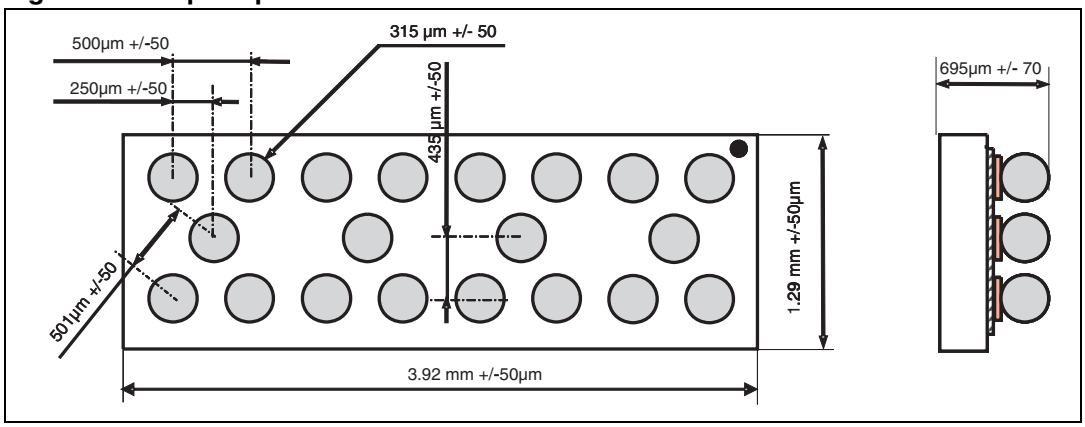


Figure 8. Marking

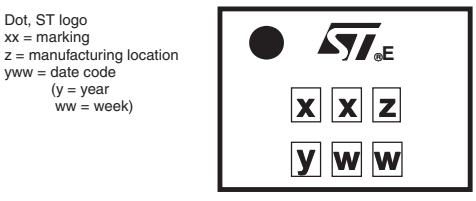


Figure 9. Footprint recommendation

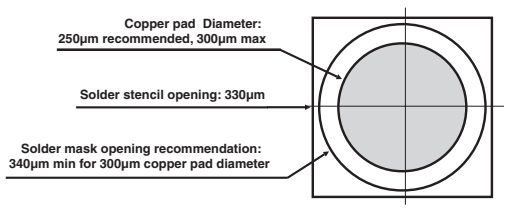
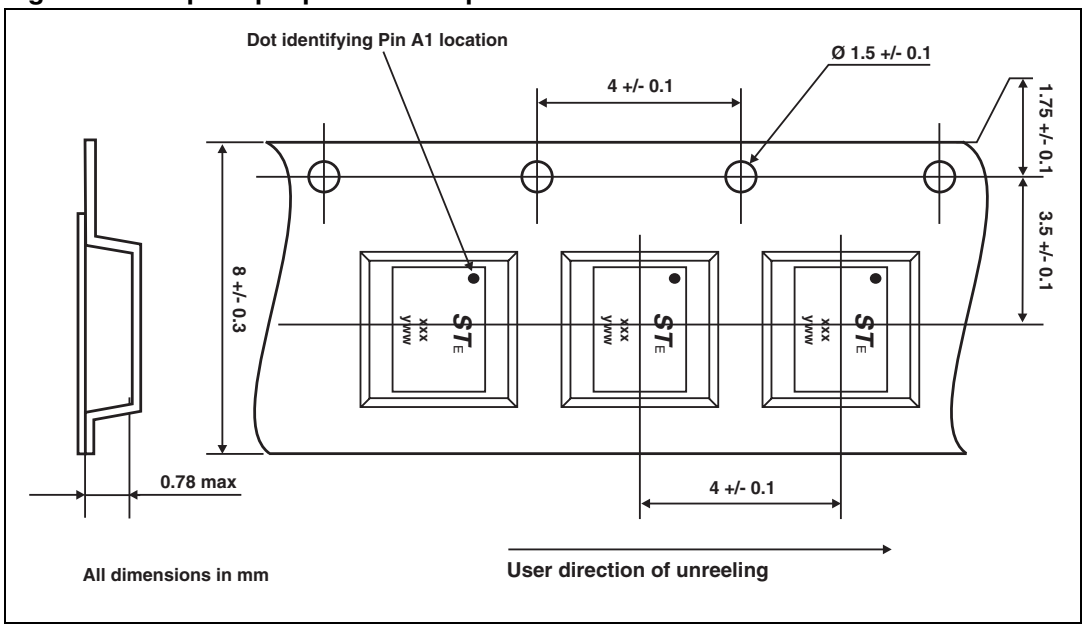


Figure 10. Flip-Chip tape and reel specification



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
EMIF08-VID01C2	GS	Flip-Chip	7.4mg	4000	7” Tape and reel

5 Revision history

Date	Revision	Changes
13-Jul-2005	1	Initial release.
11-Aug-2005	2	Fonts changed in Figures 7, 8, and 9.
31-May-2006	3	Reformatted to current standards. Depth dimension changed in Figure 10.
26-Oct-2006	4	Base quantity changed to 4000 in Ordering information

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