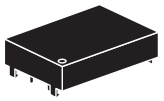
M40Z111
M40Z111W

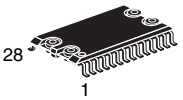
5V or 3V NVRAM supervisor for up to two LPSRAMs

Features

- Convert low power SRAMs into NVRAMs
- Precision power monitoring and power switching circuitry
- Automatic write-protection when V_{CC} is out-of-tolerance
- Choice of supply voltages and power-fail deselect voltages:
  - M40Z111: V_{CC} = 4.5 to 5.5V
    THS = V_{SS}; 4.5 ≤ V_{PFD} ≤ 4.75V
    THS = V_{OUT}; 4.2 ≤ V_{PFD} ≤ 4.5V
  - M40Z111W: V_{CC} = 3.0 to 3.6V
    THS = V_{SS}; 2.8 ≤ V_{PFD} ≤ 3.0V
    V_{CC} = 2.7 to 3.3V
    THS = V_{OUT}; 2.5 ≤ V_{PFD} ≤ 2.7V
- Less than 15ns chip enable access propagation delay (for 5.0v device)
- Packaging includes a 28-lead SOIC and SNAPHAT® top (to be ordered separately)
- SOIC package provides direct connection for a SNAPHAT top which contains the battery
- RoHS compliant
  - Lead-free second level interconnect

SNAPHAT (SH)
battery





SOH28 (MH)

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Contents

www.bdtic.com/ST

List of tables

www.bdtic.com/ST

List of figures

www.bdtic.com/ST

1 Description

The M40Z111/W NVRAM supervisor is a self-contained device which converts a standard low-power SRAM into a non-volatile memory.

A precision voltage reference and comparator monitors the V_{CC} input for an out-of-tolerance condition.

When an invalid V_{CC} condition occurs, the conditioned chip enable ($\overline{E}_{CON}$) output is forced inactive to write-protect the stored data in the SRAM.

During a power failure, the SRAM is switched from the V_{CC} pin to the lithium cell within the SNAPHAT® to provide the energy required for data retention. On a subsequent power-up, the SRAM remains write protected until a valid power condition returns.

The 28-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SOIC and battery packages are shipped separately in plastic anti-static tubes or in Tape & Reel form. For the 28-lead SOIC, the battery package (e.g., SNAPHAT) part number is “M4Z28-BR00SH1” or “M4Z32-BR00SH1” (See *Table 11 on page 19*).

Figure 1. Logic diagram

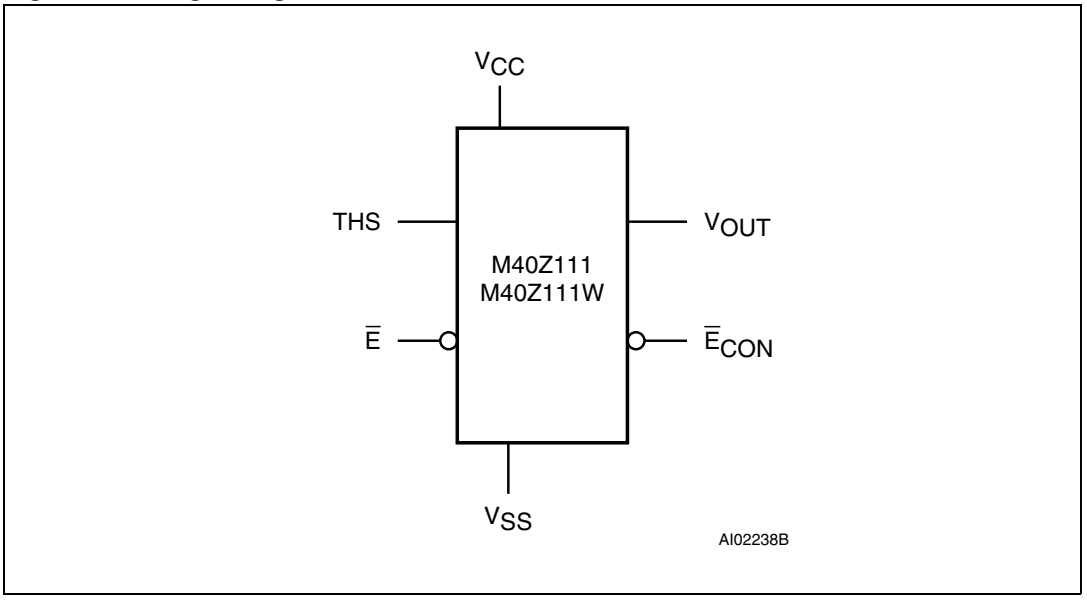

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Table 1. Signal names

THS	Threshold select input
$\overline{E}$	Chip enable input
$\overline{E}_{CON}$	Conditioned chip enable output
V_{OUT}	Supply voltage output
V_{CC}	Supply voltage
V_{SS}	Ground
NC	Not connected internally

Figure 2. SOIC28 connections

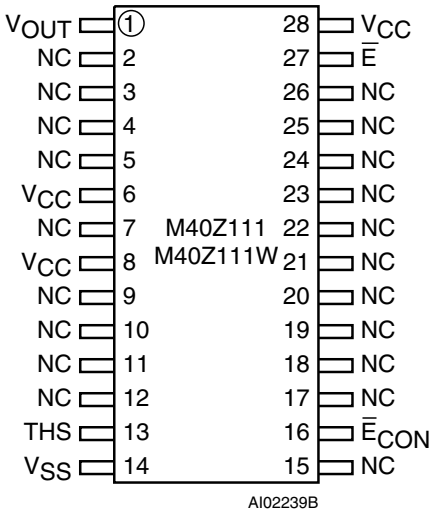

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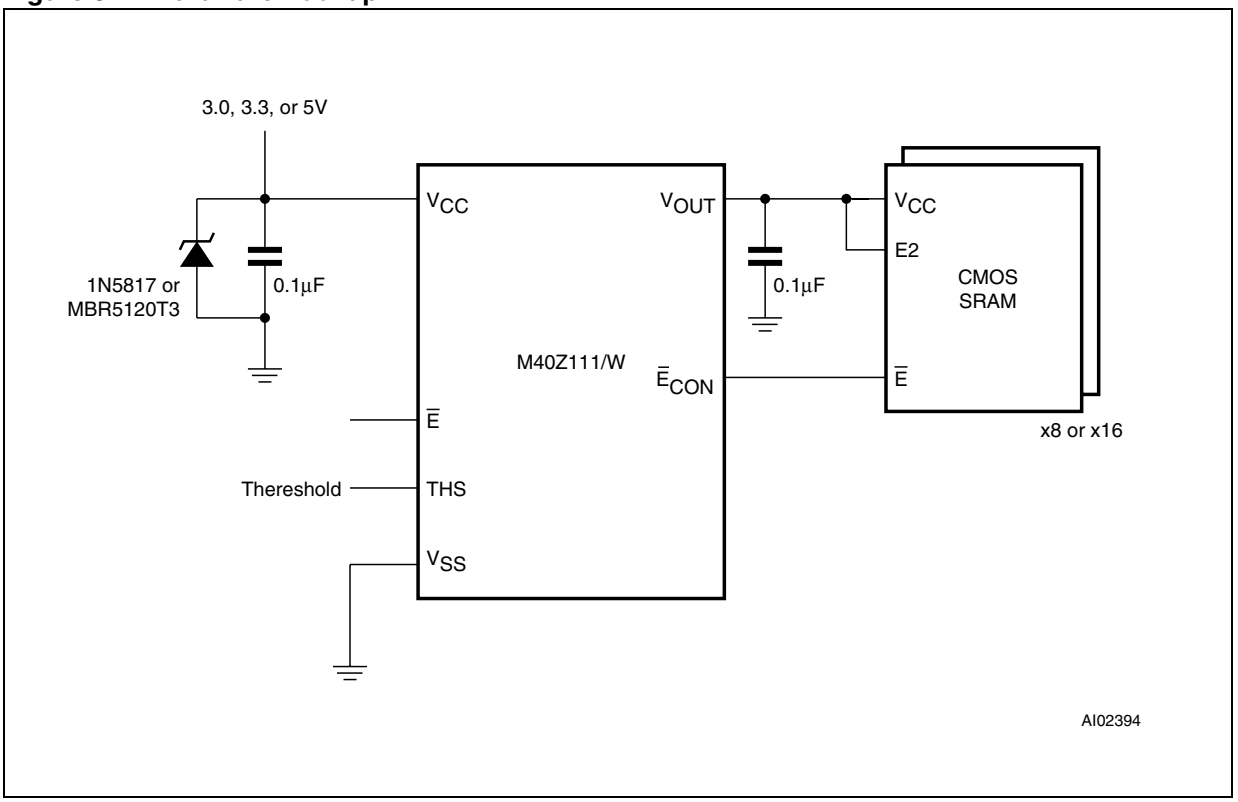
Figure 3. Hardware hookup



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2 Operation

The M40Z111/W, as shown in *Figure 3 on page 7*, can control up to two standard low-power SRAMs. These SRAMs must be configured to have the chip enable input disable all other input signals. Most slow, low-power SRAMs are configured like this, however many fast SRAMs are not. During normal operating conditions, the conditioned chip enable ($\overline{E}_{CON}$) output pin follows the chip enable ($\overline{E}$) input pin with timing shown in *Table 2 on page 10*. An internal switch connects V_{CC} to V_{OUT}. This switch has a voltage drop of less than 0.3V (I_{OUT1}).

When V_{CC} degrades during a power failure, $\overline{E}_{CON}$ is forced inactive independent of $\overline{E}$. In this situation, the SRAM is unconditionally write protected as V_{CC} falls below an out-of-tolerance threshold (V_{PFD}). The power fail detection value associated with V_{PFD} is selected by the THS pin and is shown in *Table 6 on page 14*.

Note: ***Note:*** *The THS pin must be connected to either V_{SS} or V_{OUT}.*

If chip enable access is in progress during a power fail detection, that memory cycle continues to completion before the memory is write protected. If the memory cycle is not terminated within time t_{WP}, $\overline{E}_{CON}$ is unconditionally driven high, write protecting the SRAM.

A power failure during a write cycle may corrupt data at the currently addressed location, but does not jeopardize the rest of the SRAM's contents. At voltages below V_{PFD} (min), the user can be assured the memory will be write protected provided the V_{CC} fall time exceeds t_F.

As V_{CC} continues to degrade, the internal switch disconnects V_{CC} and connects the internal battery to V_{OUT}. This occurs at the switchover voltage (V_{SO}). Below the V_{SO}, the battery provides a voltage V_{OHB} to the SRAM and can supply current I_{OUT2} (see *Table 6 on page 14*). When V_{CC} rises above V_{SO}, V_{OUT} is switched back to the supply voltage. Output $\overline{E}_{CON}$ is held inactive for t_{ER} (200ms maximum) after the power supply has reached V_{PFD}, independent of the $\overline{E}$ input, to allow for processor stabilization (see *Figure 5 on page 9*).

2.1 Data retention lifetime calculation

Most low power SRAMs on the market today can be used with the M40Z111/W NVRAM SUPERVISOR. There are, however some criteria which should be used in making the final choice of which SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M40Z111/W and SRAMs to be “Don't Care” once V_{CC} falls below V_{PFD} (min). The SRAM should also guarantee data retention down to V_{CC} = 2.0V. The chip enable access time must be sufficient to meet the system needs with the chip enable propagation delays included. If the SRAM includes a second chip enable pin (E2), this pin should be tied to V_{OUT}. If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0V.

Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use. The data retention current value of the SRAMs can then be added to the I_{CCDR} value of the M40Z111/W to determine the total current requirements for data retention.

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The available battery capacity for the SNAPHAT® of your choice can then be divided by this current to determine the amount of data retention available (see *Table 11 on page 19*). For more information on Battery Storage Life refer to the Application Note AN1012.

Figure 4. Power down timing

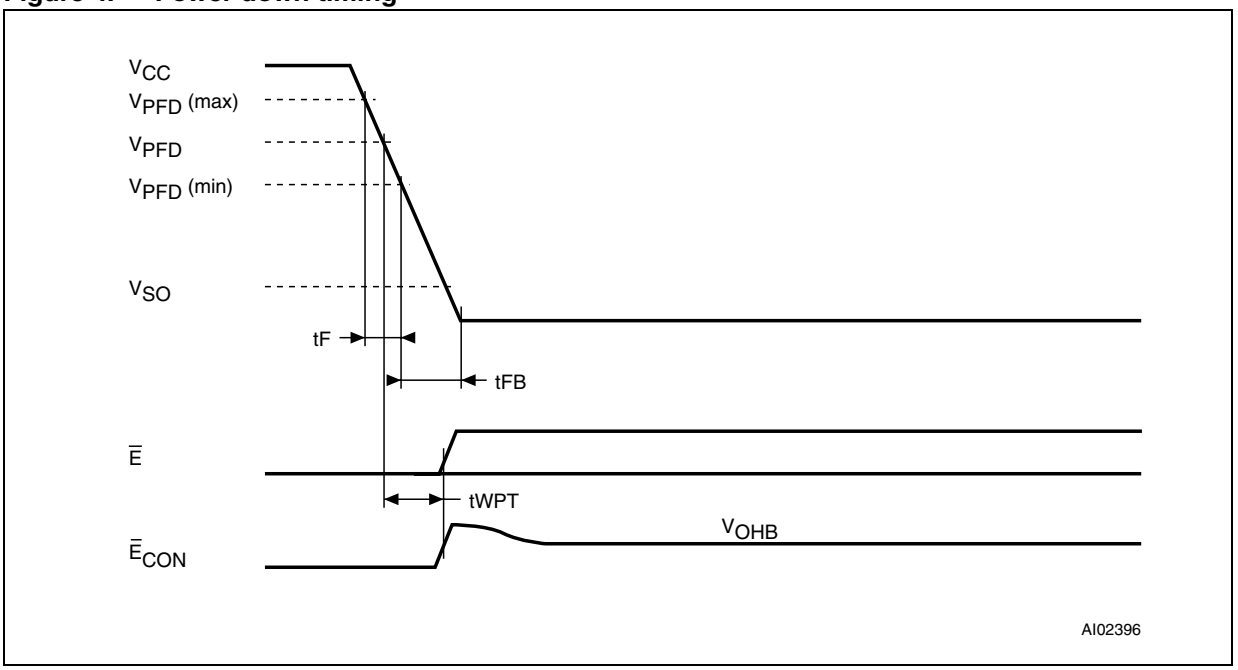

Figure 5. Power up timing

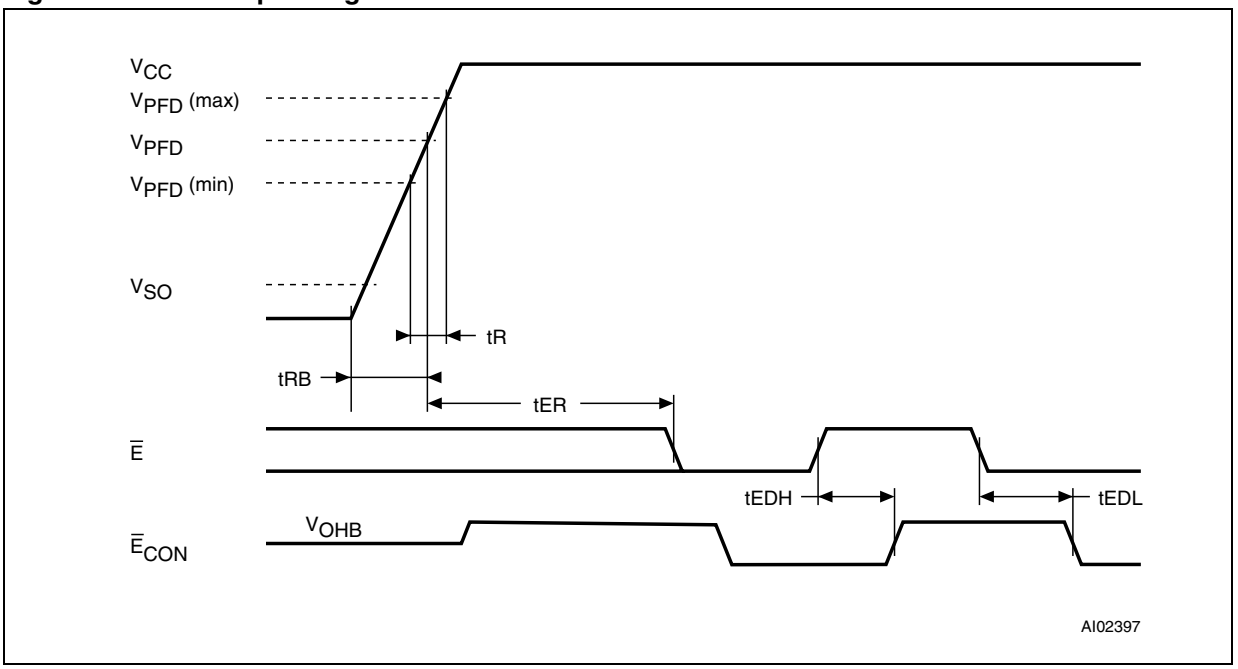

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Table 2. Power down/up AC characteristics

Symbol	Parameter[1]		Min	Max	Unit
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time		300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} fall time		10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time		10		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time		1		µs
t_{EDL}	Chip enable propagation delay	M40Z111		15	ns
		M40Z111W		20	ns
t_{EDH}	Chip enable propagation delay	M40Z111		10	ns
		M40Z111W		20	ns
t_{ER}[4]	Chip enable recovery		40	200	ms
t_{WPT}	Write protect time	M40Z111	40	150	µs
		M40Z111W	40	250	µs

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 4.5 to 5.5V or 2.7 to 3.6V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.
4. t_{ER} (min) = 20ms for industrial temperature range - grade 6 device.

2.2 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (as shown in *Figure 6*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

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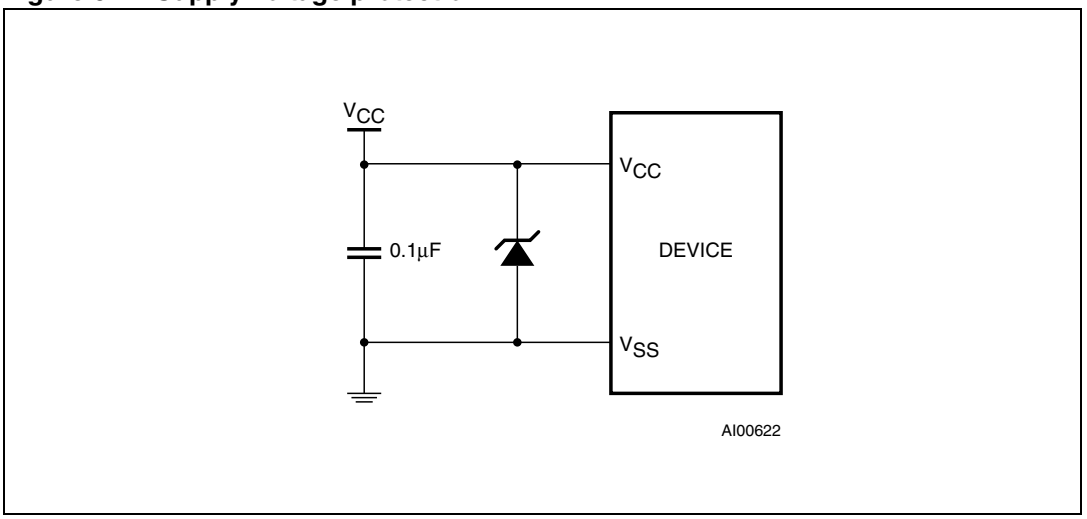
Figure 6. Supply voltage protection



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3 Maximum rating

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_A	Ambient operating temperature	Grade 6	–40 to 85	°C
T_{STG}	Storage temperature (V_{CC} off)	SNAPHAT®	–40 to 85	°C
		SOIC	–55 to 125	°C
T_{SLD}(1)	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages		–0.3 to V_{CC} +0.3	V
V_{CC}	Supply voltage	M40Z111	–0.3 to 7.0	V
		M40Z111W	–0.3 to 4.6	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. For SO package, lead-free (Pb-free) lead finish: reflow at peak temperature of 260°C (total thermal budget not to exceed 245°C for greater than 30 seconds).

Caution: Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.

Caution: Do NOT wave solder SOIC to avoid damaging SNAPHAT sockets.

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4 DC and AC parameters

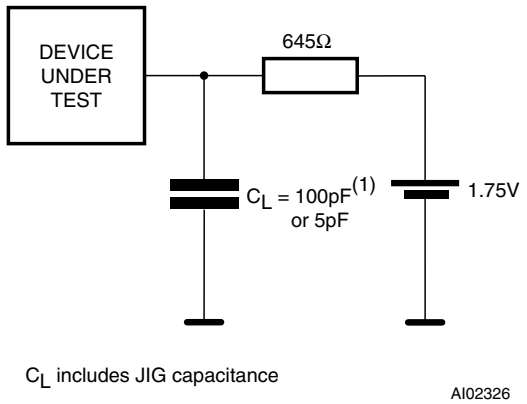
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in *Table 4: DC and AC measurement conditions*. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 4. DC and AC measurement conditions

Parameter	M40Z111	M40Z111W
V_{CC} supply voltage	4.5 to 5.5V	2.7 to 3.6V
Ambient operating temperature	–40 to 85°C	–40 to 85°C
Load capacitance (C_L)	100pF	50pF
Input rise and fall times	≤ 5ns	≤ 5ns
Input pulse voltages	0 to 3V	0 to 3V
Input and output timing ref. voltages	1.5V	1.5V

Note: Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. AC testing load circuit



1. 50pF for M40Z111W.

Table 5. Capacitance

Symbol	Parameter(1)(2)	Min	Max	Unit
C_{IN}	Input capacitance		8	pF
C_{OUT}(3)	Output capacitance		10	pF

1. Effective capacitance measured with power supply at 5V (M40Z111) or 3.3V (M40Z111W); sampled only, not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs deselected

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Table 6. DC characteristics

Sym	Parameter	Test condition(1)	M40Z111			M40Z111W			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{CC}	Supply current	Outputs open		3	6		2	4	mA
I_{CCDR}	Data retention mode current				150			150	nA
I_{LI}	Input leakage current	$0V \le V_{IN} \le V_{CC}$			±1			±1	µA
I_{LO}(2)	Output leakage current	$0V \le V_{OUT} \le V_{CC}$			±1			±1	µA
I_{OUT1}	V_{OUT} current (active)	$V_{OUT} > V_{CC} -0.3$			160			100	mA
		$V_{OUT} > V_{CC} -0.2$			100			65	mA
I_{OUT2}	V_{OUT} current (battery back-up)	$V_{OUT} > V_{BAT} -0.3$		100			100		µA
V_{BAT}	Battery voltage		2.0	3.0	3.5	2.0	3.0	3.5	V
V_{IH}	Input high voltage		2.2		V_{CC} + 0.3	2.0		V_{CC} + 0.3	V
V_{IL}	Input low voltage		–0.3		0.8	–0.3		0.8	V
V_{OH}	Output high voltage	$I_{OH} = –2.0mA$	2.4			2.4			V
V_{OHB}	V_{OH} battery back-up	$I_{OUT2} = –1.0µA$	2.0	2.9	3.6	2.0	2.9	3.6	V
V_{OL}	Output low voltage	$I_{OL} = 4.0mA$			0.4			0.4	V
THS	Threshold select voltage		V_{SS}		V_{OUT}	V_{SS}		V_{OUT}	V
V_{PFD}	Power-fail deselect voltage (THS = V_{SS})		4.50	4.60	4.75	2.80	2.90	3.00	V
	Power-fail deselect voltage (THS = V_{OUT})		4.20	4.35	4.50	2.50	2.60	2.70	V
V_{SO}	Battery back-up switchover voltage			3.0			V_{PFD} – 100mV		V

1. Valid for ambient operating temperature: $T_A = –40$ to 85°C; $V_{CC} = 4.5$ to 5.5V or 2.7 to 3.6V (except where noted).
2. Outputs deselected.

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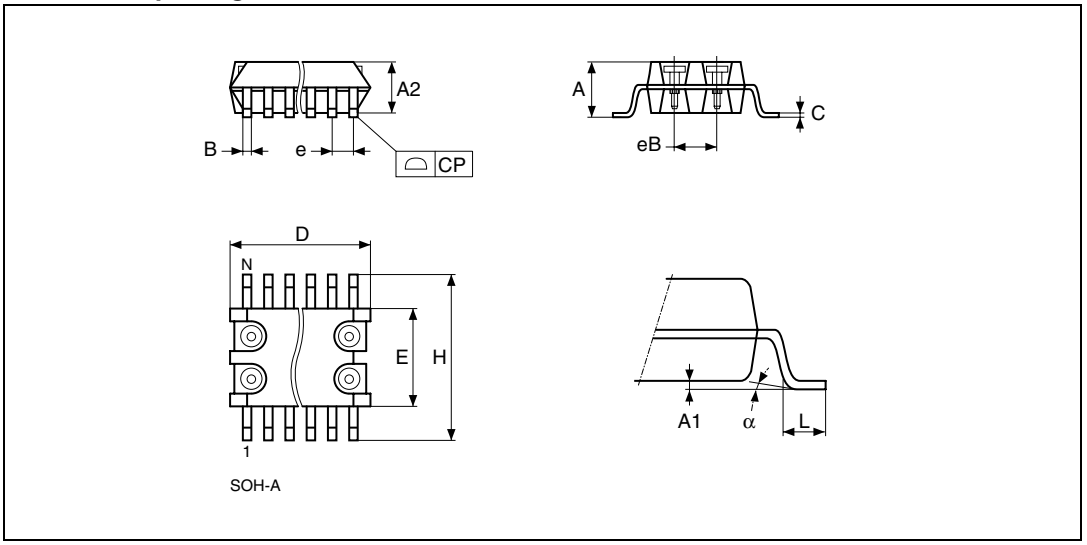
5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 8. SOH28 – 28-lead plastic small outline, 4-socket battery SNAPHAT, package outline



Note: Drawing is not to scale.

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Table 7. SOH28 – 28-lead plastic small outline, battery SNAPHAT, pack. mech. data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			3.05			0.120
A1		0.05	0.36		0.002	0.014
A2		2.34	2.69		0.092	0.106
B		0.36	0.51		0.014	0.020
C		0.15	0.32		0.006	0.012
D		17.71	18.49		0.697	0.728
E		8.23	8.89		0.324	0.350
e	1.27	–	–	0.050	–	–
eB		3.20	3.61		0.126	0.142
H		11.51	12.70		0.453	0.500
L		0.41	1.27		0.016	0.050
a		0°	8°		0°	8°
N	28			28		
CP			0.10			0.004

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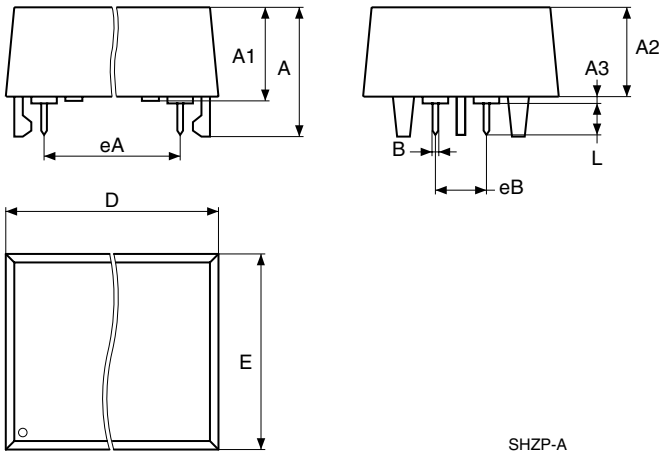
Figure 9. 4-pin SNAPHAT housing for 48mAh battery, package outline



Note: Drawing is not to scale.

Table 8. 4-pin SNAPHAT housing for 48mAh battery, package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			9.78			0.385
A1		6.73	7.24		0.265	0.285
A2		6.48	6.99		0.255	0.275
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		14.22	14.99		0.560	0.590
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

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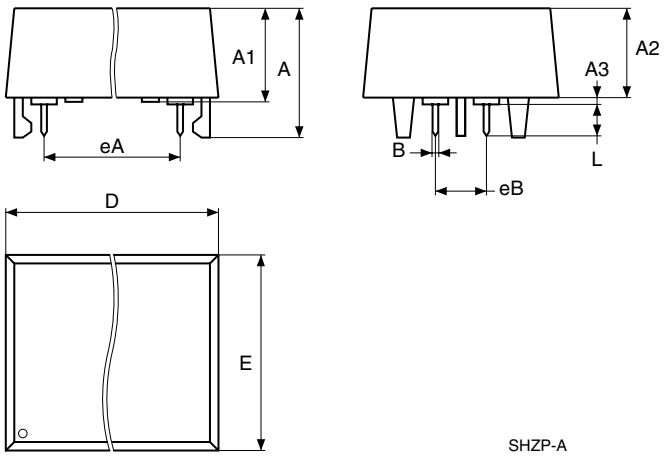
Figure 10. 4-pin SNAPHAT housing for 120mAh battery, package outline



Note: Drawing is not to scale.

Table 9. 4-pin SNAPHAT housing for 120mAh battery, package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	0.335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	0.710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

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6 Part numbering

Table 10. Ordering information scheme

Example: M40Z 111W MH 6 E

Device type

M40Z

Supply voltage and write protect voltage

111 = V_{CC} = 4.5 to 5.5V; V_{PFD} = 4.3 to 4.5V

THS = V_{SS} = 4.5 ≤ V_{PFD} ≤ 4.75V

THS = V_{OUT} = 4.2 ≤ V_{PFD} ≤ 4.5V

111W = V_{CC} = 2.7 to 3.6V; V_{PFD} = 2.6 to 2.7V

THS = V_{SS} = 2.8 ≤ V_{PFD} ≤ 3.0V

V_{CC} = 2.7 to 3.3V

THS = V_{OUT} = 2.5 ≤ V_{PFD} ≤ 2.7V

Package

MH(1) = SOH28

Temperature range

6 = –40 to 85°C

Shipping method for SOIC

E = Lead-free ECOPACK® package, tubes

F = Lead-free ECOPACK® package, tape & reel

1. The SOIC package (SOH28) requires the battery package (SNAPHAT®) which is ordered separately under the part number “M4ZXX-BR00SHX” in plastic tubes or “M4ZXX-BR00SHXTR” in tape & reel form.

Caution: Do not place the SNAPHAT battery package “M4ZXX-BR00SH” in conductive foam as this will drain the lithium button-cell battery.

For a list of available options (e.g., speed, package) or for further information on any aspect of this device, please contact the ST sales office nearest to you.

Table 11. Battery table

Part number	Description	Package
M4Z28-BR00SH1	SNAPHAT housing for 48mAh battery	SH
M4Z32-BR00SH1	SNAPHAT housing for 120mAh battery	SH

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7 Revision history

Table 12. Document revision history

Date	Revision	Changes
Sep-2000	1	First Draft Issue
14-Sep-2001	2	Reformatted, TOC added, changed DC Characteristics (*Table 6*); changed battery, ind. temperature information (*Table 3*, *2*, *10*, *11*, *Figure 9*, *10*); Corrected SOIC label (*Figure 2*); added E2 to Hookup (*Figure 3*)
13-May-2002	3	Modify reflow time and temperature footnote (*Table 3*)
12-Nov-2007	4	Reformatted document; added lead-free second level interconnect information to cover page and *Section 5: Package mechanical data*; updated *Figure 5*, *Table 3*, *10*, *11*.

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