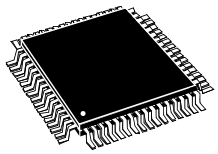
ST72682

USB 2.0 high-speed Flash dri e controller

Features

- USB 2.0 interface compatible ith mass storage de ice class
  - Integrated USB 2.0 PHY
  - Supports USB high speed and full speed
  - Suspend and Resume operations
- Mass storage controller interface MSCI
  - Supports all types of NAND Flash de ices including ST Hyni Samsung Toshiba Renesas and Micron
  - Reed-Solomon encoder/decoder on-the-fly correction 4 bytes of a 512-byte bloc
  - Flash identification support
  - Up to 21 Mbyte/s for read and 11 Mbyte/s for rite operations in dual channel
- Embedded ST7 8-bit MCU
- Supply management
  - 3.3V operation
  - Integrated 3.3 -1.8 V oltage regulator
- USB 2.0 lo -po er de ice compliant
  - Less than 100 mA during rite operation ith t o NAND Flash de ices
  - Less than 500 A in suspend mode
- Cloc management
  - Integrated PLL for generating core and USB 2.0 cloc sources using e ternal 12 MHz crystal



LQFP64 10 10

- AutoRun CDROM partition support
- Data protection
  - Write protect s itch control
  - Public/Pri ate partitions support
- Bootability support HDD mode
- Production tool de ice configurability
  - USB endor ID/product ID VID/PID serial number and USB strings ith foreign language support
  - SCSI strings
  - One or t o LED outputs
  - Ad ustable NAND Flash bus fre uency to reach highest performance
- Code update in the NAND Flash
- LQFP64 10 10 lead-free pac age
- De elopment support
  - Complete reference design including schematics BOM and gerber files
- Supports Windo s Vista XP 2000 ME Linu and MacOS. Dri ers a ailable for Windo s 98 SE

Table 1. Device summary

Features	Orderable part numbers	
	ST72682/R20	ST72682/R21
USB interface	USB 2.0 high speed	
Number of NAND de ices supported	up to 8	
Read/ rite speed	21MBps/11MBps	
Operating supply	3.0 to 3.6 V	
Operating Temperature	0 C to +70 C	
Pac age	LQFP64 10 10 / die form	

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1 Introduction

The ST72682 is a USB 2.0 high-speed Flash dri e controller. The USB 2.0 high-speed interface includes PHY and function and supports USB 2.0 mass storage de ice class.

The Mass storage controller interface MSCI combined ith the Reed-Solomon encoder/decoder on-the-fly correction 4 bytes on 512-byte data bloc s pro ides a fle ible high transfer rate solution for interfacing a ide of range NAND Flash memory de ices.

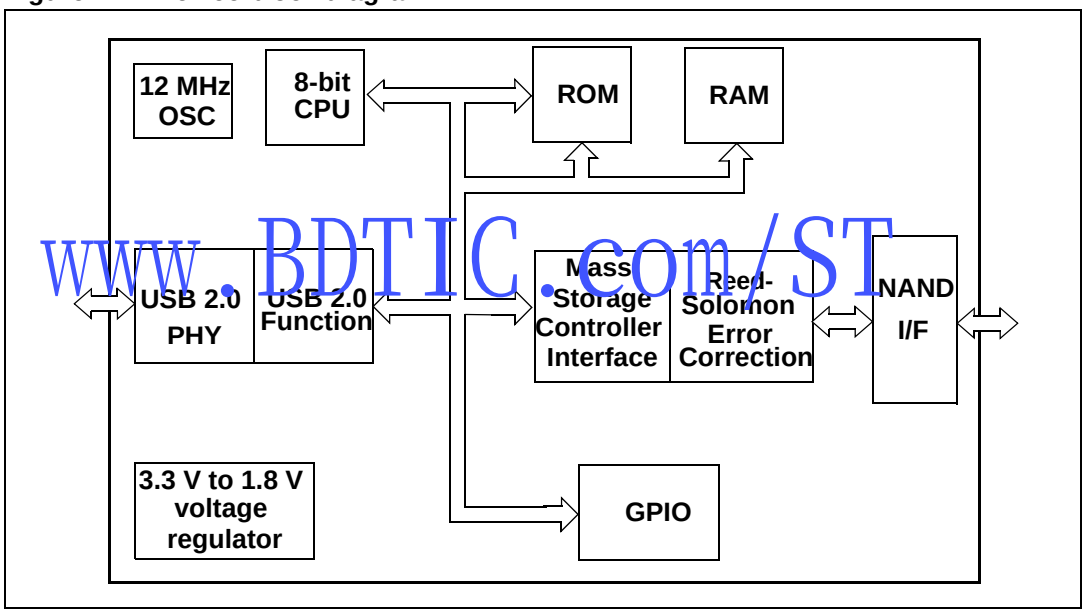
The internal 60 MHz PLL dri en by the 12 MHz oscillator is used to generate the 480 MHz fre uency re uired for the USB 2.0 PHY.

The ST7 8-bit CPU runs the application program from the internal ROM and RAM. USB data and patch code are stored in internal RAM.

The I/O ports pro ide allo to connect EEPROM LEDs and a rite protect s itch control.

The internal 3.3 to 1.8 V oltage regulator pro ides the 1.8 V supply oltage to the digital part of the circuit.

Figure 1. Device block diagram



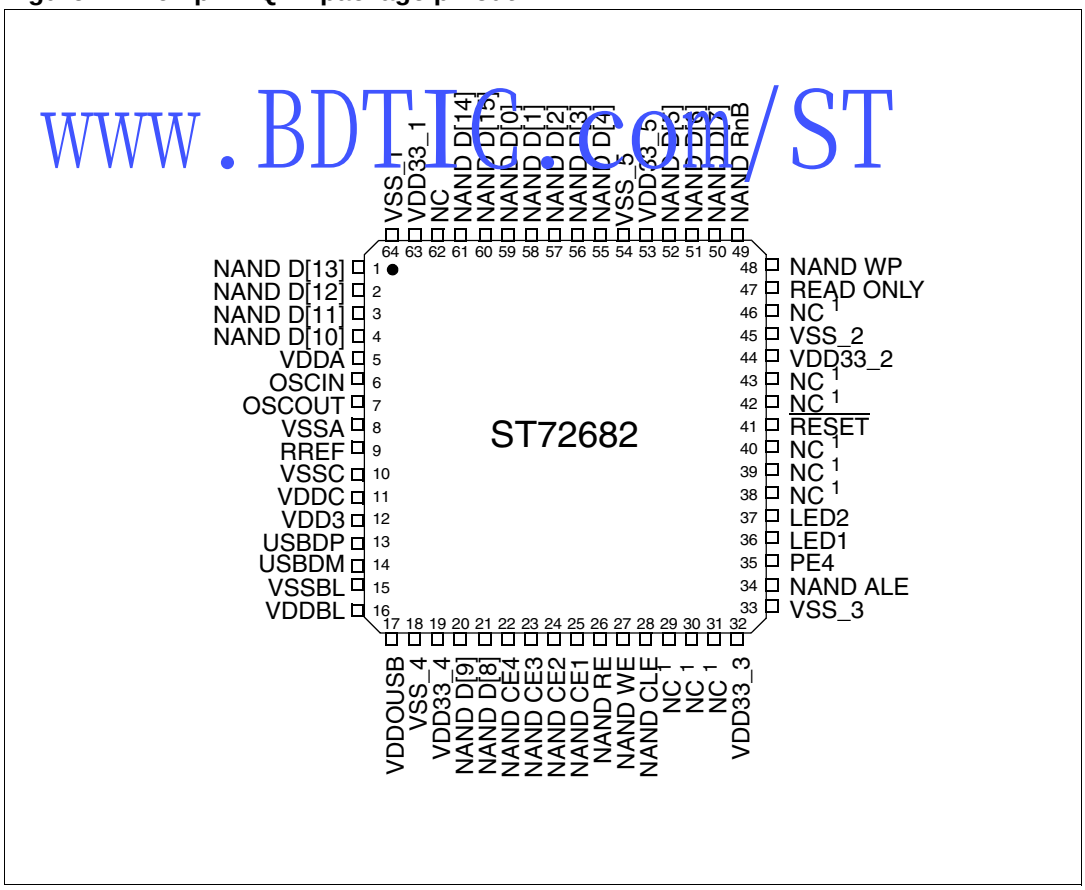
2 Pin description

Figure 2 sho s the LQPF64 pac age pinout hile *Table 2* *Table 3* *Table 4* *Table 5* and *Table 6* gi e the pin description.

The legend and abbre iations used in these tables are the follo ing

- Type
  - I input
  - O output
  - S supply
- Input le el A Dedicated analog input
- In/Output le el
  - C_T CMOS $0.3V_{DD}/0.7V_{DD}$ ith input trigger
  - T_T TTL 0.8V / 2V ith Schmitt trigger
- Output le el
  - D8 8mA dri e
  - D4 4mA dri e
  - D2 2mA dri e

Figure 2. 64-pin LQFP package pinout



1. Must remain NOT connected in the application.

Table 2. Power supply pins

Pin LQFP64	Pin name	Type	Description
64	VSS_1	S	Ground
63	VDD33_1	S	I/Os and regulator supply oltage
45	VSS_2	S	Ground
44	VDD33_2	S	I/Os and regulator supply oltage
33	VSS_3	S	Ground
32	VDD33_3	S	I/Os and regulator supply oltage
18	VSS_4	S	Ground
19	VDD33_4	S	I/Os and regulator supply oltage
54	VSS_5	S	Ground
53	VDD33_5	S	I/Os and regulator supply oltage
17	VDDOUSB	O	USB2 PHY OSC and PLL po er supply output 1.8V

Table 3. Control and system

Pin LQFP64	Pin name	Type	Power	Level		Description
				Input	Output	
47	RESET	I/O	3.3	C_T		Reset input th filter th internal pull-up

Table 4. USB 2.0 Interface

Pin LQFP64	Pin name	Type	Description
16	VDDBL	S	Supply oltage for buffers and deserialisation flip flops 1.8 V
15	VSSBL	S	Ground for buffers and deserialisation flip flops 1.8 V
14	USBDM	I/O	USB2 DATA -
13	USBDP	I/O	USB2 DATA +
12	VDD3	S	Supply oltage for the FS compliance 3.3 V
11	VDDC	S	Supply oltage for DLL XOR tree 1.8 V
10	VSSC	S	Ground for DLL XOR tree 1.8 V
9	RREF	I/O	Ref. resistor for integrated impedance process adaptation 11.3 Ohms 1% Pull Do n

Table 5. USB 2.0 and core clock system

Pin LQFP64	Pin name	Type	Description
8	VSSA	S	Ground for oscillator PLL 1.8 V
7	OSCOUT	O	12MHz oscillator output
6	OSCIN	I	12MHz oscillator input
5	VDDA	S	Supply oltage for oscillator PLL 1.8 V

Table 6. General Purpose I/O ports / Mass Storage I/Os

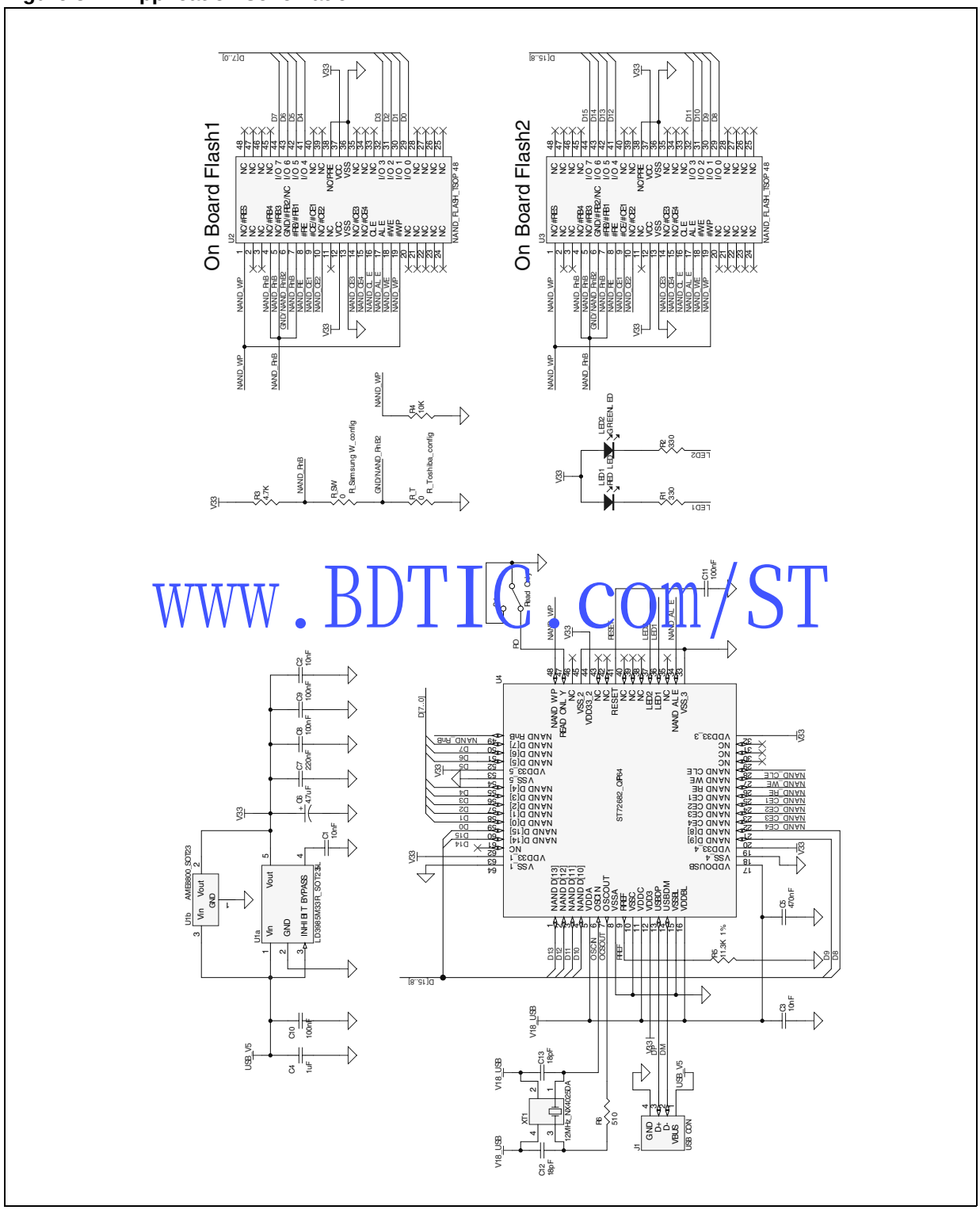
Pin LQFP64	Pin name	Type	Level		Main function (after reset)
			Input	Outputs	
59	NAND D[0]	I/O	TT	D4	NAND data [0]
58	NAND D[1]	I/O	TT	D4	NAND data [1]
57	NAND D[2]	I/O	TT	D4	NAND data [2]
56	NAND D[3]	I/O	TT	D4	NAND data [3]
55	NAND D[4]	I/O	TT	D4	NAND data [4]
52	NAND D[5]	I/O	TT	D4	NAND data [5]
51	NAND D[6]	I/O	TT	D4	NAND data [6]
50	NAND D[7]	I/O	TT	D4	NAND data [7]
21	NAND D[8]	I/O	TT	D4	NAND data [8]
20	NAND D[9]	I/O	TT	D4	NAND data [9]
10	NAND D[10]	I/O	TT	D4	NAND data [10]
11	NAND D[11]	I/O	TT	D4	NAND data [11]
12	NAND D[12]	I/O	TT	D4	NAND data [12]
13	NAND D[13]	I/O	TT	D4	NAND data [13]
14	NAND D[14]	I/O	TT	D4	NAND data [14]
15	NAND D[14]	I/O	TT	D4	NAND data [15]
34	NAND ALE	I/O	TT	D8	NAND address latch enable
35	PE4	I/O	TT	D2	
28	NAND CLE	O	TT	D8	NAND command latch enable
27	NAND WE	O	TT	D8	NAND rite enable
26	NAND RE	O	TT	D8	NAND read enable
25	NAND CE1	O	TT	D4	NAND enable 1
24	NAND CE2	O	TT	D4	NAND enable 2
23	NAND CE3	O	TT	D4	NAND enable 3

Table 6. General Purpose I/O ports / Mass Storage I/Os (continued)

Pin	Pin name	Type	Level		Main function (after reset)
LQFP64			Input	Outputs	
22	NAND CE4	O	TT	D4	NAND enable 4
49	NAND RnB	I	TT	D2	NAND Ready/$\overline{\text{Busy}}$
48	NAND WP	O	TT	D2	NAND Write Protect
47	READ ONLY	I	TT	D2	Read-only s itch 0 Read/Write 1 Read only
	EEPROM SCL	O	TT	D2	EEPROM serial cloc
37	LED2	O	TT	D8	Green LED USB access
36	LED1	O	TT	D8	Red LED NAND access

3 Application schematics

Figure 3. Application schematic



4 NAND Flash memory interface

Table 7 gi es the list of NAND Flash memory de ices compatible ith ST72682/R20 and ST72682/R21 de ices. This list is only pro ided as a guide as it is not possible to automatically guarantee support for all the additions and updates across the listed ranges of manufacturers de ices.

Table 7. Known NAND Flash memory compatibility guide for ST72682/R20 and ST72682/R21

NAND Flash part number	NAND Flash size (Mbytes or Gbytes) and type	Number of NAND Flash devices supported	
		ST72682/R20 device	ST72682/R21 device
Samsung K9F1G08U	128 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Samsung K9F2G08U	256 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Samsung K9F4G08U	512 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Samsung K9K4G08U	512 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Samsung K9W4G08U	512 MB SLC2K Dual CE	2 or 4	1 2 or 4
Samsung K9K8G08U	1 GB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Samsung K9W8G08U	1 GB SLC2K Dual CE	2 or 4	1 2 or 4
Samsung K9WAG08U	2 GB SLC2K Dual CE	2 or 4	1 2 or 4
Samsung K9NBG08U	4 GB SLC2K Quad CE	2	1 or 2
Samsung K9G4G08U	512 MB MLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Samsung K9L8G08U	1 GB MLC2K Single CE	2 4 6 or 8	1 2 4 6 or 8
Samsung K9HAG08U	2 GB MLC2K Dual CE	2 or 4	1 2 or 4
Samsung K9MBG08U	4 GB MLC2K Quad CE	2	1 or 2
Toshiba TH58NVG0S3	128 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Toshiba TH58NVG1S3	256 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Toshiba TH58NVG2S3	512 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Toshiba TH58NVG1D4	256 MB MLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Toshiba TH58NVG2D4	512 MB MLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Toshiba TH58NVG3D4	1 GB MLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
ST NAND01GW3B	128 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
ST NAND02GW3B	256 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
ST NAND04GW3B	512 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
ST NAND08GW3B	1 GB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
ST NAND04GW3C	512 MB MLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Hyni HY27UF081G2M	128 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Hyni HY27UG082G2M	256 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Hyni HY27UG084G2M	512 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Hyni HY27UH084G5M	512 MB SLC2K Dual CE	2 or 4	1 2 or 4

Table 7. Known NAND Flash memory compatibility guide for ST72682/R20 and ST72682/R21

NAND Flash part number	NAND Flash size (Mbytes or Gbytes) and type	Number of NAND Flash devices supported	
		ST72682/R20 device	ST72682/R21 device
Hyni HY27UH088G2M	1 GB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Hyni HY27UT084G2M	512 MB MLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Hyni HY27UU088G5M	1 GB MLC2K Dual CE	2 or 4	1 2 or 4
Micron 29F2G08AA	256 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Micron 29F4G08BA	512 MB SLC2K Single CE	1 2 4 6 or 8	1 2 4 6 or 8
Micron 29F8G08FA	1 GB SLC2K Dual CE	2 or 4	1 2 or 4

4.1 NAND Flash error correction

No NAND Flash memory arrays are guaranteed by manufacturers to be error-free. Error occurrence depends on the Flash cell type MLC or SLC .

The ST72682 embeds hard are and firm are mechanisms to correct the errors.

4.1.1 Hardware error correction

The ST72682 embeds a Reed-Solomon algorithm-based hard are cell. This cell directly manages 512-byte data pac ets on the NAND I/O system.

Based on the data pac et content the cell generates an 80-bit Error Correction Code ECC consisting of 8 ords each containing 10 bits.

During rite operations to NAND memory the 512-bytes of data and the ECC are stored together in the same page. The ECC is stored in the corresponding Redundant Area RA using 10 bytes.

During read operations the 512-bytes of data and the 8 ECC ords are read bac and are passed through the Reed-Solomon cell for decoding. The cell allo s the correction of 4 symbols in this 520-symbol pac et 512 symbols from data + 8 symbols from ECC .

The hard are cell gi es three possible results

- No error detected the data pac et can be used as it is.
- Correctable error detected the corrected data are a ailable in a specific 512-byte buffer in the Reed-Solomon cell and are ready to be used.
- Uncorrectable error detected data corruption cannot be repaired.

4.1.2 Firmware error management

The firm are defines the error correction possibilities ith the corrected data pac et.

When data cannot be repaired the bloc is considered as a bad bloc and is replaced by another one. See *Section 4.2* for further information on bad bloc management.

4.2 Bad block management

NAND memory manufacturers deli er their de ices ith factory-mar ed bad bloc s. This mar ing depends on the manufacturer and the NAND memory type page size memory technology etc. . The ST72682 supports all bad bloc mar ings currently a ailable on the mar et.

4.2.1 Bad Block identification

During firm are initialization the MCU scans the entire NAND memory configuration to identify bad bloc s.

A bad bloc is defined as follo s

- Fi e different bloc status bytes are considered 4 status bytes from page 0 and 1 from an other page page 127 for MLC NAND page 1 for SLC NAND .
- The considered bloc is mar ed as a bad bloc if one out of these fi e bytes contains at least four bits set to 0 .

4.2.2 Bad block replacement

The firm are or s on groups of 1024 bloc s called zones. A complete NAND configuration can contain se eral zones

- Each zone is described in a Loo Up Table LUT containing 1024 entries. A LUT is composed of 3 parts used bloc s free bloc s and bad bloc s.
- The bad bloc s part contains as many entries as the number of bad bloc s identified in that zone.
- The used bloc s part can ha e a size of 1000 900 or 500 entries. This size is configurable and also depends on the number of identified bad bloc s.
- The free bloc s part contains the remaining entries.

The used bloc s part is used to do a correspondence bet een NAND bloc s and logical address ranges.

This system allo s all bad bloc s to be mas ed from the Host. As a result bad bloc s are ne er seen. Only a range of logical addresses are isible hich correspond to the sum of the used bloc s part of all zones.

4.2.3 Late Fail block

During normal application life defects may appear in the NAND memory. Under certain conditions these defects are not correctable and the corresponding bloc is declared as bad .

In this case ne bad bloc s are identified in the bad bloc s part of the LUT and replaced by ne bloc s from the free bloc s part.

4.3 Wear levelling

During normal application life the NAND memory is ritten and erased at bloc le el many times. The NAND de ice is guaranteed for a limited number of rite operations about 100 000 cycles . As a conse uence the controller must eep rite/erase operations to a minimum for any indi idual bloc .

A method to limit these cycles is to use a Wear Le elling scheme bet een all NAND memory bloc s.

LUT usage

The LUT is used for transfers bet een a logical address range and a bloc . It contains free bloc s hich are used in the ear le elling scheme.

During rite command treatment the firm are calculates the zones bloc s and pages for data rite access. In a bloc rite operation the firm are applies the follo ing scheme to a oid bloc earing

- The least recently-used bloc is chosen from the free bloc part of the LUT.
- Valid data from the old bloc is copied to the ne bloc .
- Ne data from the rite command is ritten to the ne bloc .
- The old bloc is erased.
- The LUT is updated after identifying the ne bloc in the used bloc part and the old bloc in the free bloc part.

Using this scheme a logical address range doesn t correspond to a constant bloc . A rite command repeated se eral times to the same logical address rites physically into different bloc s.

This method shares the earing e enly across all bloc s of the concerned zone.

4.4 NAND Flash interface configuration

Applications based on ST72682 can be configured through a dedicated PC soft are tool.

The NAND memory RE and WE signals fre uencies can be independently configured to 30 MHz 20 MHz 15 MHz 12 MHz and 10 MHz.

The logical size reduction factor can be configured to 90% or 50% in the e ent of ha ing too many bad bloc s. this option resizes the used bloc s part of the LUT to 900 or 500.

5 Mass storage implementation

5.1 USB characteristics

The ST72682 is compliant ith USB 2.0 specification.

It is able to operate in both high speed and full speed modes using a bidirectional control endpoint 0 and a bidirectional bul endpoint 2.

It automatically recognizes the speed to use on the bus by a process of negotiation ith USB Host.

5.2 BOT/SCSI implementation

5.2.1 BOT specification

The USB Mass Storage Class Bul Only Transport BOT specification ersion 1.0 is implemented. It allo s the de ice to be recognized by the host as a mass-storage USB de ice.

5.2.2 SCSI specification

Moreo er inside BOT transfers SCSI commands are encapsulated for mass storage operations.

The related specifications are SBC-2 re ision 10 SCSI Bloc Commands 2 and SPC-4 re ision 7a SCSI Primary Commands 4 .

5.2.3 Bootability specification

The USB mass storage specification for bootability re ision 1.0 is implemented.

It allo s the PC host to boot the operating system from the USB mass storage application. In this case the Host uses BOT LUN 0 logical unit number .

A specific tool must be used to format the logical dri e in order to ma e it bootable by programming the correct information.

5.3 Multi-LUN device characteristics

The application can be configured ith a dedicated PC soft are tool as a multi-LUN de ice.

In this case up to 3 different dri es are a ailable public dri e additional dri e and pri ate dri e.

Public and additional dri es can be configured as remo able dri e hard dis dri e or CD-ROM dri e.

5.3.1 Public drive

The public dri e is the default configuration in a mono-LUN mode. In this default case it is declared as a remo able dri e.

The public dri e is mandatory and can not be remo ed from the configuration. By customization using PC soft are it can be declared as a remo able dri e a CD-ROM dri e or a hard dis dri e.

This dri e is the LUN 0 in BOT commands.

5.3.2 Private drive

The Pri ate dri e is optional. Its type is remo able dri e and is not configurable.

This dri e is protected by pass ord and cannot be directly accessed through the PC operating system. A PC soft are tool is necessary to send a command ith the pass ord to unloc the de ice. The de ice is then open and accessible by the PC operating system until reset or reception of a ne command to loc the dri e.

This dri e is the LUN 1 in BOT commands.

5.3.3 Additional drive

The additional dri e is optional. Its type can be remo able dri e hard dis dri e or CD-ROM dri e .

This dri e is LUN 1 in BOT commands if the pri ate dri e option is not acti e and is LUN 2 if the pri ate dri e option is acti e.

5.3.4 CD-ROM considerations

When a dri e is declared as CD-ROM the ST72682/R21 manages this dri e ith a logical bloc size of 2 Kbytes. To be correctly recognized by the host it is preferable to build a CDFS partition on this CD-ROM. See the ST7268 Production Tool User Manual for more information.

Note that the ST72682/R20 doesn t consider the CD-ROM partition as a specific case. The logical bloc size is 512 bytes and any file system can be used.

In both cases the CD-ROM partition allo s the use of the AutoRun operating system feature. During de ice connection the CD-ROM partition is recognized and the host tries to run the application corresponding to the autorun.inf file present into this CD-ROM partition.

5.4 Mass storage interface configuration

In addition to the parameters already described as configurable in the pre ious chapters additional customizable information includes

- USB parameters VID PID all string information.
- SCSI parameters strings for in uiry commands.

6 Human interface implementation

6.1 LED behavior

The application is designed to manage 2 LEDs. This beha ior is configurable through PC dedicated soft are ST7268 Production Tool .

By default LED 1 responds to NAND memory access acti ity and LED 2 responds to USB acti ity.

Use of LED 1 is optional. When this option is not acti e LED 2 reacts to both USB and NAND memory acti ity.

6.2 Read-only switch

The READ ONLY pin of the ST72682 is an input pin to be connected to VDD or GND depending on the beha ior of the de ice.

- When this pin is connected to GND no limitations are applied on the PC command recei ed.
- When this pin is connected to VDD or unconnected the firm are filters all accesses to the NAND memory hich modify the NAND memory state rite erase etc. and returns an error to the PC.

7 Electrical characteristics

7.1 Parameter conditions

Unless other ise specified all oltages are referred to V_{SS}.

7.1.1 Minimum and maximum values

Unless other ise specified the minimum and ma imum alues are guaranteed in the orst conditions of ambient temperature supply oltage and fre uencies by tests in production on 100% of the De ices ith an ambient temperature at T_A 25 C and T_A $T_A$ma gi en by the selected temperature range .

Data based on characterization results design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization the minimum and ma imum alues refer to sample tests and represent the mean alue plus or minus three times the standard de iation mean 3Σ .

7.1.2 Typical values

Unless other ise specified typical data are based on T_A 25 C V_{DD33} 3.3 V. They are gi en only as design guidelines and are not tested.

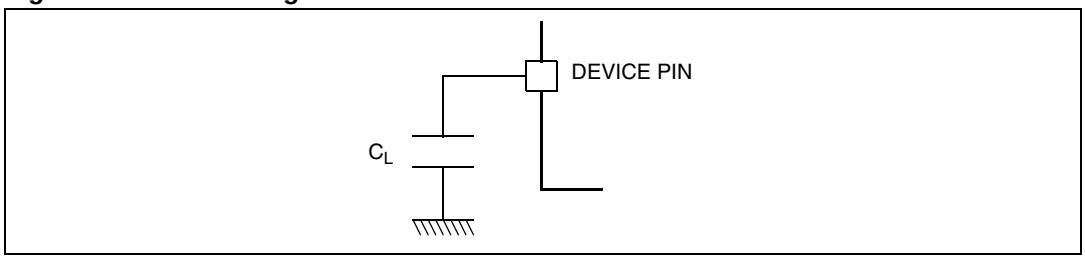
7.1.3 Typical curves

Unless other ise specified all typical cur es are gi en only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are sho n in *Figure 4*.

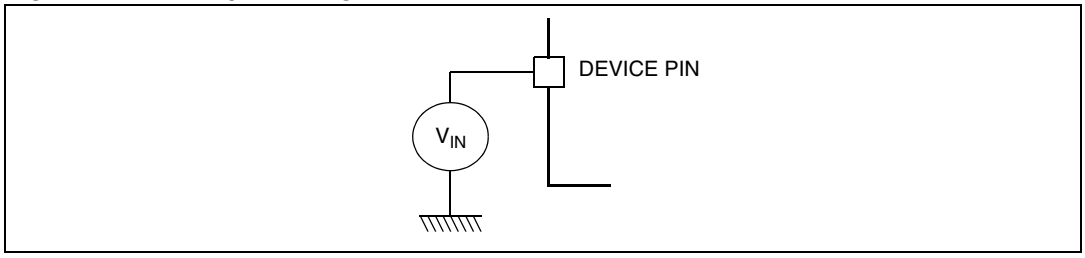
Figure 4. Pin loading conditions



7.1.5 Pin input voltage

The input oltage measurement on a pin of the de ice is described in *Figure 5*.

Figure 5. Pin input voltage



7.2 Absolute maximum ratings

Stresses abo e those listed as absolute ma imum ratings may cause permanent damage to the De ice. This is a stress rating only and functional operation of the De ice under these conditions is not implied. E posure to ma imum rating conditions for e tended periods may affect de ice reliability.

Table 8. Voltage characteristics

Symbol	Ratings	Maximum value	Unit
V_{DD33} - V_{SS}	Supply oltage	4.0	V
V_{IN} [1] [2]	Input oltage on any other pin	V_{SS} -0.3 to V_{DD33} +0.3	V
$V_{ESD\ HBM}$	Electrostatic discharge oltage Human Body Model	see *Section 7.6.3: Absolute Maximum Ratings (Electrical Sensitivity)*	

1. Directly connecting the RESET and I/O pins to V_{DD33} or V_{SS} could damage the De ice if an unintentional internal reset is generated or an une pected change of the I/O configuration occurs for e ample due to a corrupted program counter . To guarantee safe operation this connection has to be done through a pull-up or pull-do n resistor typical 4.7 Ω for RESET 10 Ω for I/Os . For the same reason unused I/O pins must not be directly tied to V_{DD33} or V_{SS}.
2. When the current limitation is not possible the V_{IN} absolute ma imum rating must be respected other ise refer to $I_{INJ\ PIN}$ specification. A positi e in ection is induced by V_{IN} V_{DD33} hile a negati e in ection is induced by V_{IN} V_{SS}.

Table 9. Current characteristics

Symbol	Ratings	Maximum value	Unit
I_{VDD33}	Total current into V_{DD33} po er lines source [1]	200	mA
I_{VSS}	Total current out of V_{SS} ground lines sin [1]	200	
I_{IO} [2]	Output current sun by any I/O D2 type	25	
	Output current sun by any I/O D4 type	35	
	Output current sun by any I/O D8 type	50	
	Output current source by any I/Os and control pin	–25	

1. All po er supply V_{DD33} and ground V_{SS} lines must al ays be connected to the e ternal supply.
2. Refer to *Table 6* for the output dri e capability of each of the I/Os.

Table 10. Thermal characteristics

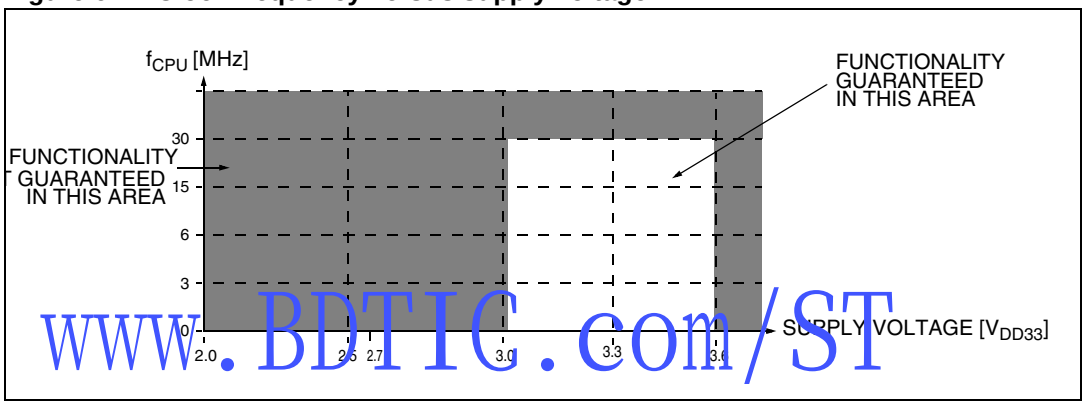
Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	C
T_{JMAX}	Ma imum unction temperature	120	C

7.3 Operating conditions

Table 11. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD33}	Po er Supply		3.0	3.6	V
T_A	Ambient temperature range		0	70	C

Figure 6. Clock frequency versus supply voltage



7.4 Supply current characteristics

Table 12. RUN and SUSPEND modes current

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current in RUN mode	f_{OSC} 12MHz	15	25	35	mA
	Supply current in SUSPEND mode	V_{DD33} 3.3V T_A +25 C	60	90	190	A

Table 13. Supply and Clock managers current

Symbol	Parameter	Conditions	Typ(1)	Max(2)	Unit
$I_{DD\ CK}$	Supply current of crystal oscillator 3		1000	2000	A

1. Typical data are based on T_A 25 C and f_{CPU} 12 MHz.
2. Data based on characterization results not tested in production.
3. Data based on characterization results done ith the e ternal components specified in *Section 7.5.1* not tested in production.

7.5 Clock and timing characteristics

Sub ect to general operating conditions for V_{DD33} f_{OSC} and T_A.

7.5.1 Crystal oscillator

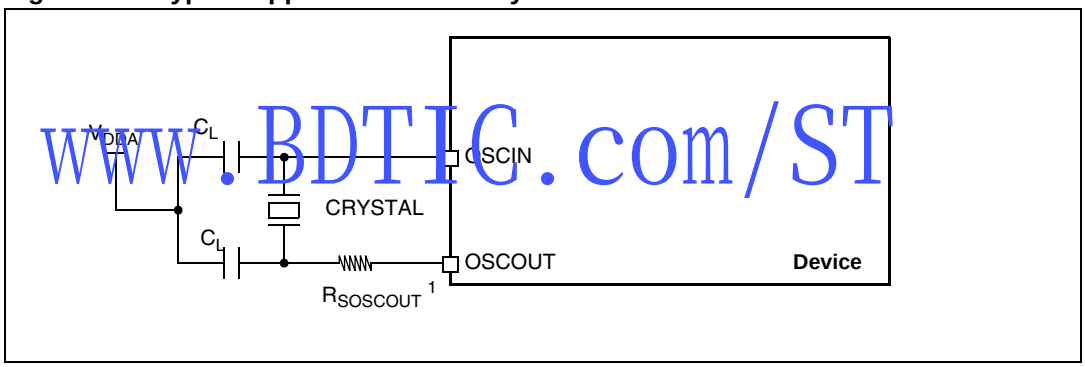
The De ice internal cloc is supplied from a crystal oscillator. All the information gi en in this paragraph are based on characterization results ith specified typical e ternal components. In the application the load capacitors ha e to be placed as close as possible to the oscillator pins in order to minimize output distortion and start-up stabilization time. Refer to the crystal manufacturer for more details fre uency pac age accuracy... .

Table 14. Clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC}	Oscillator fre uency			12		MHz
CK_{ACC}	Total crystal oscillator accuracy	Absolute alue + temperature + aging			±60	ppm
α_{OSC}	Crystal oscillator duty cycle [1]		45	50	55	%

1. The crystal oscillator duty cycle has to be ad usted through the t o C_L capacitors. Refer to the crystal manufacturer for more details.

Figure 7. Typical application with a crystal



1. Depending on the crystal po er dissipation a serial resistor $R_{sOscout}$ may be added. Refer to the crystal manufacturer for more details.

Table 15. Typical C_L and R_S values by crystal

Supplier	Typical Crystal	C_L (pF)	$R_{SOSCOUT}$ (Ω)
NDK	AT51 or AT41	16	560

7.6 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

7.6.1 Functional EMS (Electromagnetic Susceptibility)

Based on a simple running application on the product toggling 2 LEDs through I/O ports the product is stressed by t o electromagnetic e ents until a failure occurs indicated by the LEDs .

- **ESD** Electrostatic Discharge positi e and negati e is applied on all pins of the de ice until a functional disturbance occurs. This test conforms ith the IEC 1000-4-2 standard.
- **FTB** A Burst of Fast Transient oltage positi e and negati e is applied to V_{DD33} and V_{SS33} through a 100pF capacitor until a functional disturbance occurs. This test conforms ith the IEC 1000-4-4 standard.

A de ice reset allo s normal operations to be resumed. The test results are gi en in the table belo based on the EMS le els and classes defined in application note AN1709.

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component le el ith a typical application en ironment and simplified MCU soft are. It should be noted that good EMC performance is highly dependent on the user application and the soft are in particular.

Therefore it is recommended that the user applies EMC soft are optimization and pre ualification tests in relation ith the EMC le el re uested for his application.

- Soft are recommendations

  The soft are flo chart must inc ude the mar agement of runa ay conditions such as

  Corrupted program counter

  Une pected reset

  Critical Data corruption control registers...

- Pre ualification trials

  Most of the common failures une pected reset and program counter corruption can be reproduced by manually forcing a lo state on the RESET pin or the Oscillator pins for 1 second.

  To complete these trials ESD stress can be applied directly on the de ice o er the range of specification alues. When une pected beha ior is detected the soft are can be hardened to pre ent unreco erable errors occurring see application note AN1015 .

Table 16. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD33}=3.3 V T_A=+25 C f_{OSC}=12 MHz compliant ith IEC 1000-4-2	4B
V_{FFTB}	Fast transient oltage burst limits to be applied through 100pF on V_{DD33} and V_{SS33} pins to induce a functional disturbance	V_{DD33}=3.3 V T_A=+25 C f_{OSC}=12 MHz compliant ith IEC 1000-4-4	4A

7.6.2 Electromagnetic Interference (EMI)

Based on a simple application running on the product toggling 2 LEDs through the I/O ports the product is monitored in terms of emission. This emission test is in line ith the norm SAE J 1752/3 hich specifies the board and the loading of each pin.

Table 17. EMI characteristics

Symbol	Parameter	Conditions	Monitored Frequency Band	Max vs. (f_{OSC} at 12 MHz)	Unit
S_{EMI}	Pea le el	V_{DD33}=3.3 V T_A=+25 C conforming to SAE J 1752/3 [1]	0.1 to 30 MHz	20	dB V
			30 to 130 MHz	25	
			130 MHz to 1 GHz	25	
			SAE EMI Le el	4	-

1. Refer to Application Note AN1709 for data on other pac age types.

7.6.3 Absolute Maximum Ratings (Electrical Sensitivity)

Based on three different tests ESD LU and DLU using specific measurement methods the product is stressed in order to determine its performance in terms of electrical sensiti ity. For more details refer to the application note AN1181.

Electrostatic Discharge (ESD)

Electrostatic discharges a positi e then a negati e pulse separated by 1 second are applied to the pins of each sample ac co ding to each pin combination. The sample size depends on the number of supply pins in the de ice 3 parts n+1 supply pin . This test conforms to the JESD22-A114A/A115A standard.

Table 18. Absolute maximum ratings

Symbol	Ratings	Conditions	Maximum value(1)	Unit
$V_{ESD\ HBM}$	Electrostatic discharge oltage Human Body Model	T_A=+25 C	2000	V

1. Data based on characterization results not tested in production.

Static and Dynamic Latch-Up

- **LU** 3 complementary static tests are re uired on 10 parts to assess the latch-up performance. A supply o er oltage applied to each po er supply pin and a current in ection applied to each input output and configurable I/O pin are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details refer to the application note AN1181.
- **DLU** Electrostatic discharges one positi e then one negati e test are applied to each pin of 3 samples hen the micro is running to assess the latch-up performance in dynamic mode. Po er supplies are set to the typical alues the oscillator is connected as near as possible to the pins of the micro and the component is put in reset mode. This test conforms to the IEC1000-4-2 and SAEJ1752/3 standards. For more details refer to the application note AN1181.

Table 19. Electrical sensitivities

Symbol	Parameter	Conditions	Class(1)
LU	Static latch-up class	T_A=+25 C	A
DLU	Dynamic latch-up class	V_{DD33}=3.3 V f_{OSC}=12 MHz T_A=+25 C	A

1. Class description A Class is an STMicroelectronics internal specification. All its limits are higher than the JEDEC specifications that means hen a de ice belongs to Class A it e ceeds the JEDEC standard. B Class strictly co ers all the JEDEC criteria international standard .

7.7 I/O port pin characteristics

7.7.1 General characteristics

Sub ect to general operating conditions for V_{DD33} f_{OSC} and T_A unless other ise specified.

Table 20. I/O port characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input lo le el oltage [1]	TTL ports			0.16V_{DD33}	V
V_{IH}	Input high le el oltage [1]		0.85V_{DD33}			
V_{hys}	Schmitt trigger oltage hysteresis [2]		400			mV
I_L	Input lea age current	$V_{SS} \le V_{IN} \le V_{DD33}$ standard I/Os			1	A
R_{PU}	Wea pull-up e ui alent resistor [1]	V_{IN} V_{SS} V_{DD33} 3.3 V	32	50	75	Ω

1. The R_{PU} pull-up e ui alent resistor is based on a resisti e transistor. This data is based on characterization results tested in production at V_{DD33} ma .
2. Hysteresis oltage bet een Schmitt trigger s itching le els. Based on characterization results not tested in production.

Figure 8. Two typical applications with unused I/O pin

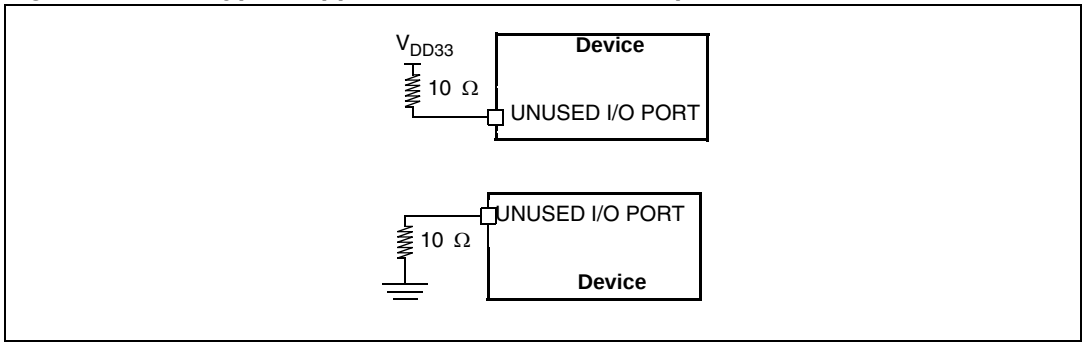


Figure 9. Typical V_{IL} and V_{IH} standard I/Os

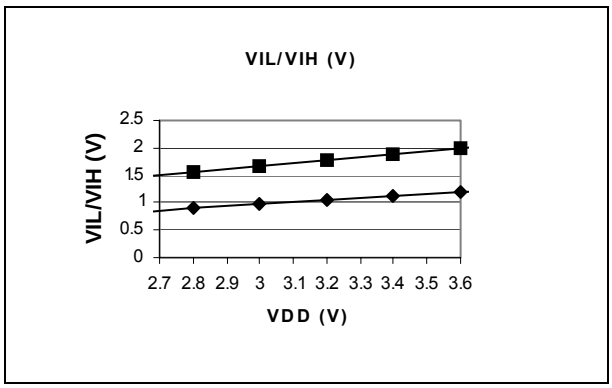
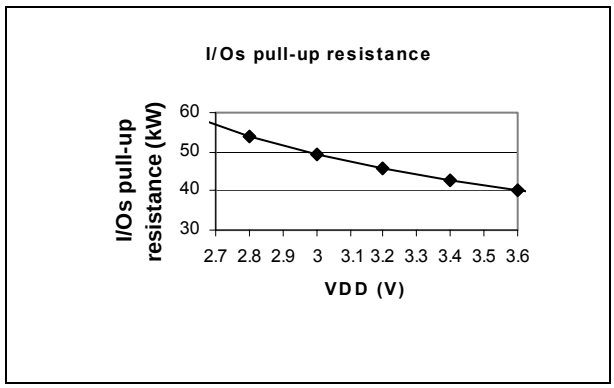


Figure 10. Typical R_{PU} vs. V_{DD33} with $V_{IN}=V_{SS}$



7.7.2 Output driving current

Sub ect to general operating conditions for V_{DD33} f_{OSC} and T_A unless other ise specified.

Table 21. Output driving current

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OL} [1]	Output lo le el oltage for a D2 I/O pin hen 8 pins are sun at same time see *Figure*	V_{DD33} 3.3 V	I_{IO} 2mA		300	mV
	Output lo le el oltage for a D4 I/O pin hen 8 pins are sun at same time see *Figure 12*		I_{IO} 4mA		400	
	Output lo le el oltage for a D8 I/O pin hen 8 pins are sun at same time see *Figure 13*		I_{IO} 8mA		500	
V_{DD33}-V_{OH} [2]	Output high le el oltage for a D2 I/O pin hen 8 pins are sourced at same time see and *Figure 14*		I_{IO} 2mA		600	mV
	Output high le el oltage for a D4 I/O pin hen 8 pins are sourced at same time see *Figure 15*		I_{IO} 4mA		600	
	Output high le el oltage for a D8 I/O pin hen 8 pins are sourced at same time see *Figure 16*		I_{IO} 8mA		600	

1. The I_{IO} current sun must al ays respect the absolute ma imum rating specified in *Section Table 9.* and the sum of I_{IO} I/O ports and control pins must not e ceed I_{VSS}.
2. The I_{IO} current sourced must al ays respect the absolute ma imum rating specified in *Section Table 9.* and the sum of I_{IO} I/O ports and control pins must not e ceed I_{VDD33}. True open drain I/O pins does not ha e V_{OH}.

Figure 11. Typical V_{OL} at V_{DD33}=3.3 V (I/O D2)

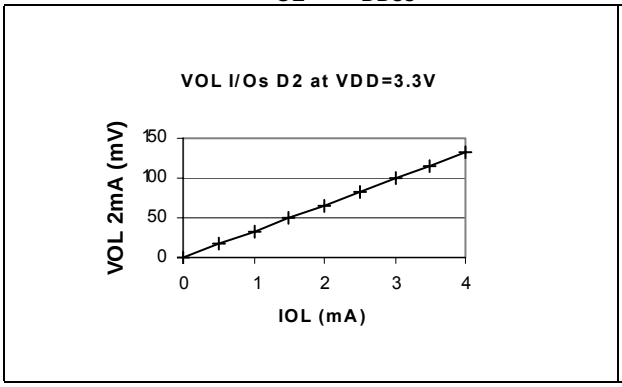


Figure 12. Typical V_{OL} at V_{DD33}=3.3 V (I/O D4)

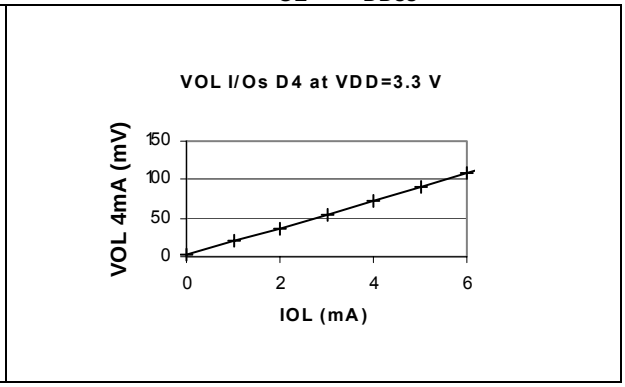


Figure 13. Typical V_{OL} at V_{DD33}=3.3 V (I/O D8)

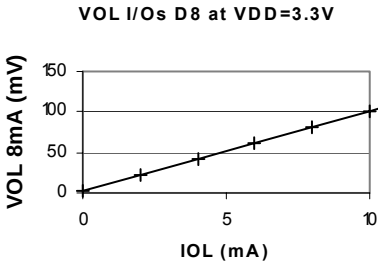


Figure 14. Typical V_{DD33}-V_{OH} vs. V_{DD33} (I/O D2)

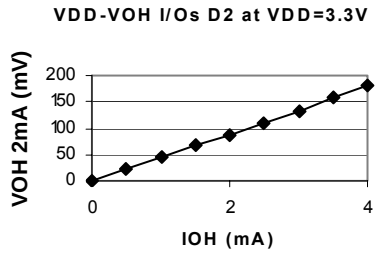


Figure 15. Typical V_{DD33}-V_{OH} vs. V_{DD33} (I/O D4)

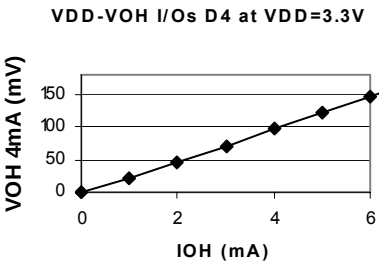
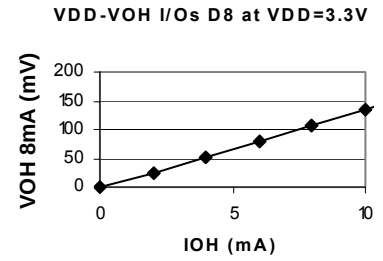


Figure 16. Typical V_{DD33}-V_{OH} vs. V_{DD33} (I/O D8)



7.8 Control pin characteristics

7.8.1 Asynchronous $\overline{\text{RESET}}$ pin

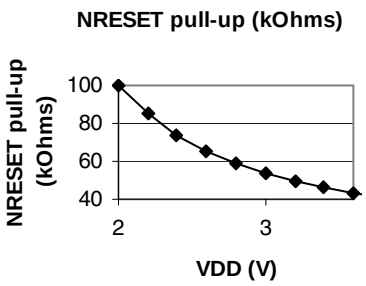
T_A ranges bet een 0 and +55 C unless other ise specified.

Table 22. Asynchronous $\overline{\text{RESET}}$ pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input lo le el oltage [1]				$0.16V_{DD33}$	V
V_{IH}	Input high le el oltage		$0.85V_{DD33}$			
V_{hys}	Schmitt trigger oltage hysteresis [1]			450		mV
R_{ON}	Pull-up e ui alent resistor	V_{DD33} 3.3 V	20	40	80	Ω
		V_{DD33} 2 V		100		
$t_{eh\ RSTL}$	E ternal reset pulse hold time [2]		2.5			s
$t_{g\ RSTL}$	Filtered glitch duration [3]			200		ns
$t_{e\ RSTL}$	E ternal reset pulse duration [4]		500			s
$t_{i\ RSTL}$	Internal reset pulse duration			2		Tcpu

1. The le el on the $\overline{\text{RESET}}$ pin must be free to go belo the V_{IL} ma . le el specified in *Section 7.8.1*. Other ise the reset ill not be ta en into account internally.
2. To guarantee the reset of the De ice a minimum pulse has to be applied to the $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin ith a duration belo $t_{eh\ RSTL}$ can be ignored. Not tested in production guaranteed by design.
3. The reset net ork protects the de ice against parasitic resets.
4. The e ternal reset duration must respect this timing to guarantee a correct start-up of the internal regulator at po er-up. Not tested in production guaranteed by design.

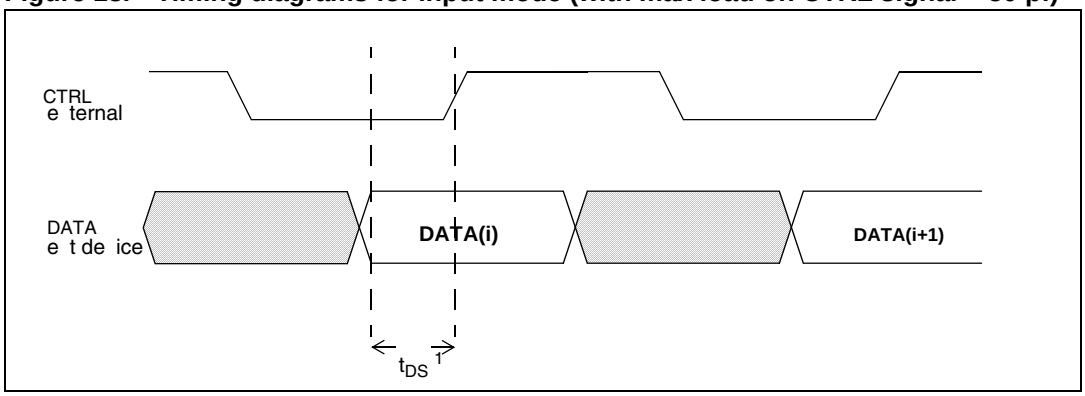
Figure 17. Typical R_{ON} on $\overline{\text{RESET}}$ pin



7.9 Other communication interface characteristics

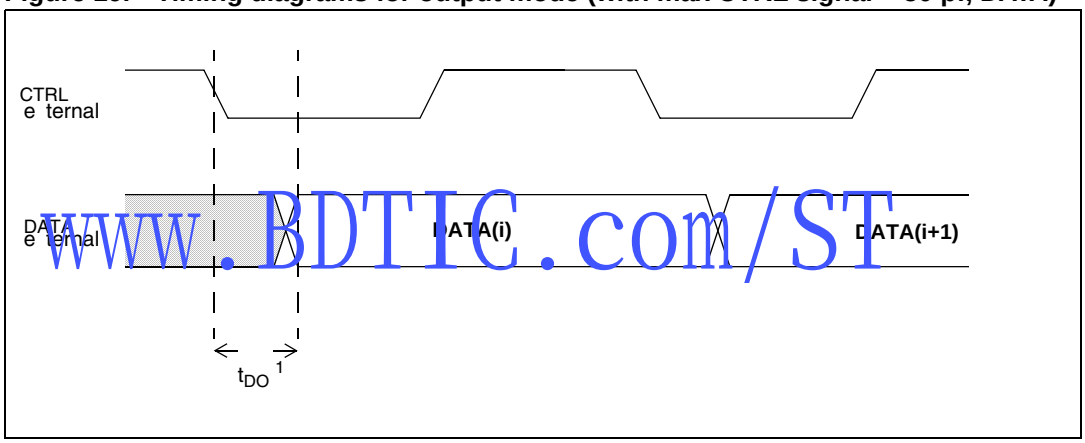
7.9.1 MSCI parallel interface

Figure 18. Timing diagrams for input mode (with max load on CTRL signal = 50 pf)



1. t_{DS} is the setup time for data sampling.

Figure 19. Timing diagrams for output mode (with max CTRL signal = 50 pf, DATA)



1. t_{DO} is the data output time for data sampling.

Table 23. MSCI parallel interface DC characteristics

MSCI DC Electrical Characteristics						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ(1)**	**Max.**	**Unit**
Data setup time	t_{DS}			11		ns
Data output time	t_{DO}			6		ns
CTRL line capacitance	Cctrl			50		pF
Data line capacitance	Cdata			50		pF

1. Data based on design simulation and not tested in production.

7.9.2 USB (Universal Bus Interface)

Table 24. USB Interface DC characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{DDsuspend}$	Suspend current	V_{DD33} 3.3 V regulator and PHY ON	0.5 [1]	1.5	6 [1]	mA
		V_{DD33} 3.3 V Po er-do n mode 25 C [2]	60	90	190	A
R_{PU}	Pull-up resistor [1]			1.5		Ω
Full Speed Mode						
V_{TERM}	Termination oltage		0.8		2.0	V
VOH	High le el output oltage		2.8		3.6	V
VOL	Lo le el output oltage				0.8	V
V_{CRS}	Crosso er oltage		1.3		2.0	V
High Speed Mode						
V_{HSOH}	HS data signalling high			400		mV
V_{HSOL}	HS data signalling lo			5		mV

1. Not tested in production guaranteed by characterization.
2. In order to reach this alue the soft are must force the regulator into po er-do n mode and the I/Os compensation cell off.

Table 25. USB Interface AC timing

Symbol	Parameter	Conditions	Min	Max.	Unit
Full Speed Mode					
T_{FR}	Rise Time	C_L 50pF	4	20	ns
T_{FF}	Fall Time	C_L 50pF	4	20	ns
High Speed Mode					
T_{HSR}	Rise Time			500 [1]	ps
T_{HSF}	Fall Time			500 [1]	ps
T_{HSDRAT}	HS Data Rate		479.76	480.24	Mb/s

1. Not tested in production guaranteed by characterization.

Figure 20. USB signal eye diagram

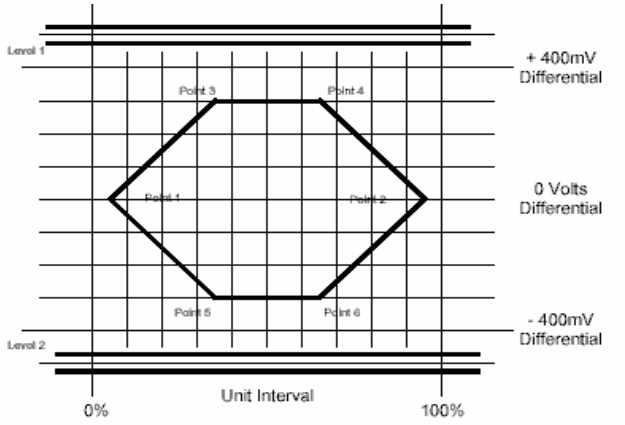


Table 26. USB high speed transmit waveform requirements

	Voltage Level (DP - DN)	Time
Unit Inter al UI	-	2.082 to 2.084 ns
Le el 1	475 mV	-
Le el 2	–475 mV	-
Point 1	0 V	5% UI
Point 2	0 V	95% UI
Point 3	300 mV	35% UI
Point 4	300 mV	65% UI
Point 5	–300 mV	35% UI
Point 6	–300 mV	65% UI

8 Package mechanical data

Figure 21. 64-pin Thin Quad Flat Package (10 x10) package outline

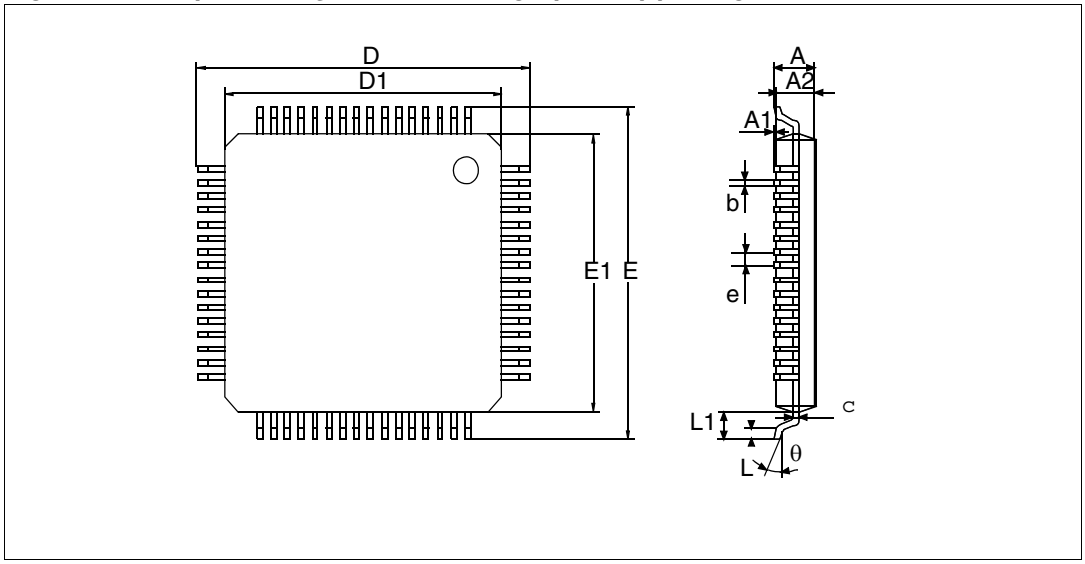


Table 27. 64-pin Thin Quad Flat Package (10 x10) mechanical data

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
E		12.00			0.472	
E1		10.00			0.394	
e		0.50			0.020	
θ	0	3.5	7	0	3.5	7
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
	Number of pins					
N	64					

9 Device ordering information

Table 28. Feature comparison

Features added in the ST72682/R21 versus ST72682/R20	Description
Continued AutoRun CDROM partition support	AutoRun runs a program hen the USB Flash dri e is inserted into a computer.

Table 29. Ordering Information

Orderable part number	Package	Operating voltage	Temperature range
ST72682/R20	LQFP64 10 10mm	3.0V to 3.6V	0 C to +70 C
ST72682/R21 latest firm are re ision	LQFP64 10 10mm	3.0V to 3.6V	0 C to +70 C

10 Revision history

Table 30. Document revision history

Date	Revision	Description of Changes
09-Feb-2006	1.0	Initial release
14-Aug-2007	2.0	Firm are re ision updated to R21. References to TQFP64 updated to LQFP64. Datasheet reformatted.

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