

STEPPER MOTOR CONTROLLER IC

 Check for Samples: [DRV8818](#)

FEATURES

- **Pulse Width Modulation (PWM) Microstepping Motor Driver**
 - Built-In Microstepping Indexer
 - Up to 2.5-A Current Per Winding
 - Microstepping Indexer Provides up to 1/8-Step Operation
 - Low 0.45-Ω (HS + LS) MOSFET On-Resistance
- **Pin-Compatible Upgrade to DRV8811 With Lower $R_{ds(on)}$**

- **Thermally Enhanced Surface Mount Package**

APPLICATIONS

- **Printers**
- **Scanners**
- **Office Automation Machines**
- **Gaming Machines**
- **Factory Automation**
- **Robotics**

DESCRIPTION/ORDERING INFORMATION

The DRV8818 provides an integrated stepper motor driver solution for printers, scanners, and other automated equipment applications. The device has two H-bridge drivers, as well as microstepping indexer logic to control a stepper motor.

The output driver block for each consists of N-channel power MOSFETs configured as full H-bridges to drive the motor windings.

A simple step/direction interface allows easy interfacing to controller circuits. Pins allow configuration of the motor in full-step, half-step, quarter-step, or eighth-step modes. Decay mode and PWM off time are programmable.

Internal shutdown functions are provided for over current protection, short circuit protection, under-voltage lockout and overtemperature.

The DRV8818 is packaged in a PowerPAD™ 28-pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS and no Sb/Br).

ORDERING INFORMATION⁽¹⁾

T_A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	PowerPAD™ (HTSSOP) – PWP	Reel of 2000	DRV8818PWPR	DRV8818
		Tube of 50	DRV8818PWP	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PRODUCT PREVIEW


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

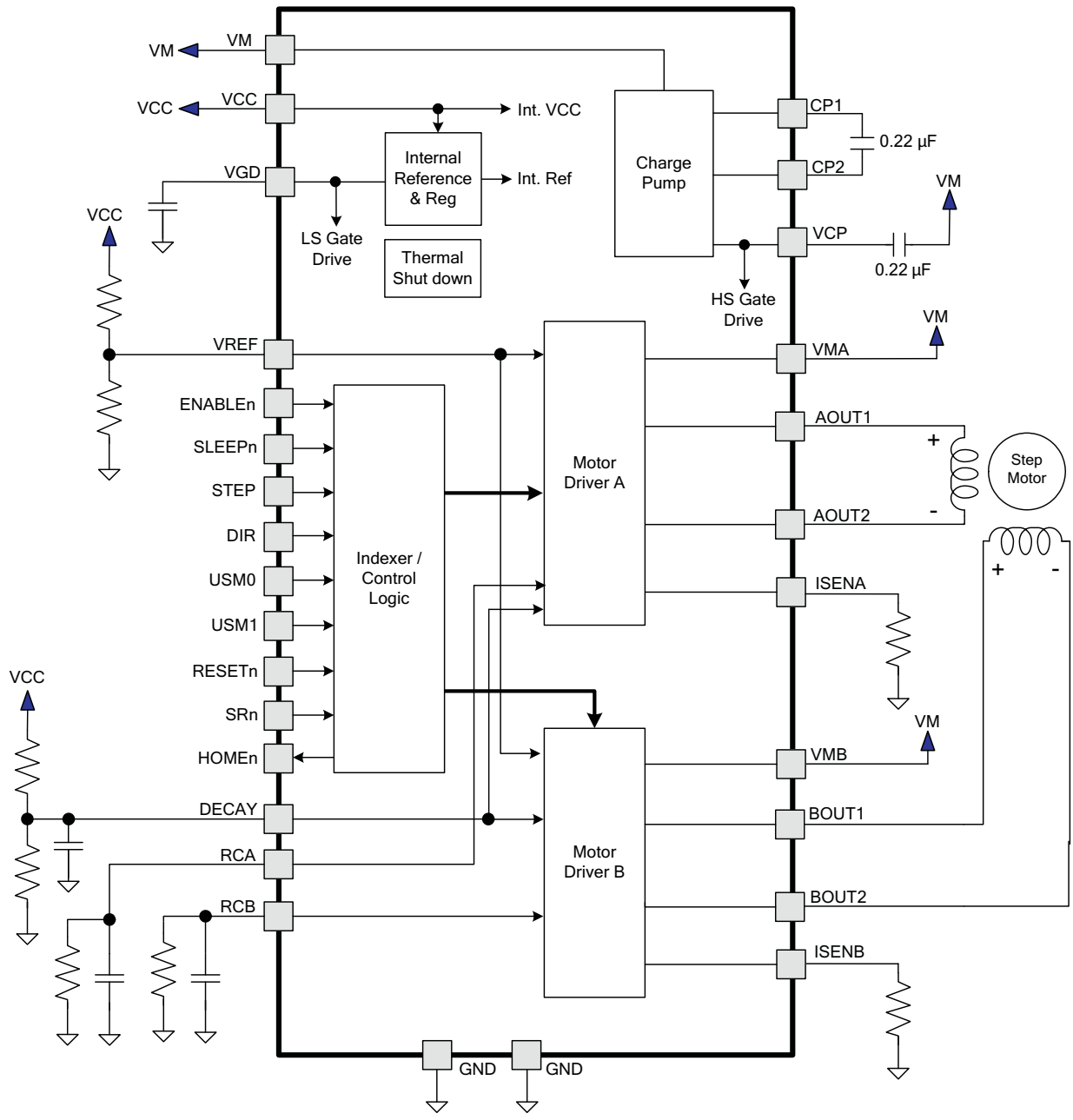
PowerPAD is a trademark of Texas Instruments.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

Copyright © 2011, Texas Instruments Incorporated

www.BDTIC.com/TI

FUNCTIONAL BLOCK DIAGRAM



PRODUCT PREVIEW

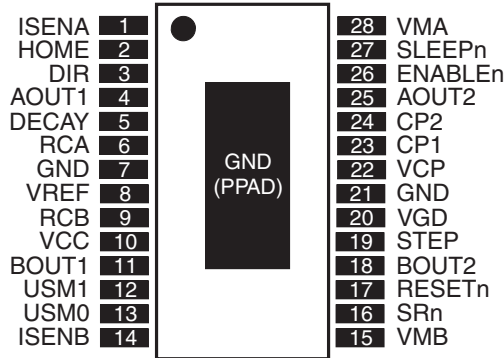
TERMINAL FUNCTIONS

NAME	NO.	I/O ⁽¹⁾	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND				
GND	7, 21	-	Device ground	
VMA	28	-	Bridge A power supply	Connect to motor supply (8 V to 35 V). Both pins must be connected to same supply.
VMB	15	-	Bridge B power supply	Connect to motor supply (8 V to 35 V). Both pins must be connected to same supply.
VCC	10	-	Logic supply voltage	Connect to 3-V to 5-V logic supply. Bypass to GND with a 0.1- μ F ceramic capacitor.
CP1	23	IO	Charge pump flying capacitor	Connect a 0.22- μ F capacitor between CP1 and CP2.
CP2	24	IO	Charge pump flying capacitor	Connect a 0.22- μ F capacitor between CP1 and CP2.
VCP	22	IO	High-side gate drive voltage	Connect a 0.22- μ F ceramic capacitor to V_M .
VGD	20	IO	Low-side gate drive voltage	Bypass to GND with a 0.22- μ F ceramic capacitor.
CONTROL				
ENABLEn	26	I	Enable input	Logic high to disable device outputs, logic low to enable outputs
SLEEPn	27	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode
DECAY	5	I	Decay mode select	Voltage applied sets decay mode - see motor driver description for details. Bypass to GND with a 0.1- μ F ceramic capacitor.
STEP	19	I	Step input	Rising edge causes the indexer to move one step
DIR	3	I	Direction input	Level sets the direction of stepping
USM0	13	I	Microstep mode 0	USM0 and USM1 set the step mode - full step, half step, quarter step, or eight microsteps/step
USM1	12	I	Microstep mode 1	USM0 and USM1 set the step mode - full step, half step, quarter step, or eight microsteps/step
RESETn	17	I	Reset input	Active-low reset input initializes the indexer logic and disables the H-bridge outputs
SRn	16	I	Sync. Rect. enable input	When active low, synchronous rectification is enabled
VREF	8	I	Current set reference input	Reference voltage for winding current set
RCA	6	I	Bridge A blanking and off time adjust	Connect a parallel resistor and capacitor to GND - see motor driver description for details.
RCB	9	I	Bridge B blanking and off time adjust	Connect a parallel resistor and capacitor to GND - see motor driver description for details.
ISENA	1	-	Bridge A ground / Isense	Connect to current sense resistor for bridge A
ISENB	14	-	Bridge B ground / Isense	Connect to current sense resistor for bridge B
OUTPUTS				
AOUT1	4	O	Bridge A output 1	Connect to bipolar stepper motor winding
AOUT2	25	O	Bridge A output 2	Positive current is AOUT1 \rightarrow AOUT2
BOUT1	11	O	Bridge B output 1	Connect to bipolar stepper motor winding
BOUT2	18	O	Bridge B output 2	Positive current is BOUT1 \rightarrow BOUT2
HOMEn	2	O	Home position	Logic low when at home state of step table, logic high at other states

(1) Directions: I = input, O = output, OZ = 3-state output, OD = open-drain output, IO = input/output

PRODUCT PREVIEW

PWP (HTSSOP) PACKAGE



ABSOLUTE MAXIMUM RATINGS^{(1) (2) (3)}

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{MX}	Power supply voltage range	-0.3	35	V
V _{CC}	Power supply voltage range	-0.3	7	V
	Digital pin voltage range	-0.5	7	V
V _{REF}	Input voltage range	-0.3 V	V _{CC}	V
	ISENSEx pin voltage range	-0.3	0.5	V
I _{O(peak)}	Peak motor drive output current, t < 1 μs	Internally limited		
P _D	Continuous total power dissipation	See Dissipation Ratings Table		
T _J	Operating virtual junction temperature range	-40	150	°C
T _{stg}	Storage temperature range	-60	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) Power dissipation and thermal limits must be observed.

PRODUCT PREVIEW

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		DRV8818		UNITS
		PWP		
		28 PINS		
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	32.2		°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽³⁾	16.3		
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	14		
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	0.5		
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	13.8		
θ_{JCbott}	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	2.1		

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range ⁽¹⁾	8		35	V
V_{CC}	Logic power supply voltage range	3		5.5	V
V_{REF}	VREF input voltage	0		V_{CC}	V
R_X	R_X resistance value	470	680	1500	pF
C_X	C_X capacitance value	12	56	100	kΩ

- (1) All V_M pins must be connected to the same supply voltage.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supplies						
I_{VM}	V_M operating supply current	$V_M = 35\text{ V}$, $f_{PWM} < 50\text{ KHz}$		4.5	8	mA
I_{VCC}	V_{CC} operating supply current	$f_{PWM} < 50\text{ KHz}$		0.4	4	mA
I_{VMQ}	V_M sleep mode supply current	$V_M = 35\text{ V}$		12	20	μA
I_{VCCQ}	V_{CC} sleep mode supply current			5	20	μA
V_{UVLO}	V_M undervoltage lockout voltage	V_M rising		6.7	8	V
	V_{CC} undervoltage lockout voltage	V_{CC} rising		2.71	2.95	
VREF Input/Current Control Accuracy						
I_{REF}	VREF input current	$V_{REF} = 3.3\text{ V}$	-3		3	μA
ΔI_{CHOP}	Chopping current accuracy	$V_{REF} = 2.0\text{ V}$, 70% to 100% current	-5		5	%
		$V_{REF} = 2.0\text{ V}$, 20% to 56% current	-10		10	%
Logic-Level Inputs						
V_{IL}	Input low voltage				$0.3 \times V_{CC}$	V
V_{IH}	Input high voltage		$0.7 \times V_{CC}$			V
I_{IL}	Input low current	$V_{IN} = 0.3 \times V_{CC}$	-20		20	μA
I_{IH}	Input high current	$V_{IN} = 0.3 \times V_{CC}$	-20		20	μA

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

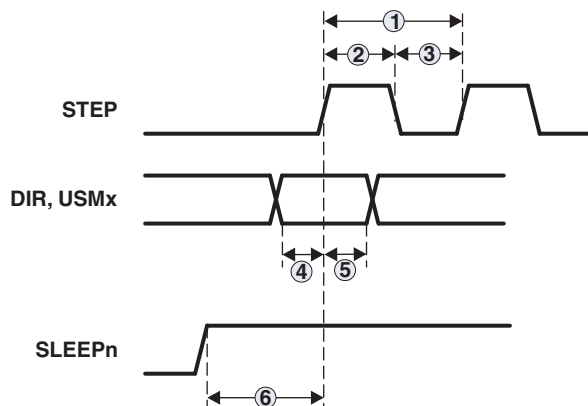
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R _{PU}	Pullup resistance	ENBLn to V _{CC}		1		MΩ
HOMEn Output						
V _{OL}	Output low voltage	I _O = 200 μA			0.3 × V _{CC}	V
V _{OH}	Output high voltage	I _O = –200 μA	0.7 × V _{CC}			V
Decay Input						
V _{IL}	Input low threshold voltage	For fast decay mode		0.21 × V _{CC}		V
V _{IH}	Input high threshold voltage	For slow decay mode		0.6 × V _{CC}		V
H-Bridge FETS						
R _{ds(on)}	HS FET on resistance	V _M = 24 V, I _O = 2.5 A, T _J = 25°C		0.25	0.30	Ω
R _{ds(on)}	LS FET on resistance	V _M = 24 V, I _O = 2.5 A, T _J = 25°C		0.20	0.24	Ω
I _{OFF}			–20		20	μA
Motor Driver						
t _{OFF}	Off time	R _x = 56 kΩ, C _x = 680 pF	30	38	46	μs
t _{BLANK}	Current sense blanking time	R _x = 56 kΩ, C _x = 680 pF	700	950	1200	ns
t _{DT}	Dead time ⁽¹⁾	SRn = 0	100	475	800	ns
Protection Circuits						
t _{TSD}	Thermal shutdown temperature ⁽¹⁾	Die temperature	150	160	180	°C

(1) Not tested in production - guaranteed by design.

TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
f_{STEP}	Step frequency		500	kHz
$t_{WH(STEP)}$	Pulse duration, STEP high	1		μ s
$t_{WL(STEP)}$	Pulse duration, STEP low	1		μ s
$t_{SU(STEP)}$	Setup time, command to STEP rising	200		ns
$t_{H(STEP)}$	Hold time, command to STEP rising	200		ns
t_{WAKE}	Wakeup time, SLEEPn inactive to STEP	1		ms



PRODUCT PREVIEW

FUNCTIONAL DESCRIPTION

PWM H-Bridge Drivers

DRV8818 contains two H-bridge motor drivers with current-control PWM circuitry, and a microstepping indexer. A block diagram of the motor control circuitry is shown below.

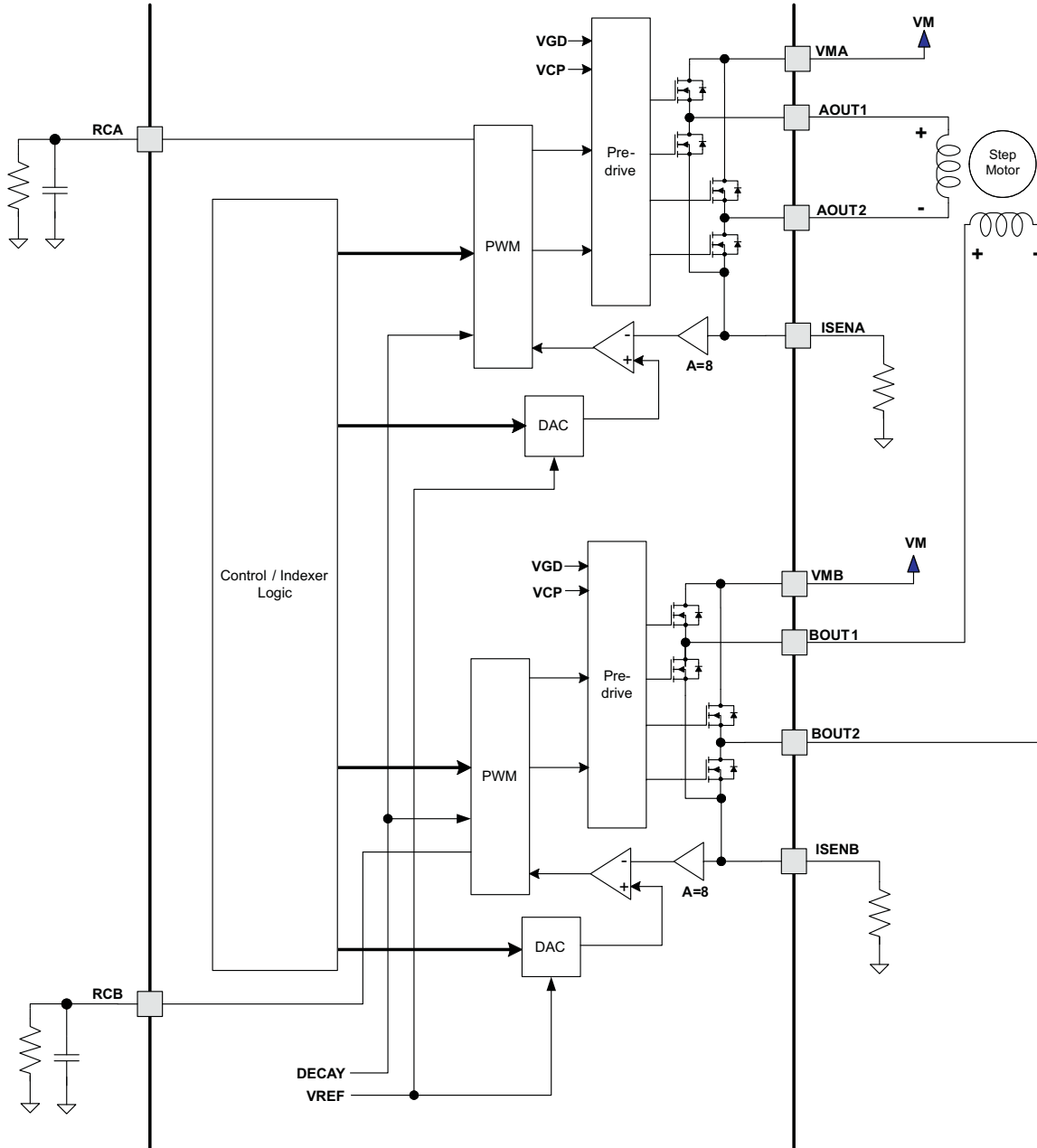


Figure 1. Motor Control Circuitry

PRODUCT PREVIEW

Current Regulation

The PWM chopping current is set by a comparator, which compares the voltage across a current sense resistor, multiplied by a factor of 8, with a reference voltage. The reference voltage is input from the VREF pin. The full-scale (100%) chopping current is calculated as follows:

$$I_{CHOP} = \frac{V_{REFX}}{8 \cdot R_{ISENSE}} \quad (1)$$

Example:

If a 0.22-Ω sense resistor is used and the VREFx pin is 3.3 V, the full-scale (100%) chopping current is 3.3 V/(8 * 0.22 Ω) = 1.875 A.

The reference voltage is also scaled by an internal DAC that allows torque control for fractional stepping of a bipolar stepper motor, as described in the "Microstepping Indexer" section below.

When a winding is activated, the current through it rises until it reaches the chopping current threshold described above, then the current is switched off for a fixed off time. The off time is determined by the values of a resistor and capacitor connected to the RCA (for bridge A) and RCB (for bridge B) pins. The off time is approximated by:

$$t_{OFF} = R \cdot C \quad (2)$$

To avoid falsely tripping on transient currents when the winding is first activated, a blanking period is used immediately after turning on the FETs, during which the state of the current sense comparator is ignored. The blanking time is determined by the value of the capacitor connected to the RCx pin and is approximated by:

$$t_{BLANK} = 1400 \cdot C \quad (3)$$

Decay Mode

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in [Figure 2](#), Item 1. The current flow direction shown indicates positive current flow in the step table below.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. If synchronous rectification is enabled (SRn pin logic low), the opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. If SRn is high, current is recirculated through the body diodes, or through external Schottky diodes. Fast-decay mode is shown in [Figure 2](#), Item 2.

In slow-decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in [Figure 2](#), Item 3.

If SRn is high, current is recirculated only through the body diodes, or through external Schottky diodes. In this case fast decay is always used.

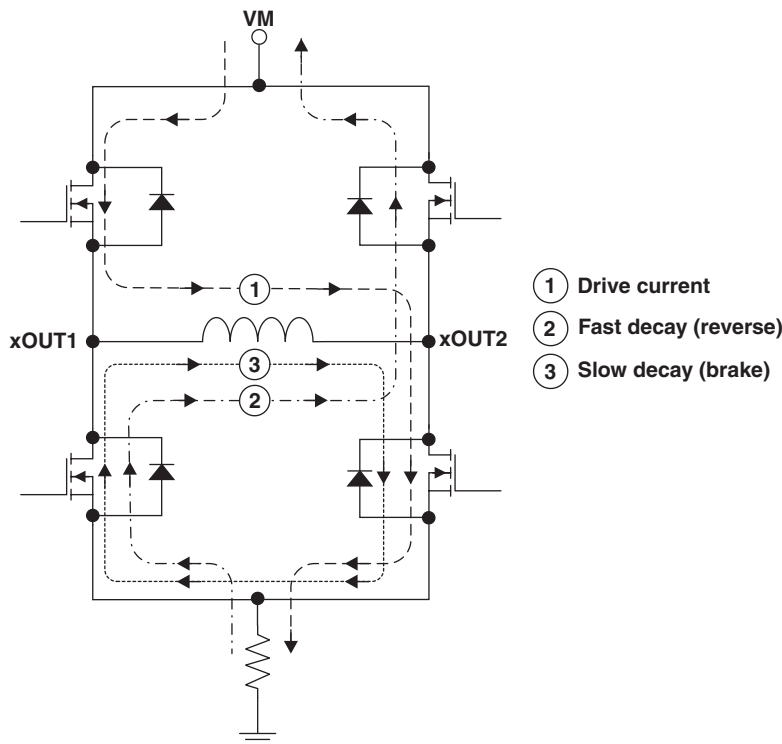


Figure 2. Decay Mode

The DRV8818 also supports a mixed decay mode. Mixed decay mode begins as fast decay, but after a period of time switches to slow decay mode for the remainder of the fixed off time.

Fast and mixed decay modes are only active if the current through the winding is decreasing; if the current is increasing, then slow decay is always used.

Which decay mode is used is selected by the voltage on the DECAy pin. If the voltage is greater than $0.6 \times V_{CC}$, slow decay mode is always used. If DECAy is less than $0.21 \times V_{CC}$, the device operates in fast decay mode when the current through the winding is decreasing. If the voltage is between these levels, mixed decay mode is enabled.

In mixed decay mode, the voltage on the DECAy pin sets the point in the cycle that the change to slow decay mode occurs. This time can be approximated by:

$$t_{FD} = R \cdot C \cdot \ln\left(\frac{0.6 \cdot V_{CC}}{V_{DECAy}}\right) \tag{4}$$

Mixed decay mode is only used while the current through the winding is decreasing; slow decay is used while the current is increasing.

Operation of the blanking, fixed off time, and mixed decay mode is illustrated in [Figure 3](#).

PRODUCT PREVIEW

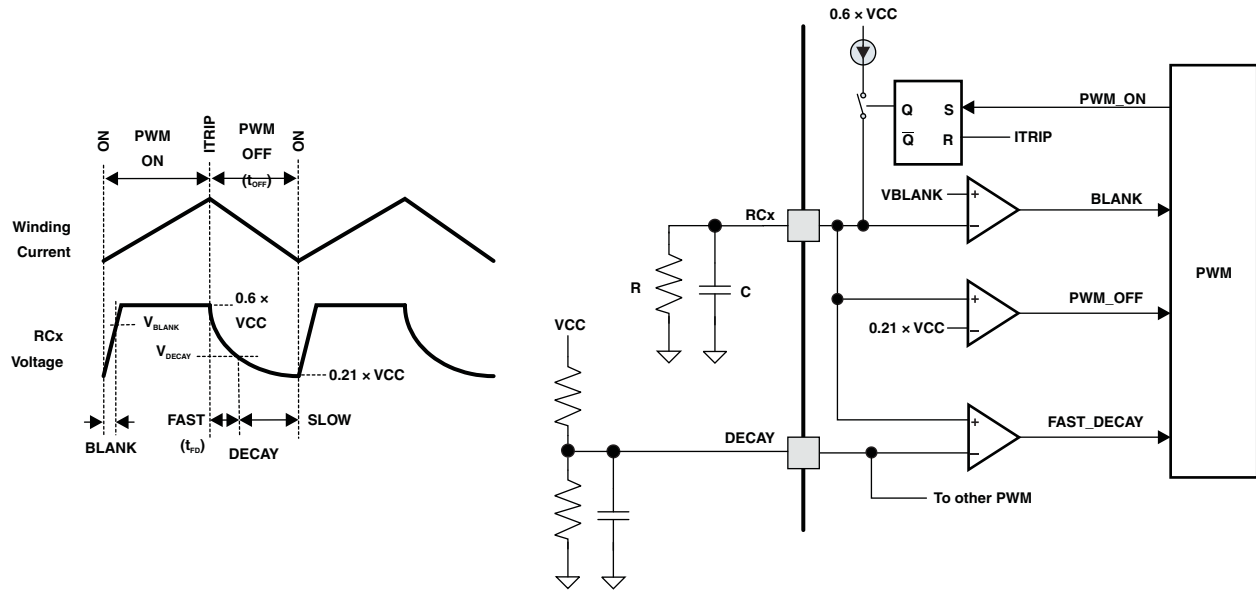


Figure 3. PWM

Microstepping Indexer

Built-in indexer logic in the DRV8818 allows a number of different stepping configurations. The USM1 and USM0 pins are used to configure the stepping format as shown in the table below:

USM1	USM0	STEP MODE
0	0	Full step (2-phase excitation)
0	1	1/2 step (1-2 phase excitation)
1	0	1/4 step (W1-2 phase excitation)
1	1	Eight microsteps/steps

The following table shows the relative current and step directions for different settings of USM1 and USM0. At each rising edge of the STEP input, the indexer travels to the next state in the table. The direction is shown with the DIR pin high; if the DIR pin is low the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

Note that the home state is 45 degrees. This state is entered at power-up or device reset. The HOMEn output pin is driven low in this state. In all other states it is driven logic high.

PRODUCT PREVIEW

FULL STEP USM = 00	1/2 STEP USM = 01	1/4 STEP USM = 10	1/8 STEP USM = 11	AOUTx CURRENT (% FULL-SCALE)	BOUTx CURRENT (% FULL-SCALE)	STEP ANGLE (DEGREES)
	1	1	1	100	0	0
			2	98	20	11.325
		2	3	92	38	22.5
			4	83	56	33.75
1	2	3	5	71	71	45 (home state)
			6	56	83	56.25
		4	7	38	92	67.5
			8	20	98	78.75
	3	5	9	0	100	90
			10	-20	98	101.25
		6	11	-38	92	112.5
			12	-56	83	123.75
2	4	7	13	-71	71	135
			14	-83	56	146.25
		8	15	-92	38	157.5
			16	-98	20	168.75
	5	9	17	-100	0	180
			18	-98	-20	191.25
		10	19	-92	-38	202.5
			20	-83	-56	213.75
3	6	11	21	-71	-71	225
			22	-56	-83	236.25
		12	23	-38	-92	247.5
			24	-20	-98	258.75
	7	13	25	0	-100	270
			26	20	-98	281.25
		14	27	38	-92	292.5
			28	56	-83	303.75
4	8	15	29	71	-71	315
			30	83	-56	326.25
		16	31	92	-38	337.5
			32	98	-20	348.75

PRODUCT PREVIEW

RESETn, ENABLEn and SLEEPn Operation

The RESETn pin, when driven active low, resets the step table to the home position. It also disables the H-bridge drivers. The STEP input is ignored while RESETn is active.

The ENABLEn pin is used to control the output drivers. When ENABLEn is low, the output H-bridges are enabled. When ENABLEn is high, the H-bridges are disabled and the outputs are in a high-impedance state.

Note that when ENABLEn is high, the input pins and control logic, including the indexer (STEP and DIR pins) are still functional.

The SLEEPn pin is used to put the device into a low power state. If SLEEPn is low, the H-bridges are disabled, the gate drive charge pump is stopped, and all internal clocks are stopped. In this state all inputs are ignored until the SLEEPn pin returns high.

Protection Circuits

Overcurrent Protection (OCP)

If the current through any FET exceeds the preset overcurrent threshold, all FETs in the H-bridge will be disabled until the ENABLEn pin has been brought inactive high and then back low, or power is removed and re-applied. Overcurrent conditions are sensed in both directions; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown.

Note that overcurrent protection does not use the current sense circuitry used for PWM current control and is independent of the Isense resistor value or VREF voltage.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all drivers in the device are shut down and the indexer is reset to the home state. Once the die temperature has fallen to a safe level operation resumes.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM or VCC pins falls below the VM or VCC undervoltage lockout threshold voltage, all circuitry in the device will be disabled, and the indexer will be reset to the home state. Operation will resume when VM and VCC both rise above their UVLO thresholds.

THERMAL INFORMATION

Thermal Protection

The DRV8818 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the DRV8818 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation when running a stepper motor can be roughly estimated by:

$$P_{TOT} = 4 \cdot R_{DS(ON)} \cdot (I_{OUT(RMS)})^2 \quad (5)$$

where P_{TOT} is the total power dissipation, $R_{DS(ON)}$ is the resistance of each FET, and $I_{OUT(RMS)}$ is the RMS output current being applied to each winding. $I_{OUT(RMS)}$ is equal to the approximately 0.7x the full-scale output current setting. The factor of 4 comes from the fact that there are two motor windings, and at any instant two FETs are conducting winding current for each winding (one high-side and one low-side).

The maximum amount of power that can be dissipated in the DRV8818 is dependent on ambient temperature and heatsinking. The thermal dissipation ratings table in the datasheet can be used to estimate the temperature rise for typical PCB constructions.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI Application Report [SLMA002](#), "PowerPAD™ Thermally Enhanced Package" and TI Application Brief [SLMA004](#), "PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
DRV8818PWP	PREVIEW	HTSSOP	PWP	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
DRV8818PWPR	PREVIEW	HTSSOP	PWP	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

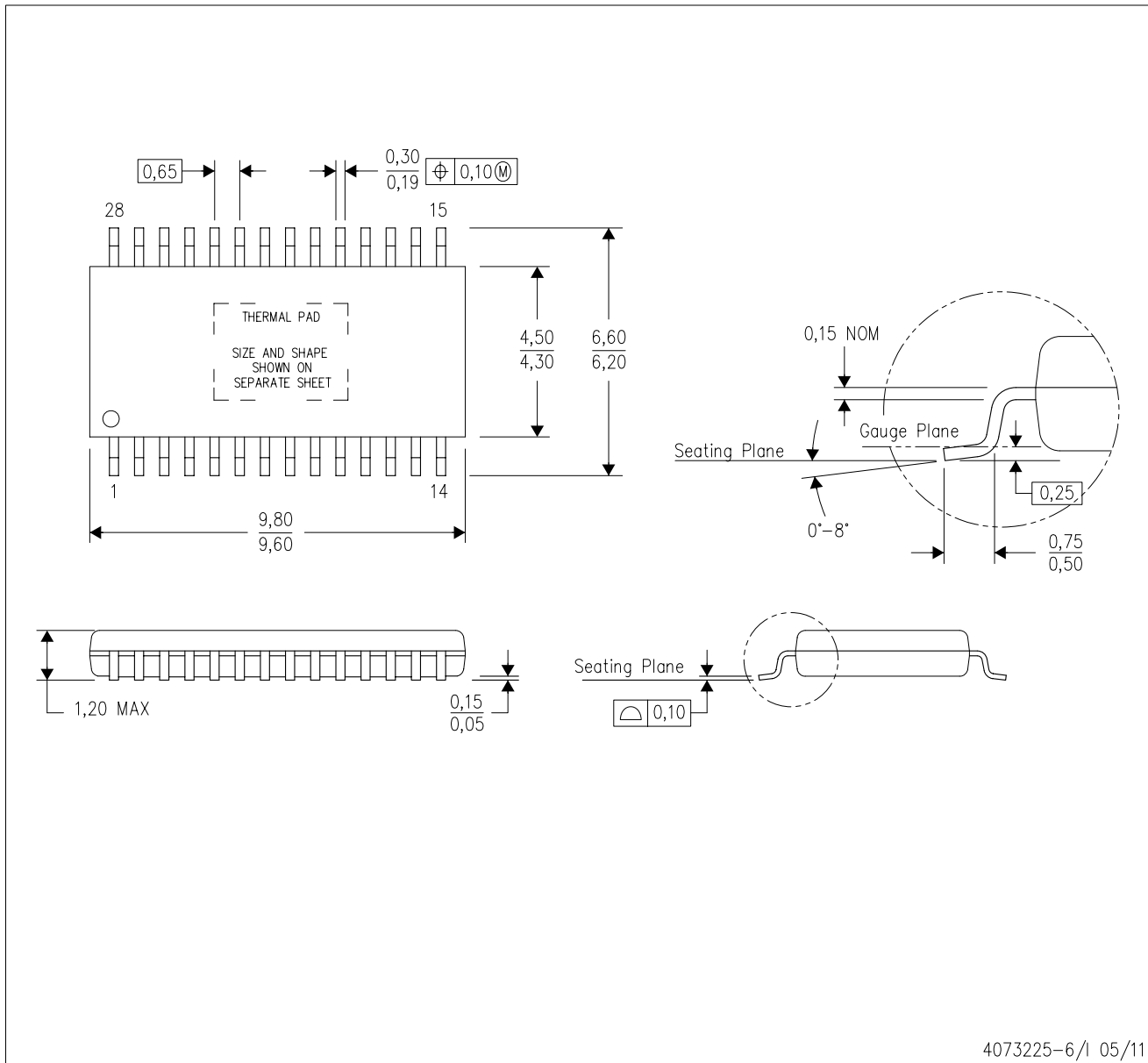
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

MECHANICAL DATA

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-6/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.



www.BDTIC.com/TI

THERMAL PAD MECHANICAL DATA

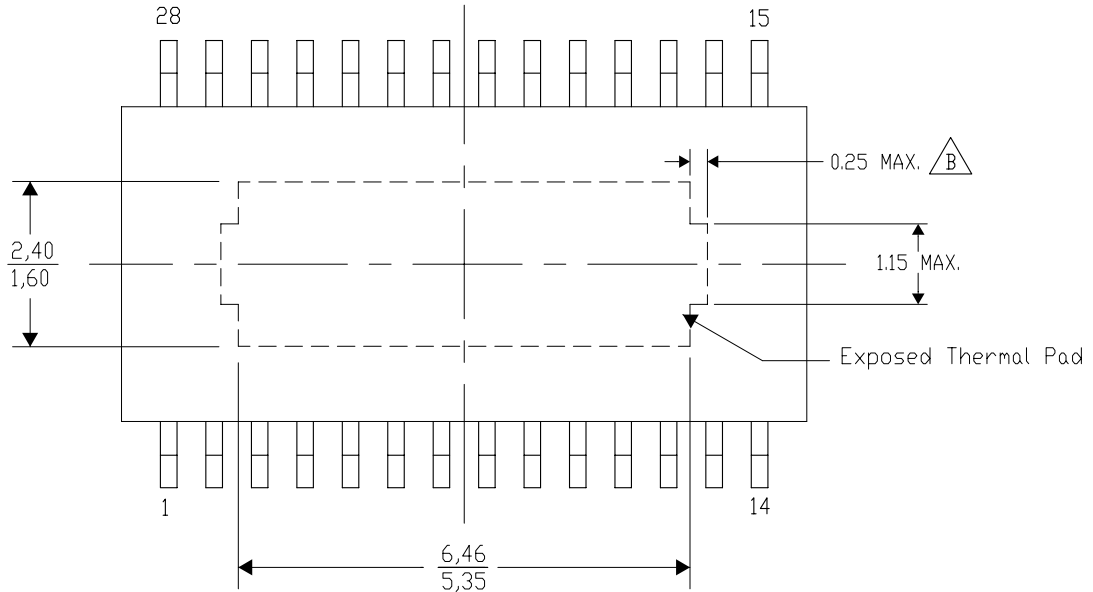
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-24/W 05/11

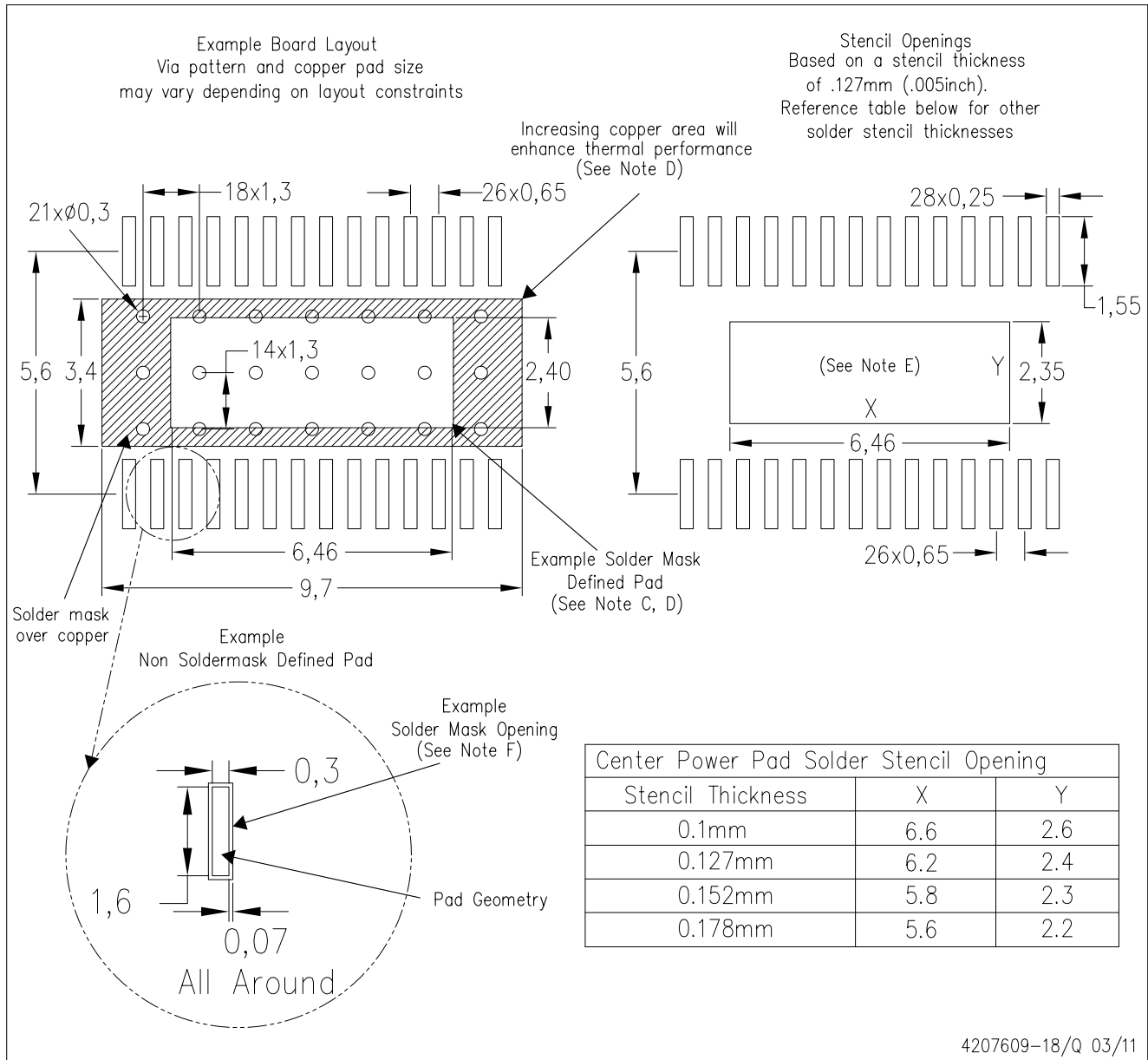
NOTE: A. All linear dimensions are in millimeters

$\triangle B$ Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.



IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated

www.BDTIC.com/TI