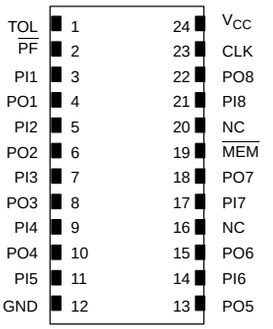
DALLAS SEMICONDUCTOR

DS1381
NV RAMport

FEATURES

- 2K x 8 Nonvolatile Static RAM
- 8–Bit transparent I/O Port
- Greater than 10 years of data retention in absence of V_{CC}
- Multiplexed address/data bus reduces pin count
- Write protection for both RAM and port status at either 5% or 10%
- Power Fail output signal
- Low power CMOS
- 24–pin DIP package
- Ideally suited for microcontroller applications as add on memory

PIN ASSIGNMENT



24–PIN ENCAPSULATED PACKAGE

PIN DESCRIPTION

PI1 – PI8	–	Port Inputs (µP Ports)
PO1 – PO8	–	Port Outputs (External Ports)
$\overline{PF}$	–	Power Fail Output
CLK	–	Clock
$\overline{MEM}$	–	Memory Select
V_{CC}	–	+5 Volts
GND	–	Ground
NC	–	No Connection

Note: Pins 16 and 20 are missing by design.

DESCRIPTION

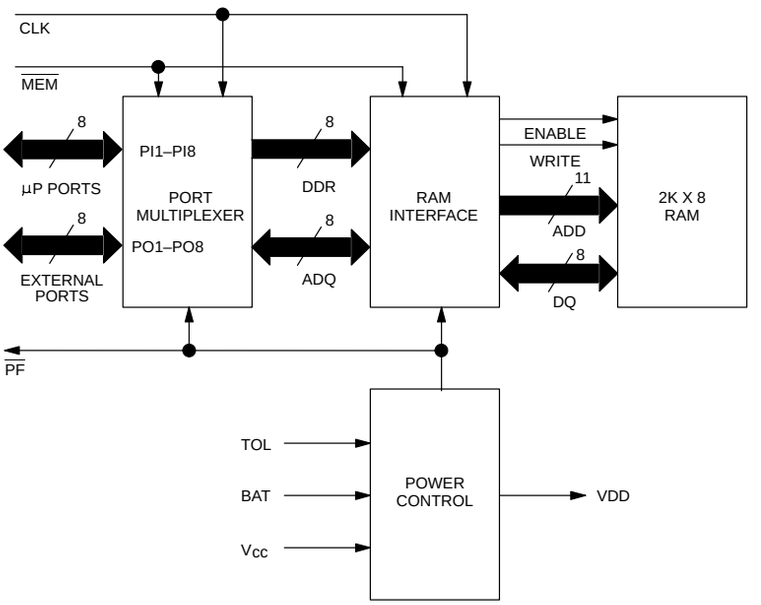
The DS1381 is a 2K x 8 nonvolatile static RAM designed to connect directly to the port pins of a microcontroller. Eight of ten port pins required to interface with the microcontroller are reproduced by the DS1381 for general purpose use. The reproduced port pins can be both inputs and outputs and will appear exactly the same as the pins on the attached microcontroller. The static RAM is read or written with three successive cycles containing high order address, low order address and then data. Read, write and status information is passed to the DS1381 along with the high order address transfer. While transferring data to and from memory, the I/O status is locked and maintained. All data within the DS1381 is nonvolatile and data retention time is over 10 years. The DS1381 is controlled by only two signals; clock and memory select.

OPERATION–MEMORY AND PORT PINS

A block diagram of the DS1381 nonvolatile RAMport is shown in Figure 1. As shown, the DS1381 has four key elements; namely the port multiplexer, the RAM interface, a 2K x 8 static RAM, and a power control section. The port multiplexer is connected to eight microcontroller port pins from which address, data and port data are received. The 8 microcontroller port pins are reproduced through transmission gates at the multiplexer output when the $\overline{MEM}$ pin is high. When the $\overline{MEM}$ pin is low all reproduced output pins are latched in their high or low states and all reproduced inputs go to a high impedance state. With the $\overline{MEM}$ pin low the microcontroller port pins are then free to pass address and data to and from the nonvolatile static RAM. Each read or write cycle to memory is accomplished in three separate steps involving two address transfers and one data transfer. The clock signal (CLK) is used to strobe address and data information through the port multiplexer into the RAM interface circuitry. To accomplish RAM access the high order address (A8–A10) is placed on port input pins PI1 through PI3. PI4 through PI8 contain bits which dictate a read of RAM or a write to RAM. If these bits do not match exactly the bit patterns as shown in Figure 2, completion of the full cycle will be allowed but no action will be taken during the data transfer portion. With the proper bit patterns placed on the port pins, the CLK input is then transitioned high to low and then high again. The clock action allows the address and read/write information to propagate through the port multiplexer and latch the information into the RAM interface. Next the low order address (A0–A7) is placed on the port input pins (PI1 through PI8) and the second address transfer also propagates through the port multiplexer as CLK goes low and returns high. The RAM is now ready for data transfer. If a write cycle is to occur, the microcontroller port pins must deliver the correct data to be written. As the CLK transitions high to low, data propagates through the port multiplexer and the RAM interface and finally to the RAM where data is written into RAM. The write cycle is terminated when the CLK transitions low to high. Data can then be removed from the port input pins. If during the data transfer a read cycle is to occur, the port input pins must not be driven by the microcontroller. Then as CLK transitions high to low, the RAM becomes active and data is presented on the port input pins for the microcontroller to read. A read cycle is terminated when the CLK signal is transitioned low to high and the port input pins are returned to a high impedance state.

After completing the read or write cycle another read or write cycle can be performed without pulsing the $\overline{MEM}$ pin high between cycles. After all access to the RAM is complete, the $\overline{MEM}$ pin must be returned to a high state.

FUNCTIONAL BLOCK DIAGRAM Figure 1



OPERATION – WRITING THE DATA DIRECTION REGISTER

The data direction register is written with a logic one in each bit location which will have a corresponding high impedance output pin (PO1–PO8) during reading and writing of the memory of the DS1381 by the microcontroller (see Figure 3). This will avoid contention between PO1–PO8 and devices driving PO1–PO8 as inputs. To write data to the data direction register, the CLK input is driven low prior to $\overline{MEM}$ going low. With CLK low $\overline{MEM}$ is driven low which latches the port output pins and readies the DS1381 for data direction information. Data direction information is then placed on the port input pins by the microcontroller and is written into the data direction register as $\overline{MEM}$ transitions low to high. While the data direction register is being written, the output pins (PO1 through PO8) are latched to the PI1 through PI8 states with their high or low impedance condition determined by the old data direction contents. The new data direction contents will be effective the next time $\overline{MEM}$ is taken to a low state.

OPERATION – POWER FAIL AND DATA RETENTION MODE

The DS1381 has full functional capability when V_{CC} is within normal limits. However, when V_{CC} goes to an out of tolerance level, the nonvolatile RAMport assumes a write protected status such that the memory and data direction register cannot be accessed. In addition the port output signals go to a high impedance state, the port input pins become “don’t care” and the transmission gates connecting the 8 microprocessor port pins to the external ports will go to a low impedance state. The power fail pin ($\overline{PF}$) goes to an active low level when power fail occurs and remains low until V_{CC} returns to nominal limits. The point at which write protection occurs depends on the level of the tolerance pin (TOL). When TOL is grounded, write protection will occur between 4.75 volts and 4.5 volts. When TOL is connected to V_{CC}, write protection occurs between 4.5 volts and 4.25 volts. After power fail detection has occurred and the V_{CC} level falls below the voltage level of the internal lithium cell the internal memory and register contents are maintained by this cell which is capable of maintaining data for over 10 years. The switch over from V_{CC} to the lithium cell occurs when V_{CC} is below approximately 3 volts.

READ AND WRITE BIT PATTERNS Figure 2

	LSB							MSB
READ	A8	A9	A10	1	0	1	0	1
WRITE	A8	A9	A10	0	1	0	1	0

DATA DIRECTION REGISTER BITS Figure 3

LSB							MSB
PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	–40°C to +70°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(0°C to 70°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage (TOL=GND)	V_{CC}	4.75	5.0	5.5	V	1
Supply Voltage (TOL=V_{CC})	V_{CC}	4.5	5.0	5.5	V	1
Logic 1 Input	V_{IH}	2.0		V_{CC} + 0.3	V	1
Logic 0 Input	V_{IL}	-0.3		+0.8	V	1

DC ELECTRICAL CHARACTERISTICS

(0°C to 70°C; V_{CC} within DC operating conditions)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Active Current t_{CYC}=200 ns	I_{CC1}		20	25	mA	2
Standby Current	I_{CC2}		3	7	mA	3
Logic 1 Out @ 1 mA	V_{OH}	2.4			V	1, 6
Logic 0 Out @ 2 mA	V_{OL}			0.4	V	1, 6
V_{CC} Write Protect (TOL=GND)	V_{TP}	4.50	4.62	4.75	V	1
V_{CC} Write Protect (TOL=VCC)	V_{TP}	4.25	4.37	4.50	V	1
Input Leakage	I_{IL}	–1.0		+1.0	µA	4
Output Leakage	I_{LO}	–1.0		+1.0	µA	5
Port Pins In to Out Impedance	P_Z		75	150	Ω	7

CAPACITANCE

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}	t_A=25°C			10	pF	
Output Capacitance	C_{OUT}	t_A=25°C			10	pF	

AC ELECTRICAL CHARACTERISTICS

(0°C to 70°C TOL = V_{CC}; V_{CC}=4.50 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Low	t_{CL}	150			ns	
Clock High	t_{CH}	50			ns	
Address Setup	t_{AS}	20			ns	
Address Hold	t_{AH}	0			ns	
Data Setup	t_{DS}	20			ns	
Data Hold	t_{DH}	0			ns	
$\overline{MEM}$ to CLK Low	t_{MC}	40			ns	
$\overline{MEM}$ to Output Latch	t_{ML}	25			ns	
CLK to $\overline{MEM}$ High	t_{CMH}	10			ns	
CLK to Data Valid	t_{CD}			100	ns	
CLK to Data at High Z	t_{DZ}			20	ns	
CLK to $\overline{MEM}$ Active	t_{CM}	40			ns	
DDR Data Setup	t_{DSD}	100			ns	
V_{CC} Slew Rate	t_R, t_F	250			µs	

DATA RETENTION

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Expected Data Retention	t_{DR}	10			years	

NOTES:

1. All voltages are reference to ground
2. Active current is defined as $\overline{MEM}$ low with CLK low and all outputs are open
3. Standby current is defined as $\overline{MEM}$ high with CLK high and all outputs are open
4. Input leakage applies to CLK and $\overline{MEM}$ only
5. Output leakage applies to $\overline{PF}$ only
6. Logic levels apply to $\overline{PF}$ and PO1–PO8 when these outputs are latched
7. Port input to output impedance is the on resistance of the transmission gate between port inputs and port outputs with $\overline{MEM}$ high and with less than 4 mA flowing through the transmission gate.

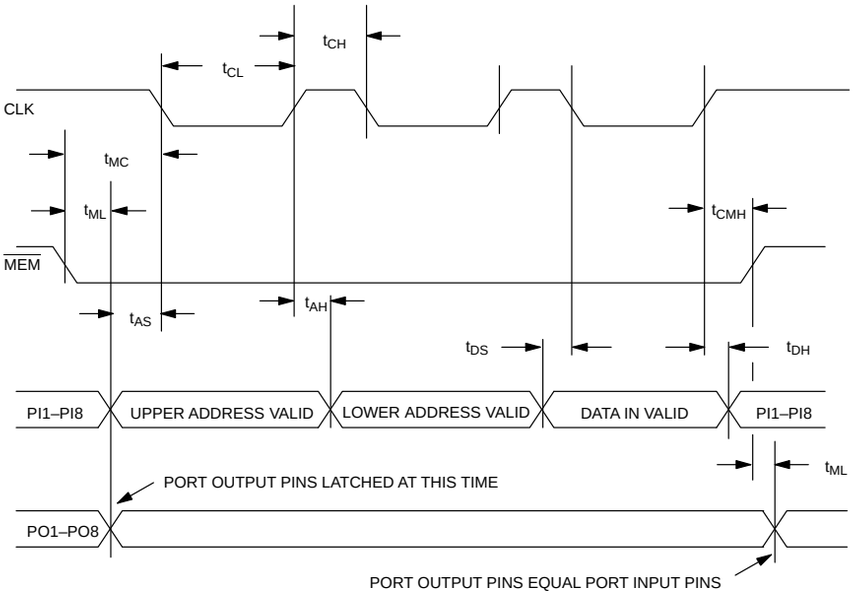
DC TEST CONDITIONS

Outputs Open
All voltages are referenced to ground.

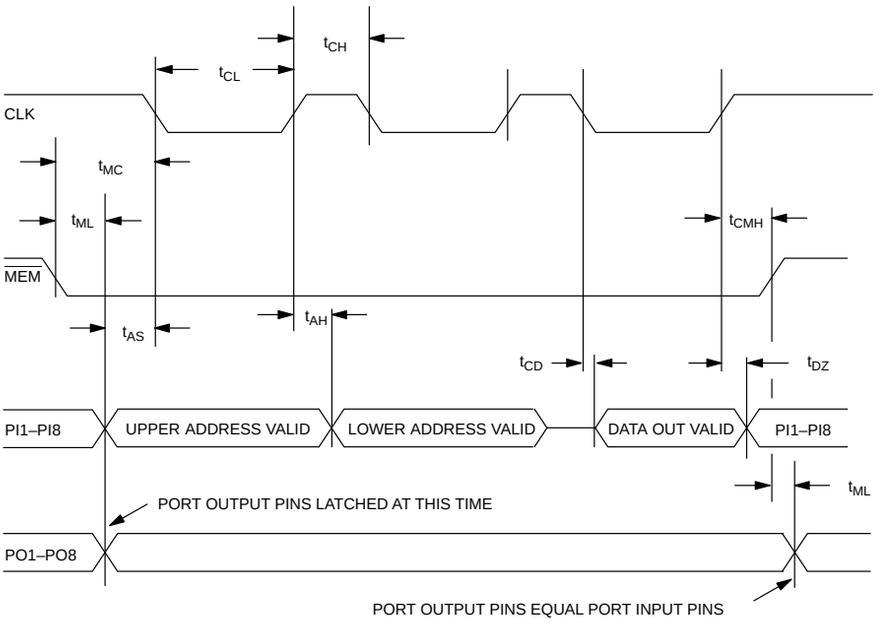
AC TEST CONDITIONS

Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0V – 3.0V
Timing Measurement Reference Levels
Input: 1.5V
Output: 1.5V
Input Pulse Rise and Fall Times: 5 ns

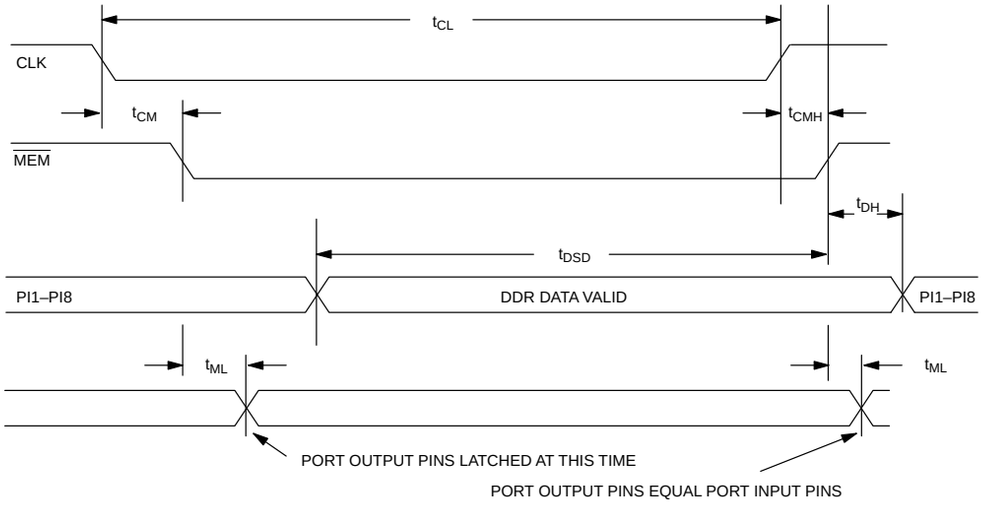
TIMING DIAGRAM: WRITE CYCLE TO MEMORY



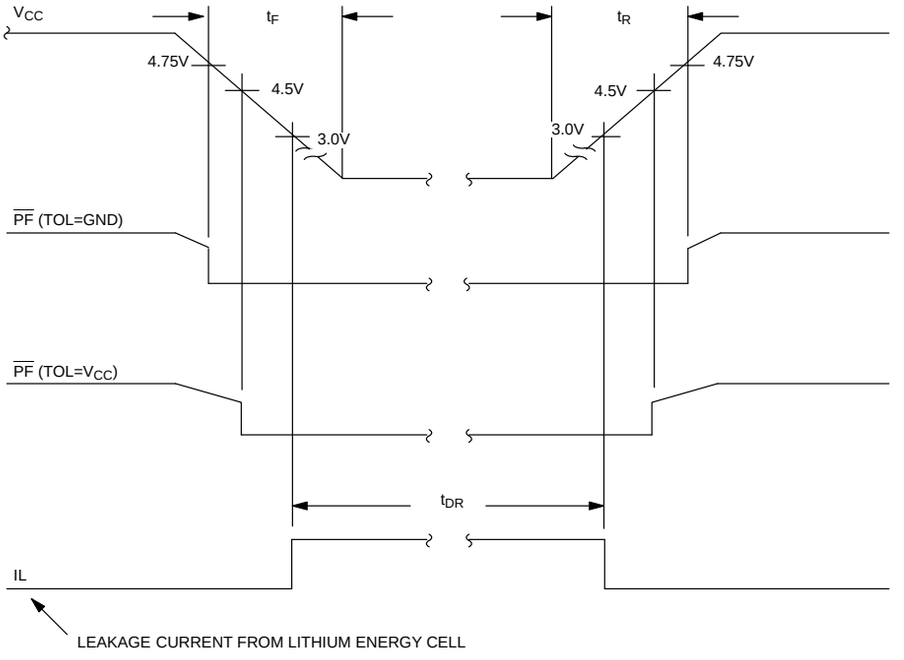
TIMING DIAGRAM: READ CYCLE FROM MEMORY



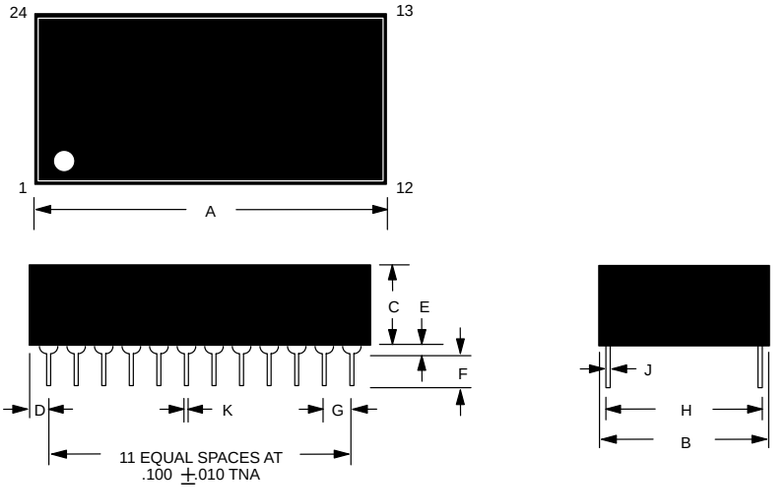
TIMING DIAGRAM: WRITE CYCLE TO DATA DIRECTION REGISTER



TIMING DIAGRAM: POWER UP – POWER DOWN



NONVOLATILE RAMPORT



DIM	MIN	MAX
A IN.	1.320	1.335
MM	33.53	33.91
B IN.	0.675	0.700
MM	17.14	17.78
C IN.	0.345	0.370
MM	8.76	9.40
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.015	0.035
MM	0.38	0.89
F IN.	0.110	0.140
MM	2.79	3.57
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53

NOTE: PINS 16 AND 20 ARE MISSING BY DESIGN