



MAX3671 Evaluation Kit

General Description

The MAX3671 evaluation kit (EV kit) is a fully assembled and tested demonstration board that simplifies evaluation of the MAX3671 low-jitter frequency synthesizer with selectable input reference. The EV kit includes slide switches to allow easy selection of different modes of operation. Clock I/Os have SMA connectors and are AC-coupled to simplify connection to test equipment. The EV kit is powered by a +3.3V supply and uses LEDs for signal status indicators.

Features

- ◆ Fully Assembled and Tested
- ◆ Slide Switches for Mode Control
- ◆ SMA Connectors and AC-Coupled Clock I/Os
- ◆ Powered by +3.3V Supply
- ◆ LED Signal Status Indicators

Ordering Information

PART	TYPE
MAX3671EVKIT+	EV Kit

+ Denotes lead(Pb)-free and RoHS compliant.

Component List

DESIGNATION	QTY	DESCRIPTION
C1, C6, C7 C11–C13, C16, C18–C22, C24–C27, C29, C30, C32–C39, C41, C42, C46–C50, C62, C63	35	0.1 μ F \pm 10% ceramic capacitors (0402)
C2	1	33 μ F \pm 5% tantalum capacitor (B case)
C3	1	2.2 μ F \pm 10% ceramic capacitor (0805)
C4	1	0.1 μ F \pm 10% ceramic capacitor (0603)
C5	1	0.01 μ F \pm 10% ceramic capacitor (0603)
C28	1	0.22 μ F \pm 10% ceramic capacitor (0402)
D1, D3, D8	3	Green SMD LEDs (1206) Panasonic LNJ311G8PRA
D2, D4, D7	3	Red SMD LEDs (1206) Panasonic LNJ211R8ARA
J1, J2, J5–J12, J14, J15, J19, J20, J22–J29, J44, J45	24	SMA connectors, edge-mount, tab center Johnson 142-0701-851
J4, J13	2	Test points Keystone 5000
L1	1	4.7 μ H \pm 20% inductor Taiyo Yuden CBC3225T4R7M

DESIGNATION	QTY	DESCRIPTION
R1–R5, R15, R16, R17, R37–R46	18	150 Ω \pm 1% resistors (0402)
R6–R11	6	49.9 Ω \pm 1% resistors (0402)
R12, R13, R14, R18, R21, R22	6	332 Ω \pm 1% resistors (0603)
R23, R24, R25	3	10k Ω \pm 1% resistors (0603)
S1	1	Switch, momentary, SPST-NO Panasonic EVQQ2S02W
S2, S3, S5	3	Switches, slide, SPDT Copal Electronics CUS-12TB
S6, S7, S8	3	Switches, slide, SP4T Copal Electronics CUS-14TB
S9, S10	2	Switches, slide, SP3T Copal Electronics CUS-13TB
TP3, TP20	2	Test points Keystone 5000
U1, U2, U4	3	Dual inverters (6 SC-70) TI SN74LVC2G14DCKR
U7	1	Low-jitter, frequency synthesizer with selectable input reference (56 TQFN) Maxim MAX3671ETN+
None	1	PCB: MAX3671 EV Kit+ Circuit Board, Rev A

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Quick Start

- Set the slide switches to the following settings:
 PLL_BYPASS = NORMAL
 SEL_CLK = REFCLK0
 DM = 62.5M
 DA = 125M
 DB = 125M
 $\overline{\text{OUTA_EN}}$ = A0, A1
 $\overline{\text{OUTB_EN}}$ = B0
 FB_SEL = INTERNAL
- Connect a +3.3V supply to VCC (J13) and GND (J4). Set the supply current limit to 450mA.
- Using SMA cables, connect a low-jitter 62.5MHz differential clock source to the REFCLK0 input. Verify that the green LEDs switch on for $\overline{\text{IN0FAIL}}$ and LOCK.
- Using SMA cables, connect the OUTA0 output to test equipment. Terminate all unused enabled outputs ($\overline{\text{OUTB0}}$ and OUTA1).

Detailed Description

The MAX3671 EV kit simplifies evaluation by providing the hardware needed to evaluate all the MAX3671 functions. Table 1 contains functional descriptions for the switches and indicators.

Clock Inputs

The clock inputs (REFCLK0, REFCLK1, FB_IN) are AC-coupled at the SMA connectors and have on-board 100 Ω differential terminations. For optimal jitter performance it is critical to use a low-jitter, differential, square-wave clock source. If such a source is not available, the clock inputs can be driven with a single-ended sinusoidal or square-wave clock source for functional testing.

Clock Outputs

The clock outputs (OUTA[3:0], OUTB[4:0]) have on-board DC-biasing and are AC-coupled at the SMA connectors to allow direct connection to 50 Ω -terminated test equipment. Unused outputs should be disabled (using switches S9 and S10) or have 50 Ω terminations placed on the SMA connectors.

Table 1. Switch and Indicator Descriptions

COMPONENT	NAME	FUNCTION
S1	MASTER RESET	Momentary switch to reset internal dividers. Not required at power-up. If the output divider settings (DA, DB) are changed on the fly, a reset is required to phase align the outputs.
S2	PLL_BYPASS	Selects normal PLL operation or PLL bypass.
S3	SEL_CLK	Selects the reference clock input.
S5	FB_SEL	Selects internal or external feedback for the PLL. If external is selected, connect any of the A-group or B-group outputs to the FB_IN input. If DA \neq DB, a B-group output must be used.
S6	DM	Selects the frequency of the reference clock inputs.
S7	DA	Selects the frequency of the A-group clock outputs.
S8	DB	Selects the frequency of the B-group clock outputs.
S9	$\overline{\text{OUTA_EN}}$	Selects which A-group outputs are enabled (see Note).
S10	$\overline{\text{OUTB_EN}}$	Selects which B-group outputs are enabled (see Note).
D1, D2	$\overline{\text{IN0FAIL}}$	REFCLK0 failure indicator (green = pass, red = fail).
D3, D4	$\overline{\text{IN1FAIL}}$	REFCLK1 failure indicator (green = pass, red = fail).
D7, D8	LOCK	PLL lock indicator (green = PLL locked, red = PLL not locked).

Note: Setting $\overline{\text{OUTA_EN}}$ = "—" and $\overline{\text{OUTB_EN}}$ = "B0" at the same time enables a factory test mode and is not a valid mode of operation.

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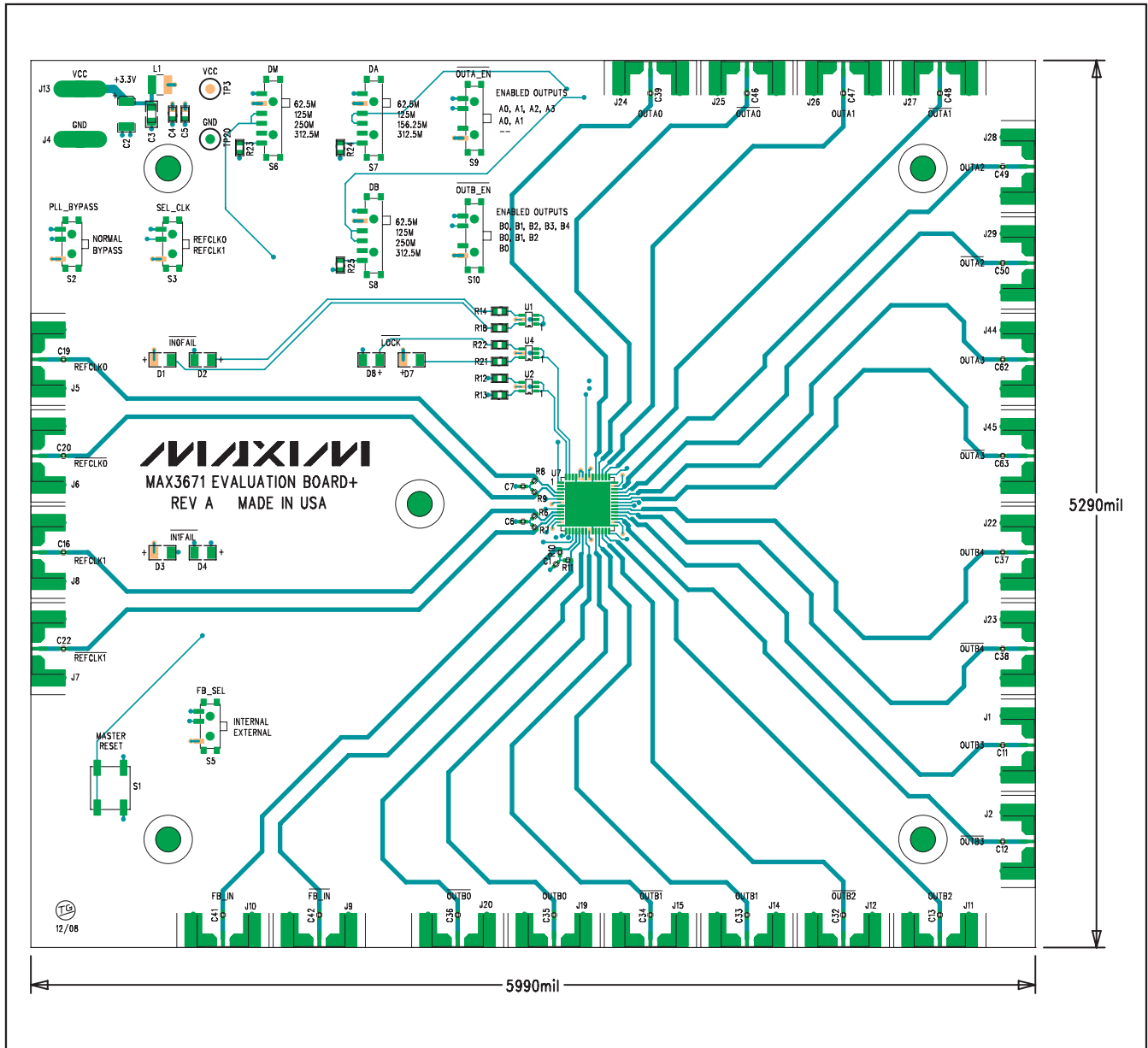


Figure 2. MAX3671 EV Kit Component Placement Guide—Component Side

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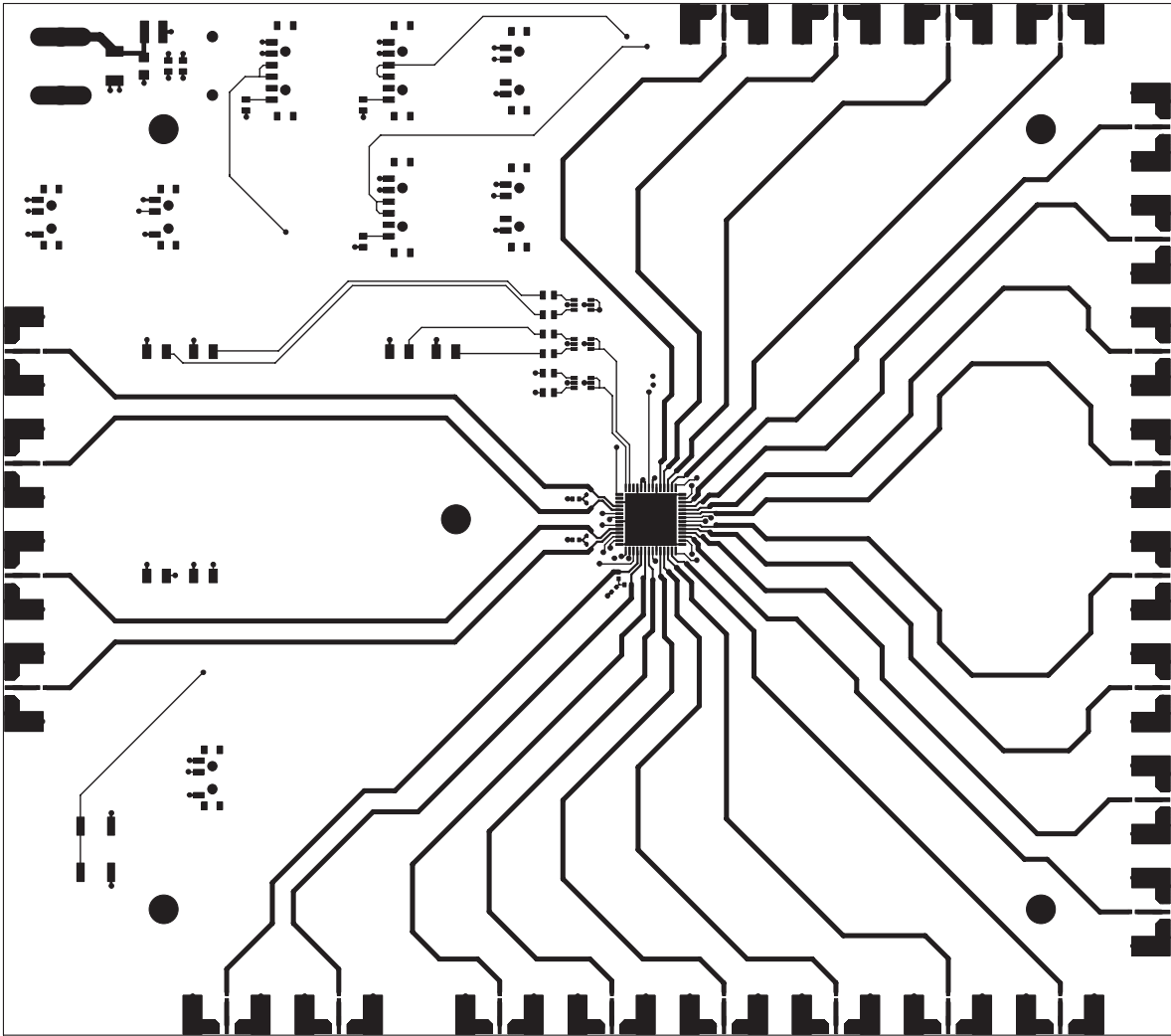


Figure 3. MAX3671 EV Kit PCB Layout—Component Side

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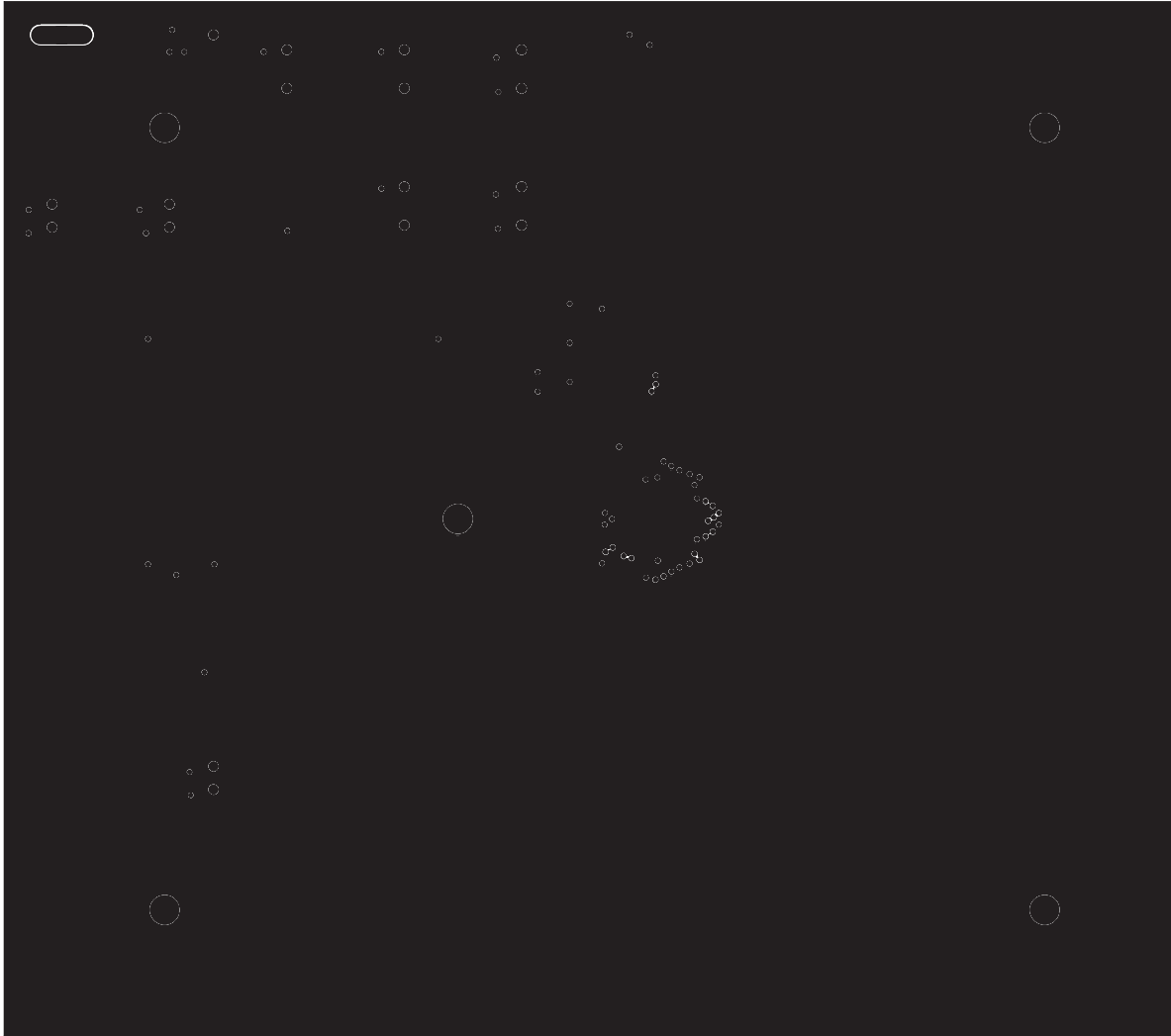


Figure 4. MAX3671 EV Kit PCB Layout—Ground Plane

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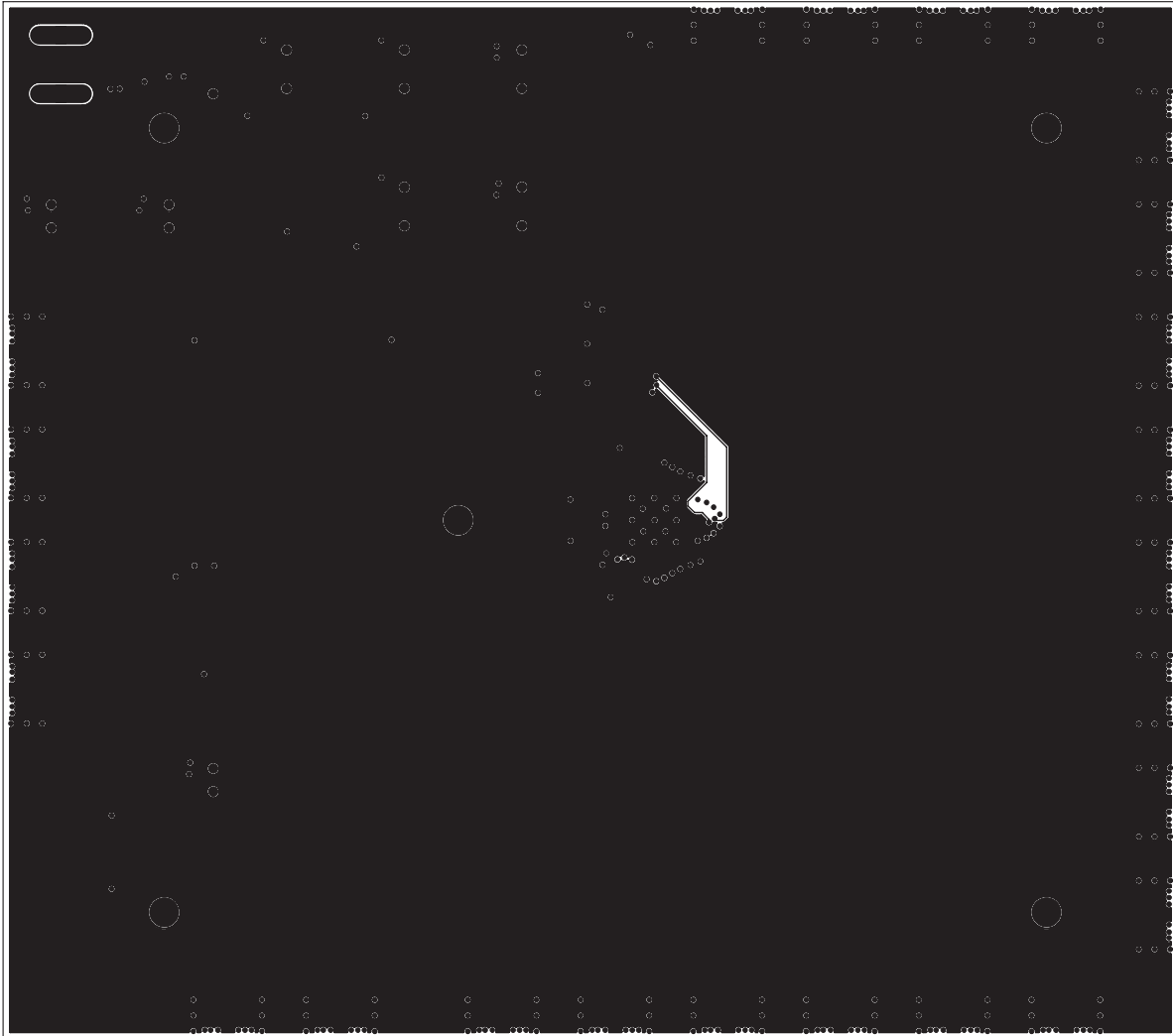


Figure 5. MAX3671 EV Kit PCB Layout—Power Plane

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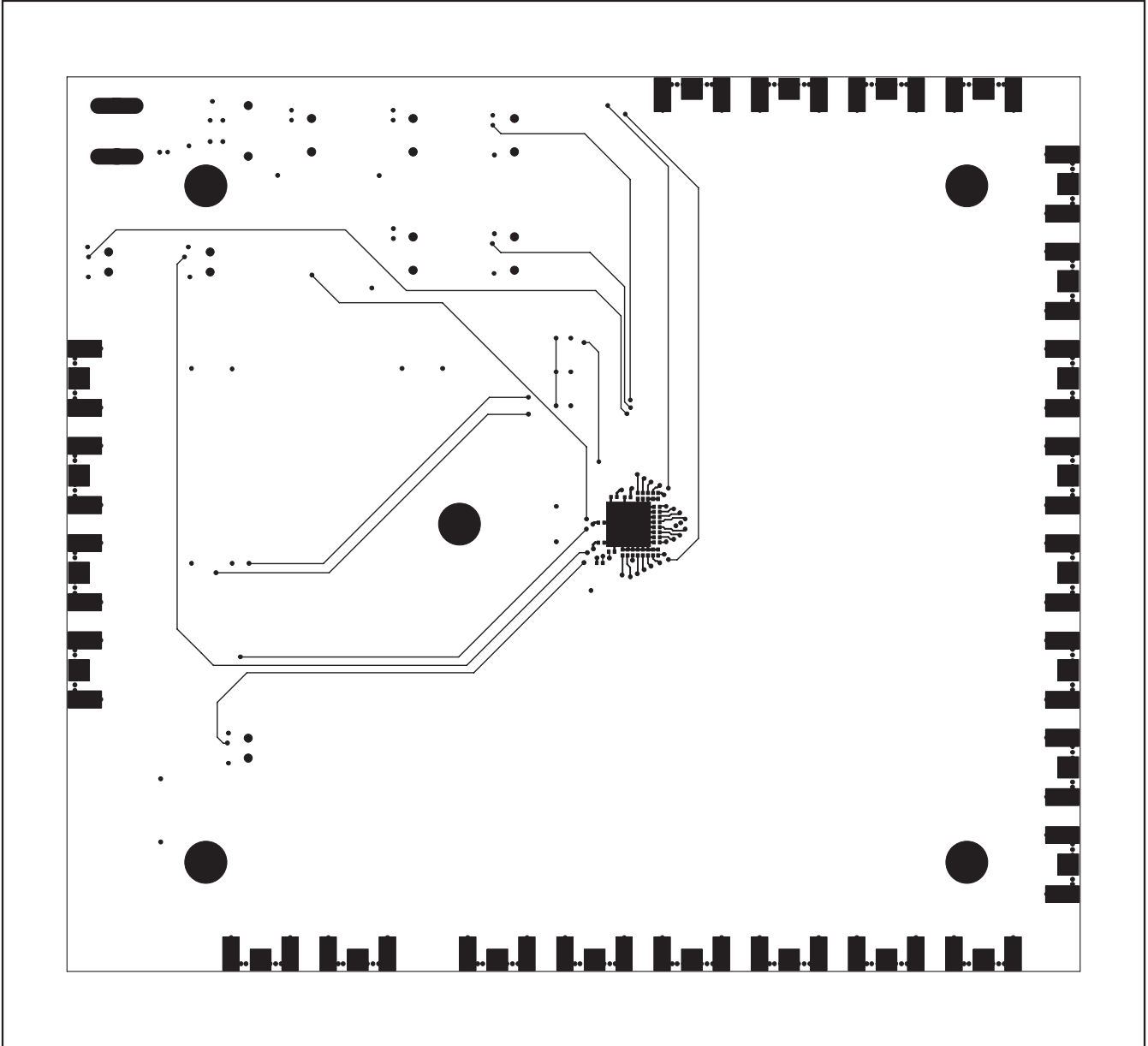


Figure 6. MAX3671 EV Kit PCB Layout—Solder Side

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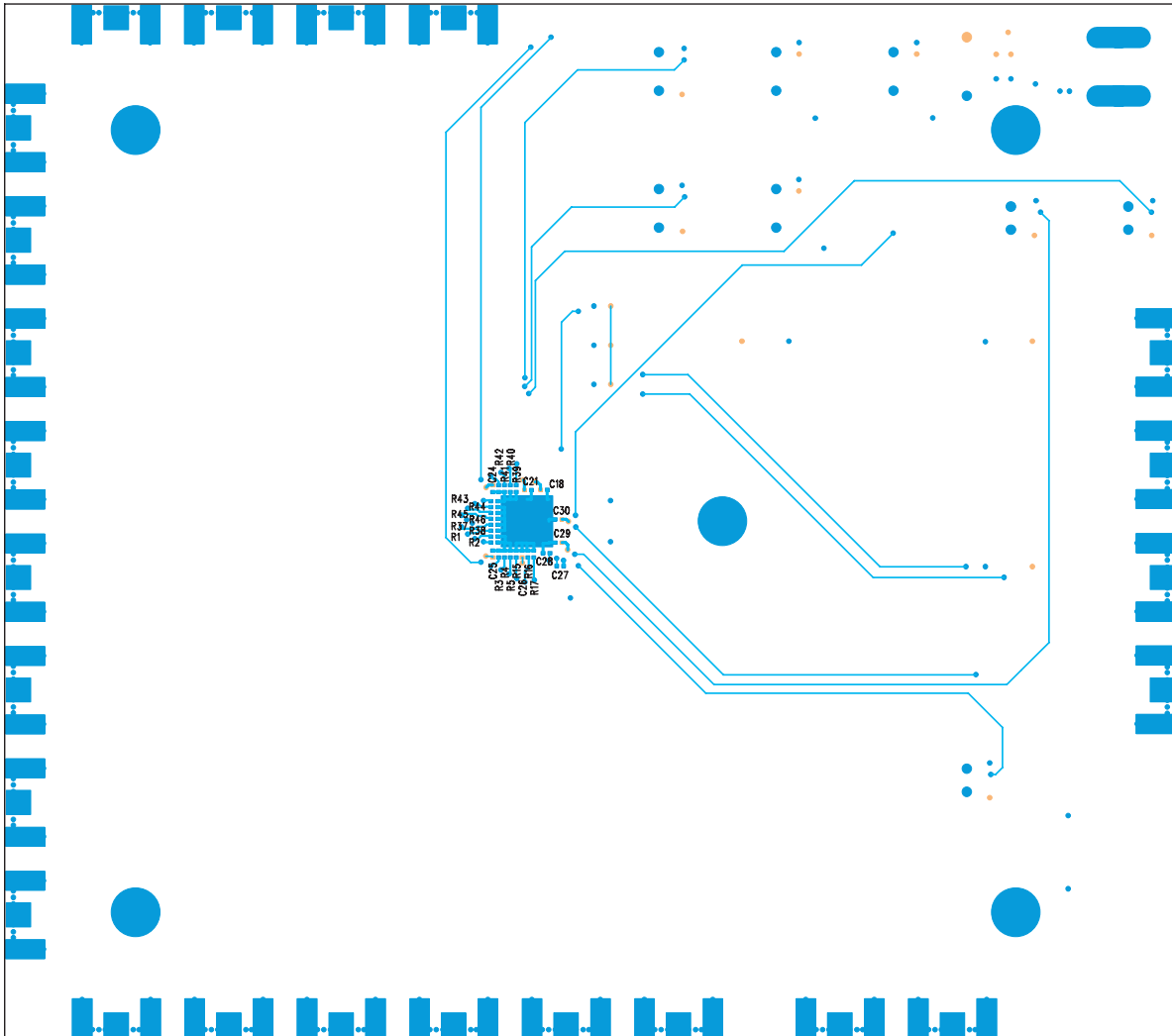


Figure 7. MAX3671 EV Kit Component Placement Guide—Solder Side

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