MAXIM

MAX3975 Evaluation Kit

Evaluates: MAX3975

General Description

The MAX3975 evaluation kit (EV kit) is an assembled demonstration board that provides complete optical and electrical evaluation of the MAX3975 VCSEL driver.

The EV kit is composed of two independent sections, one optical and one electrical, with a score line between the sections for optional separation. The output of the electrical section has an SMA connector that can be connected to a 50Ω terminated oscilloscope. The output of the optical section is configured for attachment to the flex cable of a user-provided VCSEL TOSA. Bias and modulation currents are manually set with variable resistors.

Users can add the DS1862 controller IC with accompanying hardware and software for closed-loop testing. The DS1862 incorporates an automatic power control (APC) feedback loop, extinction ratio control, and digital diagnostics. Programming is accomplished through an I²C-compatible interface, which can also be used to access diagnostic functionality.

Features

♦ **Assembled and Tested**

♦ **Allows Optical and Electrical Evaluation**

♦ **Programmable Bias and Modulation Currents**

♦ **AC-Coupling Provided On-Board**

Ordering Information

PART	TEMP RANGE	IC PACKAGE
MAX3975EVKIT	0°C to +85°C	20 UCSP-20

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Component List

DESIGNATION	QTY	DESCRIPTION
C1–C5, C9, C13, C16, C20, C24–C27	13	0.1µF ±5% ceramic capacitors (0402)
C6, C14, C23	3	10µF ±5% tantalum capacitors (B case)
C7, C10, C12, C15	4	1000pF ±5% ceramic capacitors (0402)
C8, C11, C18	3	0.01µF ±5% ceramic capacitors (0402)
C17, C21	0	0.1µF ±5% ceramic capacitors (0402) (Not installed)
C22, C28	0	1000pF ±5% ceramic capacitors (0402) (Not installed)
J1–J5	5	SMA connectors (edge mount, tab contact) Johnson 142-0701-851
J7, J10, J11, J18, J19, TP1–TP9, TP22, TP23	16	Test points Digi-Key 5000K-ND
TP10–TP21, TP24	0	Test points Digi-Key 5000K-ND (Not installed)
JU1, JU3, JU4, JU7	4	2-pin headers, 0.1in centers Digi-Key S1012E-36-ND
JU2, JU5, JU6	3	3-pin headers, 0.1in centers Digi-Key S1012E-36-ND

DESIGNATION	QTY	DESCRIPTION
JU8, JU11, JU13, JU16	0	2-pin headers, 0.1in centers Digi-Key S1012E-36-ND (Not installed)
JU12, JU14, JU15	0	3-pin headers, 0.1in centers Digi-Key S1012E-36-ND (Not installed)
None	7	Shunts Digi-Key S9000-ND
L1, L3, L6	3	1µH ±10% chip inductors (0805) Taiyo Yuden CK21251R0M-T
L2	0	1µH ±10% chip inductor (0805) Taiyo Yuden CK21251R0M-T (Not installed)
L5	0	VCSEL TOSA with 50Ω flex Advanced Optical Components HFE6190-561 (Not installed)
R1, R7	2	1kΩ ±1% resistors (0402)
R2, R4, R5, R16	4	825Ω ±1% resistors (0402)
R3, R6, R10, R11	4	20kΩ variable resistors
R8	1	511kΩ ±1% resistor (0402)
R9	1	7.5kΩ ±1% resistor (0402)
R12	1	26.7kΩ ±1% resistor (0402)

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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

MAX3975 Evaluation Kit

_____Component List (continued)

DESIGNATION	QTY	DESCRIPTION
R13	1	20kΩ ±1% resistor (0402)
R14, R15, R17, R18, R19	0	4.7kΩ ±5% resistor (0402) (Not installed)
R21	1	10kΩ ±1% resistor (0402)
U1, U2	2	MAX3975UBA-T (20 UCSP)
U3	1	p-Channel MOSFET Fairchild FDN302P
U4	1	Dual p-channel MOSFET Fairchild FDC6306P
U5	1	MAX9039BEBT-T (6 UCSP)
U6	0	DS1862B+ (25 CSBGA) (Not installed)
None	1	PCB: MAX3975 EV kit circuit board, Rev B

_____Electrical Quick Start

The electrical section of the evaluation board requires a positive and negative supply in order for the output termination to electrically emulate the characteristics of a VCSEL. For more information, refer to Figure 1 in the MAX3975 data sheet. If desired, the electrical section of the board can be separated from the optical section by bending the board length-wise until they snap apart. Use the following procedure to configure the electrical section for evaluation.

1) Place a shunt on JU3. This connects the BIASSET pin to the $R_{BIASSET}$ variable resistor (R11).

2) Place a shunt on JU4. This connects the MODSET pin to the R_{MODSET} variable resistor (R10).

3) Place a shunt on JU1. This enables the driver output by connecting the DISABLE pin to V_{EE}.

4) Adjust R11 until there is 2.4kΩ resistance between TP5 and TP6. This sets the output bias current to approximately 5mA.

5) Adjust R10 until there is 2.4kΩ resistance between TP4 and TP6. This sets the output modulation current to approximately 5mA.

6) Apply a 10Gbps differential signal (650mV$_{P-P}$) between SMA connectors J1 (IN+) and J2 (IN-).

7) Connect an oscilloscope with a 50Ω termination to SMA connector J3 (OUT). The output must be DC-coupled to the oscilloscope.

8) Connect a +1.2V supply to J7 (V_{CC}), a -2.1V supply to J11 (V_{EE}), and the supply ground to J10 (GND).

9) Verify that there is +1.2V at the V_{CC} pin by measuring the voltage from TP8 to TP7 and adjusting the voltage at J7 accordingly.

10) Verify that there is -2.1V at the V_{EE} pin by measuring the voltage from TP6 to TP7 and adjusting the voltage at J11 accordingly.

11) Test the driver output current monitor by measuring the voltage from TP3 to TP6.

12) Adjust the variable resistor R11 until the desired bias current is achieved.

13) Adjust the variable resistor R10 until the desired modulation current is achieved.

_____Optical Quick Start

The optical evaluation board requires installation of a single-ended cathode-driven VCSEL such as Advanced Optical Components HFE6190-561 VCSEL TOSA (not included with EV Kit). The interface pins are for 50Ω flex circuit with 31-mil pad pitch. The HFE6190-561 flex cable should be soldered to the board so that the TOSA points toward the top of the board. See Figure 1. If the DS1862 controller IC is to be used during the evaluation, it is best to install the DS1862 and the remainder of the components before installing the TOSA.
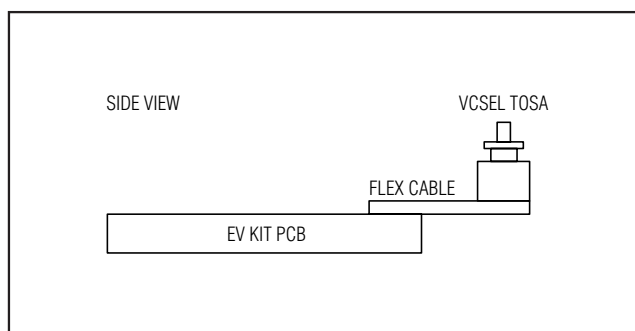

Figure 1. VCSEL TOSA Assembly

Open-Loop Evaluation

1) Place a shunt on the "MANUAL" side of JU2. This connects the driver BIASSET pin to the $R_{BIASSET}$ variable resistor (R6).

2) Place a shunt on the "MANUAL" side of JU5. This connects the driver MODSET pin to the R_{MODSET} variable resistor (R3).

3) Move the shunt on JU6 to the side labeled GND.

4) Pull the disable pin low by placing a shunt on JU7.

5) Adjust R6 until there is 3kΩ resistance between TP2 and ground. This sets the output bias current to approximately 4mA.

6) Adjust R3 until there is 3kΩ resistance between TP1 and ground. This sets the output modulation current to approximately 4mA.

7) Apply a 10Gbps differential signal (650mV$_{P-P}$) between SMA connectors J4 (IN+) and J5 (IN-).

8) Connect a +3.3V supply to V$_{CC1}$ (J19) and the supply ground to GND (J18). The power-on-reset circuit will apply power to the VCSEL when V$_{CC1}$ reaches approximately 2.9V.

9) Verify that there is +3.3V at the V$_{CC}$ pin by measuring the voltage from TP22 to ground and adjusting the voltage at J19 accordingly.

10) Use a multimode fiber to connect the VCSEL TOSA to an optical-to-electrical converter or optical power meter.

11) Adjust the bias current with variable resistor R6 and the modulation current with variable resistor R3 until the desired optical average power and modulation amplitude is achieved.

12) Test the driver output current monitor by measuring the voltage from MONITOR (TP9) to ground.

Closed-Loop Evaluation Using DS1862

Closed-loop evaluation at 10Gbps is most easily accomplished using the *HFRD-19.2: 850nm XFP Transceiver* reference design. Documentation for the reference design is available at www.maxim-ic.com/AN3730. If the reference design cannot be used for the evaluation continue with the steps outlined below.

Closed-loop evaluation requires installation of the components noted as (Not Installed) in the *Component List*. The following items are also required:

1) DS3900 serial communication module and breakout board.

2) RS-232 serial cable with standard DB-9 connector.

3) DS1862 evaluation software (GUI). The latest version of the EV kit software can be downloaded at www.maxim-ic.com/DS1862EVsoftware.

For technical support and to obtain items 1 and 3, contact Maxim at (972) 371-4076 between 8AM and 5PM Central Time or email: MixedSignal.Apps@dalsemi.com.

Follow these steps to configure the EV kit for closed-loop operation with the DS1862.

1) Place a shunt on the "DS1862" side of JU2. This connects the driver BIASSET pin to the DS1862 BIASSET pin.

2) Place a shunt on the "DS1862" side of JU5. This connects the driver MODSET pin to the DS1862 MODSET pin.

3) Move the shunt on JU6 to the side labeled FETG. This connects the safety fault output of the DS1862 to the power MOSFET gate.

4) Place shunts on JU7, JU8, JU11, JU13, and JU16.

5) Place shunts on the "L" side of JU12, JU14, and JU15.

6) Connect a +3.3V supply to V$_{CC1}$ (J19) and the supply ground to GND (J18). The power-on-reset circuit will apply power to the VCSEL and V$_{CC2}$ when V$_{CC1}$ reaches approximately 2.9V.

7) Verify that there is +3.3V at the supply pins by measuring the voltage from TP22 (V$_{CC1}$) to ground and TP24 (V$_{CC2}$) to ground. Adjust the voltage at J19 as needed.

8) Connect a +3.3V supply to the DS3900 breakout board. Use the serial cable to connect the DS3900 to the serial port of a computer.

9) Use wires with clip-ends to connect the DS3900 data (SDA), clock (SCL), and ground (GND) test points to the respective SDA, SCL, and GND test points on the MAX3975 EV kit.

10) Open the DS1862 EV kit software and verify communication with the controller. Refer to the DS1862 data sheet for configuring I/O ports and thresholds.

11) Use the software to set the optical average power and to load the temperature-indexed lookup table that controls optical modulation amplitude.

Adjustment and Control Descriptions (see Quick Start first)

COMPONENT		NAME	FUNCTION
OPTICAL	ELECTRICAL		
JU7	JU1	DISABLE	Enables/disables the driver output currents. Place a shunt on JU1 or JU7 to enable the output currents.
—	JU3	—	Connects the BIASSET pin to the $R_{BIASSET}$ variable resistor (R11).
—	JU4	—	Connects the MODSET pin to the R_{MODSET} variable resistor (R10).
JU2	—	—	Connects the BIASSET pin to either the $R_{BIASSET}$ variable resistor (R6) or to the BIASSET pin of the DS1862. Shunt pins 1 and 2 to use the $R_{BIASSET}$ resistor. Shunt pins 2 and 3 to use the DS1862.
JU5	—	—	Connects the MODSET pin to either the R_{MODSET} variable resistor (R3) or the MODSET pin of the DS1862. Shunt pins 1 and 2 to use the R_{MODSET} resistor. Shunt pins 2 and 3 to use the DS1862.
R6	R11	$R_{BIASSET}$	Adjusts the driver bias current. Rotate clockwise to increase the bias current.
R3	R10	R_{MODSET}	Adjusts the driver modulation current. Rotate clockwise to increase the modulation
JU6	—	—	Connects the MOSFET gate to either ground or the FETG pin of the DS1862.
JU8	—	V_{CC2}	Connects the V_{CC1} power plane to the V_{CC2} power plane.
JU11	—	MOD-DESEL	Enables/disables communication with the DS1862 over the 2-wire interface bus (SDA and SCL). Place a shunt on JU11 to enable communication on the bus.
JU12	—	SC-TX-LOS	Sets the SC-TX-LOS pin of the DS1862 high or low. Shunt pins 1 and 2 for low. Shunt pins 2 and 3 for high.
JU13	—	P-DOWN	Enables/disables power-down mode of the DS1862. Remove the shunt to enable power-down mode.
JU14	—	SC-RX-LOS	Sets the SC-RX-LOS pin of the DS1862 high or low. Shunt pins 1 and 2 for low. Shunt pins 2 and 3 for high.
JU15	—	SC-RX-LOL	Sets the SC-RX-LOL pin of the DS1862 high or low. Shunt pins 1 and 2 for low. Shunt pins 2 and 3 for high.
JU16	—	TX-D	Control pin of the DS1862 used to enable/disable the bias and modulation currents. Place a shunt on JU16 to enable the currents.

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Figure 2. MAX3975 EV Kit Schematic—Electrical Section
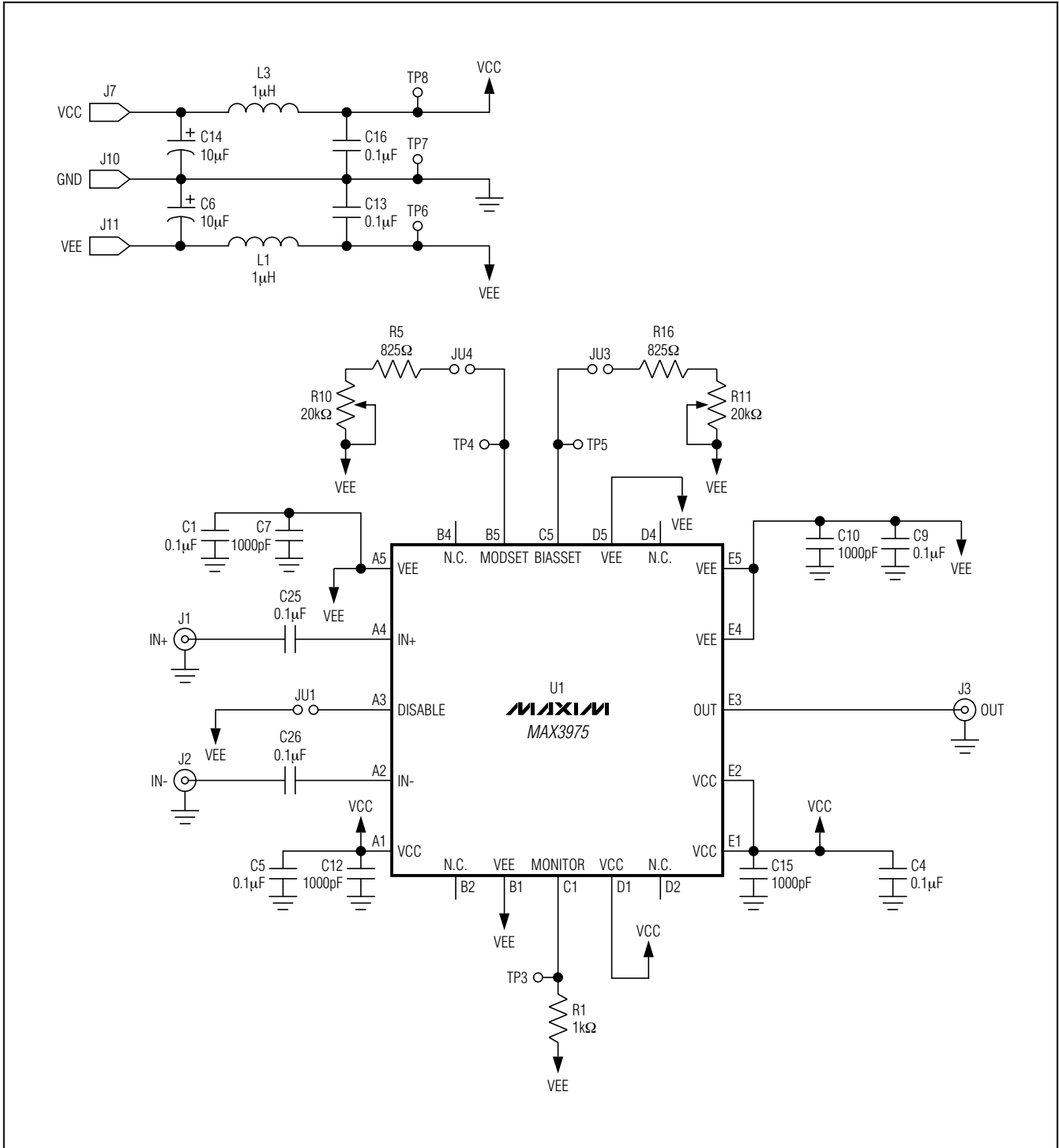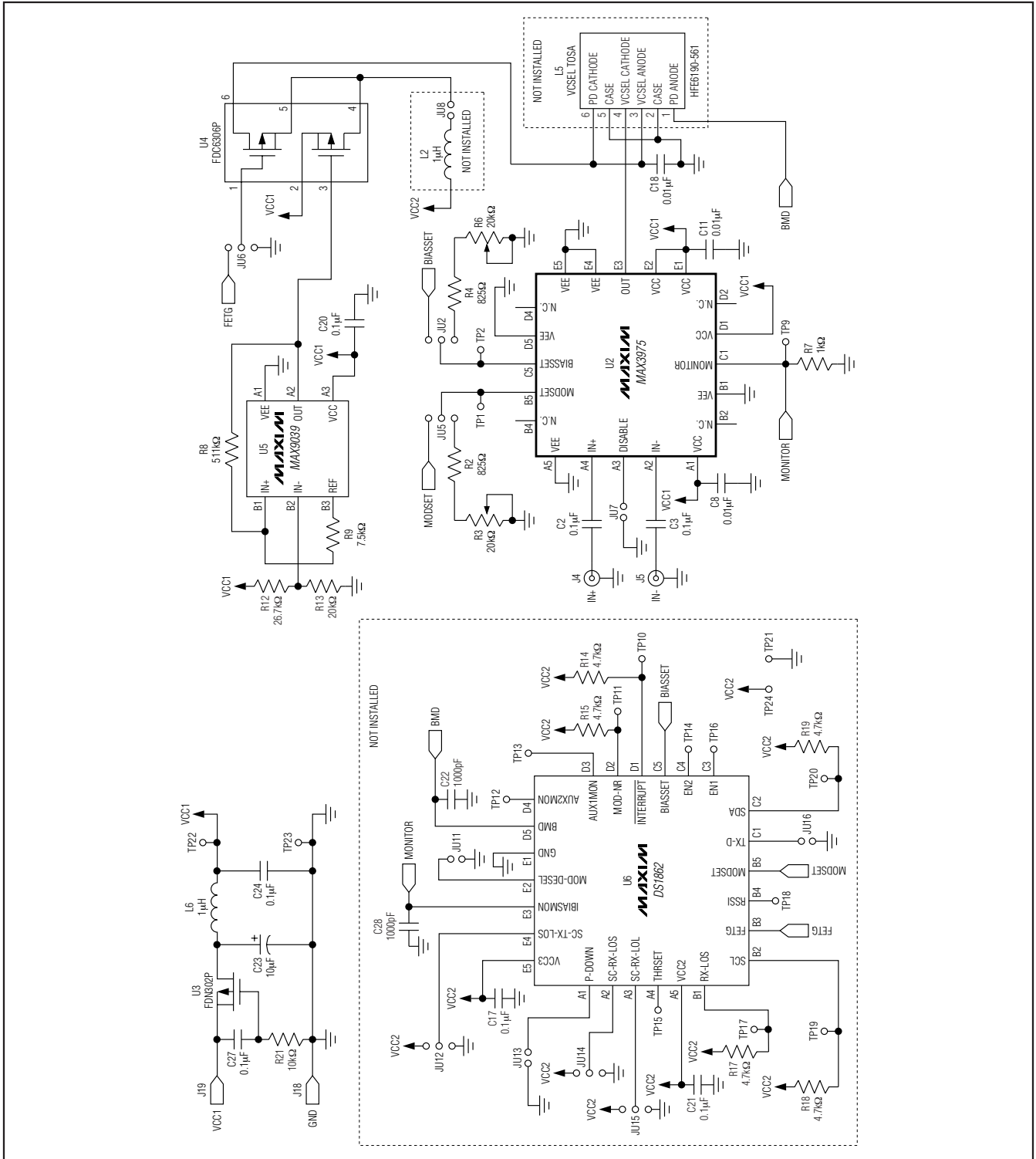
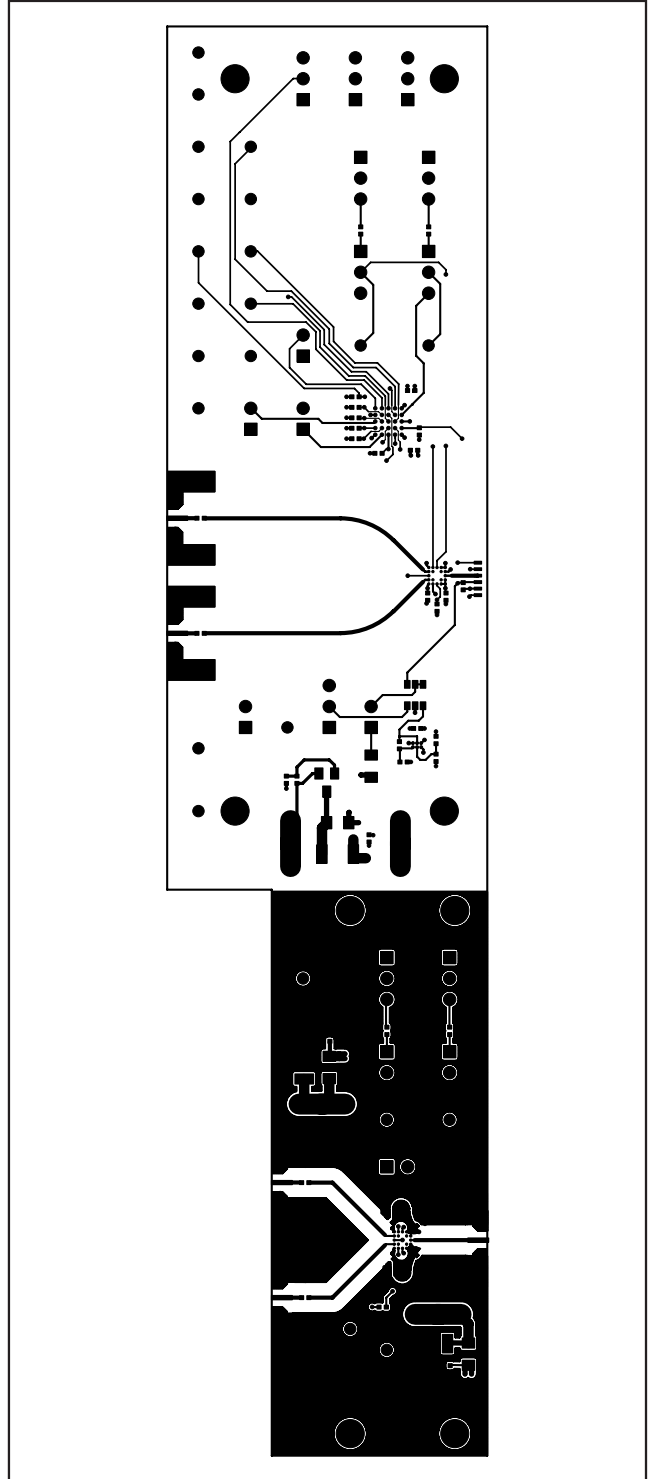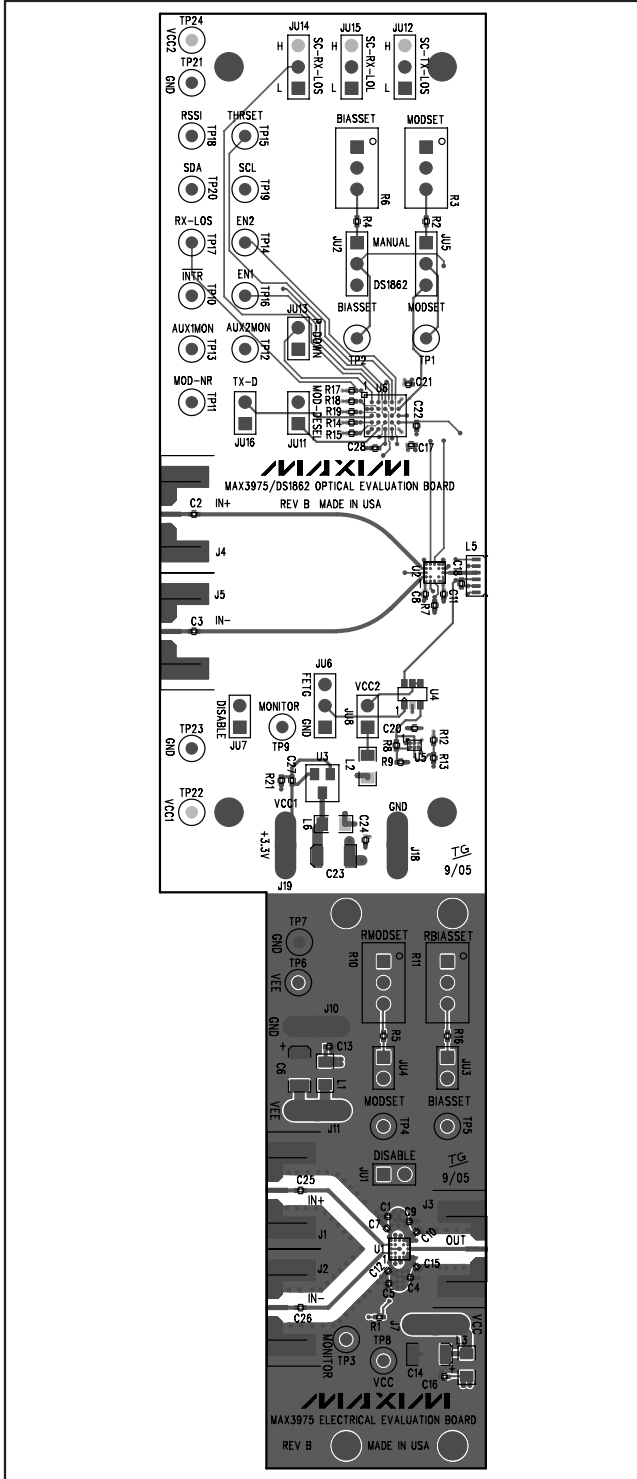Figure 3. MAX3975 EV Kit Schematic—Optical Section

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Figure 4. MAX3975 EV Kit Component Placement Guide—
Component Side

Figure 5. MAX3975 EV Kit PCB Layout—Component Side

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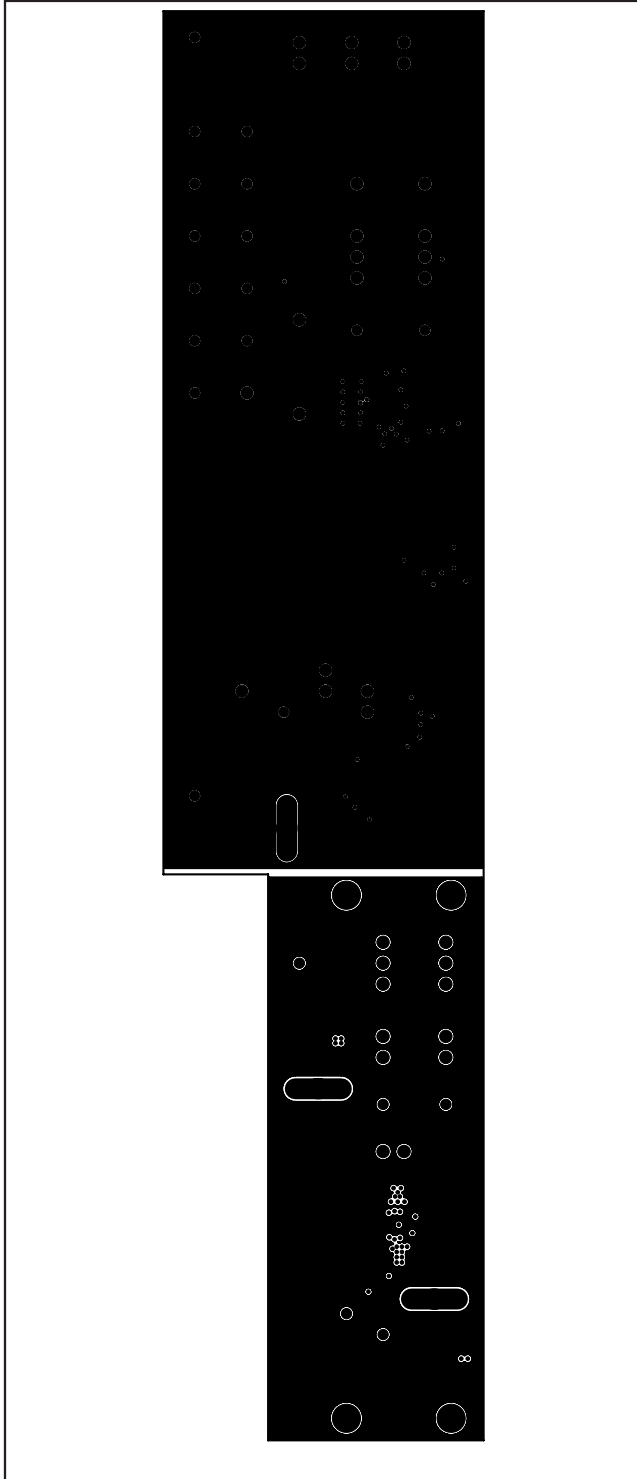
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Figure 6. MAX3975 EV Kit PCB Layout—Ground Plane

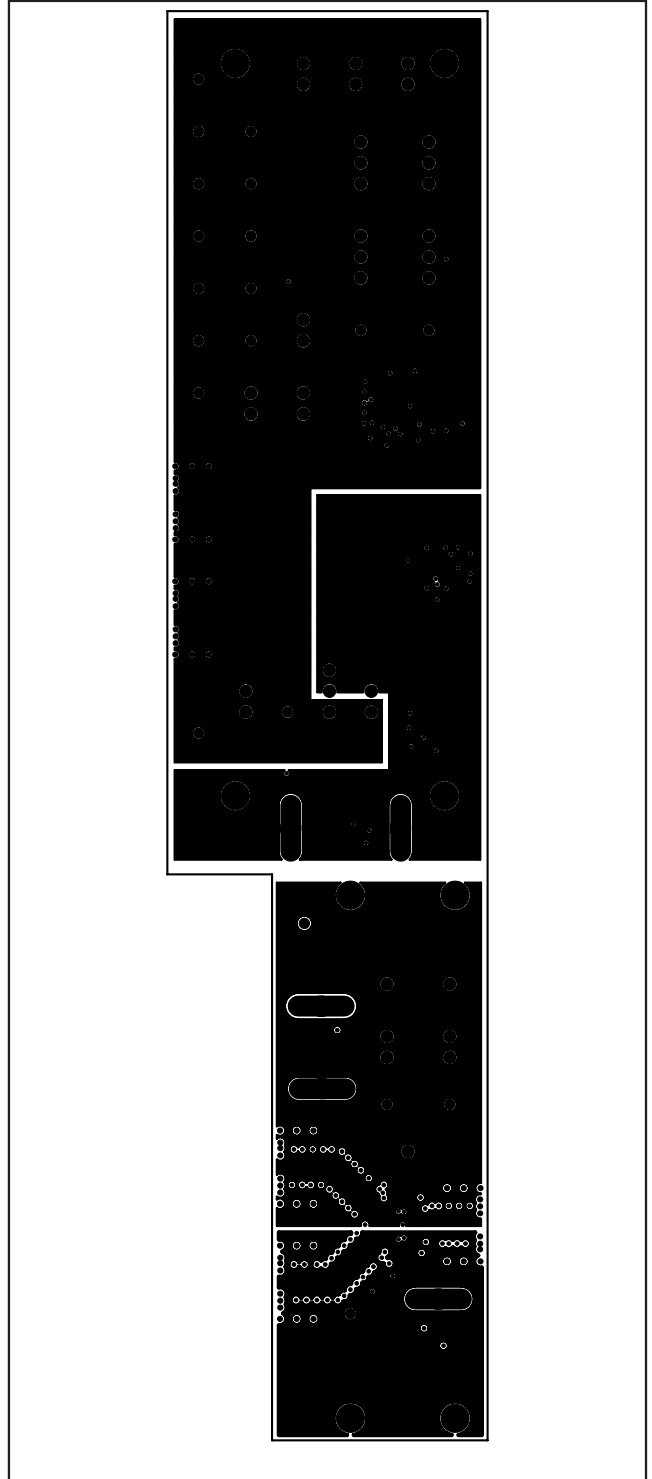Figure 7. MAX3975 EV Kit PCB Layout—Power Plane

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Figure 8. MAX3975 EV Kit PCB Layout—Solder Side

_____**Revision History**

Pages changed at Rev 1: 1–9

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