MicroLeadFrame Packages Pad Landing Recommendations

1. Introduction

This application note provides PCB designers with a set of guidelines for successful board mounting of Atmel's DataFlash memories housed in the MicroLeadFrame® package. The MicroLeadFrame package (MLF®) is a near CSP plastic encapsulated package with a copper leadframe substrate. This is a leadless package where electrical contact to the PCB is made by soldering the lands on the bottom surface of the package to the PCB, instead of the conventional formed perimeter leads. The ePad technology enhances the thermal and electrical properties of the package. The exposed die attach paddle on the bottom efficiently conducts heat to the PCB and provides a stable ground through down bonds and electrical connections through conductive die attach material. The design of the MicroLeadFrame package also allows for flexibility. Its enhanced electrical performance enables the standard 2 GHz operating frequency to be increased up to 10 GHz with some design considerations.

Figure 1-1. MLF Package Photo and Cross Section Drawings

MLF Top View

MLF Bottom View

Punch Singulated

Saw Singulated, Full Lead

Saw Singulated, Full Pullback

2. Surface Mount Considerations for MLF Packages

For devices to perform at their peak, special considerations are needed to properly design the motherboard and to mount the package. For enhanced thermal, electrical, and board level performance, the exposed pad on the package needs to be soldered to the board using a corresponding thermal pad on the board. Furthermore, for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region. The PCB footprint design needs to be considered from dimensional tolerances due to the package, PCB, and the assembly factors.

A number of factors may have a significant effect on mounting the MLF package on the board and the quality of the solder joints. Some of these factors include: amount of solder paste coverage in the thermal pad region, stencil design for peripheral and thermal pad region, type of vias, board thickness, lead finish on the package, surface finish on the board, type of solder paste, and reflow profile. This applications note provides the guidelines for this purpose. It should be emphasized that this is just a guideline to help the user in developing the proper motherboard design and surface mount process. Actual studies as well as development effort maybe needed to optimize the process as per user's surface mount practices and requirements.

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3. PCB Design Guidelines

As shown in Figure 3-1, the lands on the package bottom side are rectangular in shape with rounded edges on the inside. Since the package does not have any solder balls, the electrical connection between the package and the motherboard is made by printing the solder paste on the motherboard and reflowing it after the component placement. In order to form reliable solder joints, special attention is needed in designing the motherboard pad pattern and the solder paste printing.

3.1 Perimeter Pads Design

Typically the PCB pad pattern for an existing package is designed based on guidelines developed within a company or by following industry standards such as IPC-SM-782. However, since the MLF is a new package and the industry guidelines have not been developed yet for a PCB pad pattern design, the development of proper design considerations may require some experimental trials. For the purpose of this document, IPC's methodology is used here for designing PCB pad pattern. However, because of the exposed die paddle and the package lands on the bottom side of the package, certain constraints are added to IPC's methodology. The pad pattern developed here includes considerations for lead and package tolerances.

Figure 3-1 shows the bottom and side views of full lead option, indicating the dimensions needed to design the pad pattern for the PCB. Although, the leads are pulled back in the design, the PCB pad pattern does not need to change for these options. Since most packages are square with dimension D equal to dimension E and the leads are along the E direction for dual packages, the side view dimensions are used to determine the land length on the PCB.

Figure 3-1. MLF (Full Lead Design) Component Dimensions Needed for PCB Land Pattern

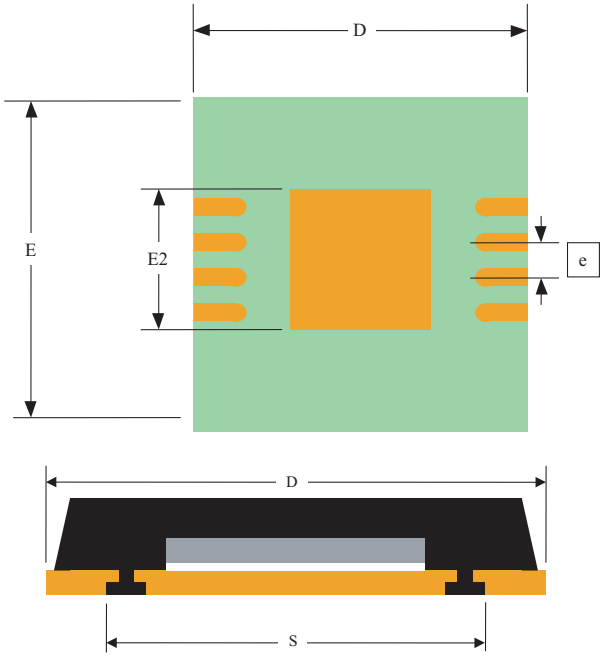
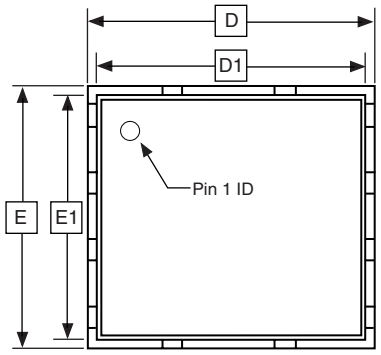
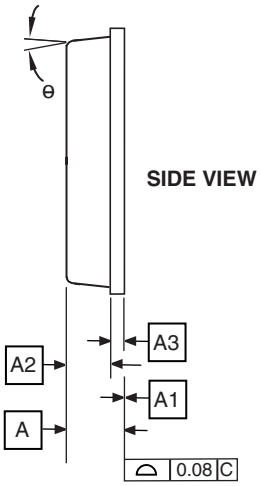


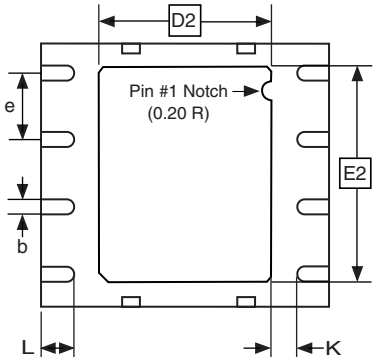
Figure 3-2. PCB Land Pattern Dimensions for 6 x 5 x 1.00 mm Body



TOP VIEW



SIDE VIEW

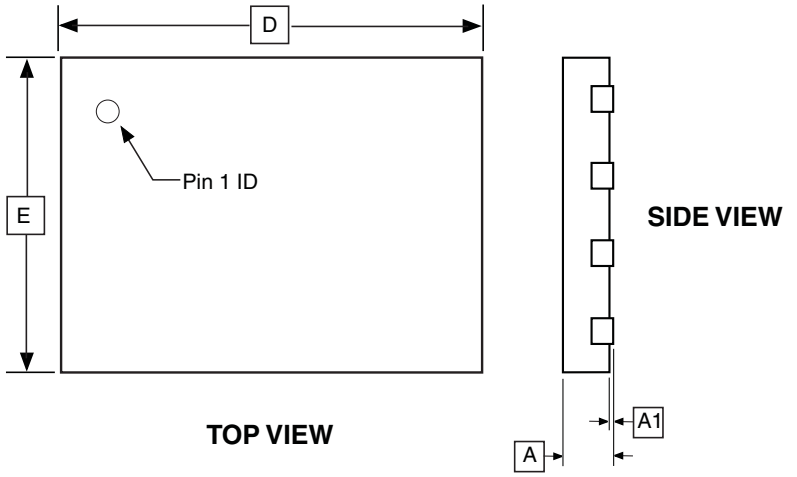


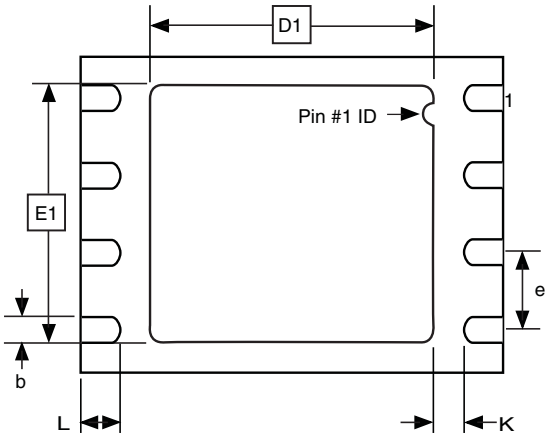
BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	0.85	1.00	
A1	–	–	0.05	
A2		0.65 TYP		
A3		0.20 TYP		
b	0.35	0.40	0.48	
D	5.90	6.00	6.10	
D1	5.70	5.75	5.80	
D2	3.20	3.40	3.60	
E	4.90	5.00	5.10	
E1	4.70	4.75	4.80	
E2	3.80	4.00	4.20	
e		1.27		
L	0.50	0.60	0.75	
θ			12°	
K		1.30 REF		

Figure 3-3. PCB Land Pattern Dimensions for 8 x 6 x 1.0 mm Body





COMMON DIMENSIONS
(Unit of Measure = mm)

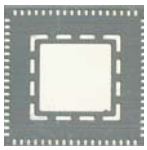
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.00	
A1	–	–	0.05	
b	0.35	0.40	0.48	
D	7.90	8.00	8.10	
D1	6.30	6.40	6.50	
E	5.90	6.00	6.10	
E1	4.70	4.80	4.90	
e		1.27		
L	0.45	0.50	0.55	
K		0.30 REF		

3.2 Thermal Pad and Via Design

The MLF package is designed to provide a superior thermal performance. This is partly achieved by incorporating an exposed die paddle on the bottom surface of the package. However, in order to take full advantage of this feature, the PCB must have features to effectively conduct heat away from the package. This can be achieved by incorporating a thermal pad and thermal vias on the PCB. While a thermal pad provides a solderable surface on the top surface of the PCB (to solder the package die paddle on the board), the thermal vias are needed to provide a thermal path to the inner and/or bottom layers of the PCB to remove the heat.

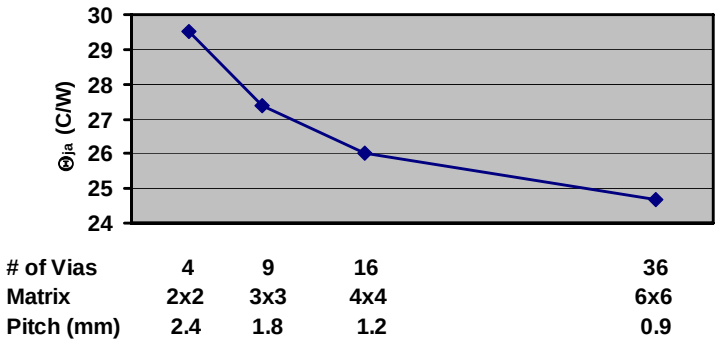
Normally, the size of the thermal pad should at least match the exposed die paddle size. However, depending upon the die paddle size, this size needs to be modified in some cases to avoid solder bridging between the thermal pad and the perimeter pads. The thermal pad design on the board should be based on the exposed paddle area, excluding the ring area.

Figure 3-4. Thermal Pad Design



In order to effectively transfer heat from the top metal layer of the PCB to the inner or bottom layers, thermal vias need to be incorporated into the thermal pad design. The number of thermal vias will depend on the application, the power dissipation, and the electrical requirements. Although more thermal vias improve the package thermal performance, there is a point of diminishing returns as additional thermal vias may not significantly improve the performance. This is shown in Figure 3-5 where the effect of number of vias versus θja is plotted for a 7 mm, 48-lead package. A via diameter of 0.3 mm was used for this simulation. As the via pitch decreases more vias can be incorporated for the same thermal pad size but the incremental performance improvement goes down.

Figure 3-5. Effect of Number of Thermal Vias on the Package Thermal Performance



Based on this and similar thermal simulations, it is recommended that an array of thermal vias should be incorporated at a 1.0 to 1.2 mm pitch with a via diameter of 0.3 to 0.33 mm.

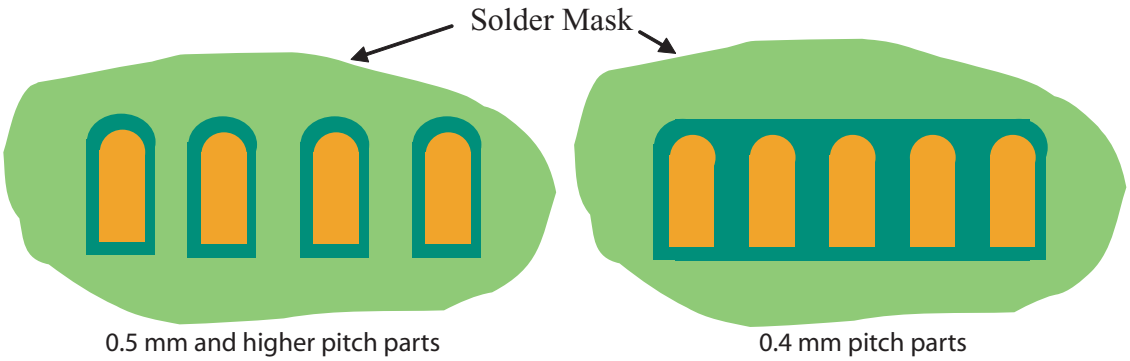
3.3 Solder Masking Considerations

The pads on the printed circuit board are either solder mask defined (SMD) or non solder mask defined (NSMD). Since the copper etching process has tighter control than the solder masking process, NSMD pads are preferred over SMD pads. Also, NSMD pads with the solder mask opening larger than the metal pad size also improves the reliability of the solder joints, as solder is allowed to wrap around the sides of the metal pads. Because of these reasons, the NSMD pad is recommended for perimeter lands.

The solder mask opening should be 120 to 150 microns larger than the pad size resulting in 60 to 75 micron clearance between the copper pad and the solder mask. This allows for solder mask registration tolerances, which are typically between 50 to 65 microns, depending upon the board fabricators' capabilities. Typically each pad on the PCB should have its own solder mask opening with a web of solder mask between the two adjacent pads. Since the web has to be at least 75 microns in width for the solder mask to stick to the PCB surface, each pad can have its own solder mask opening for a lead pitch of 0.5 mm or higher, based on the pad width. However, for 0.4 mm pitch parts with a PCB pad width of 0.25 mm, not enough space is available for

the solder mask web in between the pads. In such cases, it is recommended to use the “trench” type solder mask opening where a big opening is designed around all the pads on each side of the package with no solder mask in between the pads, as shown in Figure 3-6. It should also be noted that the inner edge of the solder mask should be rounded, especially for the corner leads to allow for enough solder mask web in the corner area.

Figure 3-6. Solder Mask Definition for Perimeter Lands



For the cases where the thermal land dimensions are close to the theoretical maximum discussed above, it is recommended that the thermal pad area should be solder mask defined in order to avoid any solder bridging between the thermal pad and the perimeter pads. The mask opening should be 100 microns smaller than the thermal land size on all four sides. This will guarantee a 25 micron solder mask overlap even for the worse case misregistration.

4. Board Mounting Guidelines

Because of the small lead surface area and the sole reliance on the printed solder paste on the PCB surface, care must be taken to form reliable solder joints for MLF packages. This is further complicated by the large thermal pad underneath the package and its proximity to the inner edges of the leads. Although the pad pattern design suggested above might help in eliminating some of the surface mounting problems, special considerations are needed in the stencil design and the paste printing for both the perimeter and the thermal pads. Since the surface mount process varies from company to company, careful process development is recommended. The following provides some guidelines for the stencil design based on Atmel’s experience in the surface mounting of the MLF packages.

4.1 Stencil Design for Perimeter Pads

The optimum and the reliable solder joints on the perimeter pads should have about 50 to 75 microns (2 to 3 mils) standoff height and a good side fillet on the outside. A joint with good standoff height but no or low fillet will have reduced life but may meet the application requirement. The first step in achieving good standoff is the solder paste stencil design for the perimeter pads. The stencil aperture opening should be designed so that maximum paste release is achieved. This is typically accomplished by considering the following two ratios:

- Area Ratio = Area of Aperture Opening/Aperture Wall Area, and
- Aspect Ratio = Aperture width/ Stencil Thickness

For rectangular aperture openings, as required for this package, these ratios are given as

- Area Ratio = LW/2T(L+W), and

- Aspect Ratio = W/T

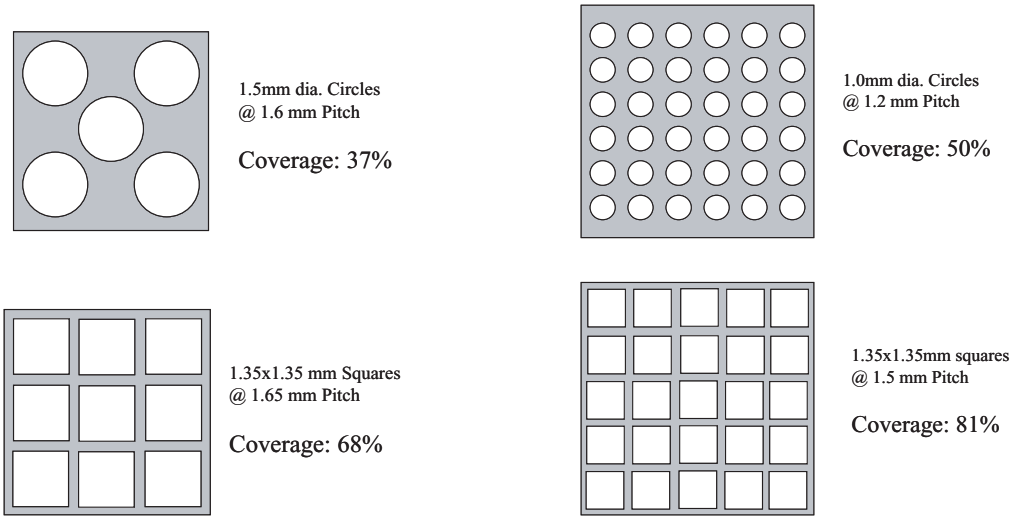
Where L and W are the aperture length and width, and T is stencil thickness. For optimum paste release the area and the aspect ratios should be greater than 0.66 and 1.5 respectively.

It is recommended that the stencil aperture should be 1:1 to the PCB pad sizes as both the area and the aspect ratio targets are easily achieved by this aperture. The opening can be reduced for a lead pullback option because of the reduction of the solderable area on the package. The stencil should be laser cut and electro polished. The polishing helps in smoothing the stencil walls which results in a better paste release. It is also recommended that the stencil aperture tolerances should be tightly controlled, especially for 0.4 and 0.5mm pitch devices, as these tolerances can effectively reduce the aperture size.

4.2 Stencil Design for Thermal Pad

In order to effectively remove the heat from the package and to enhance the electrical performance, the die paddle needs to be soldered to the PCB thermal pad, preferably with minimum voids. However, eliminating voids may not be possible because of the presence of thermal vias and the large size of the thermal pad for larger size packages. Also, out gassing occurs during reflow process which may cause defects (splatter, solder balling) if the solder paste coverage is too big. Therefore, it is recommended that smaller multiple openings in the stencil should be used instead of one big opening for printing the solder paste on the thermal pad region. This will typically result in 50 to 80% solder paste coverage. Shown in Figure 4-1 are some of the ways to achieve these levels of coverage.

Figure 4-1. Thermal Pad Stencil Designs for 7x7 and 10x10mm MLF Packages



4.3 Via Types and Solder Voiding

Voids within the solder joints under the exposed pad can have an adverse effect on high speed and RF applications as well as on the thermal performance. As the MLF package incorporates a large center pad, controlling solder voiding within this region can be difficult. Voids within this ground plane can increase the current path of the circuit. The maximum size for a void should be less than the via pitch within the plane. This recommendation would assure that any via would not be rendered ineffectual based on any void increasing the current path beyond the distance to the next available via.

With regards to the voids in the thermal pad region, it should be emphasized that the presence of these voids is not expected to result in degradation of the thermal and the electrical performance. This is shown in Figure 4-2 where no loss in thermal performance is predicted from the thermal simulation of the smaller multiple voids covering up to 50% of the thermal pad area. It should also be noted that the voids in the thermal pad region do not impact the reliability of the perimeter solder joints.

Although the percentage of voids may not be a big concern, large voids in the thermal pad area should be avoided. In order to control these voids, solder masking may be required for the thermal vias to prevent solder wicking inside the via during reflow, thus displacing the solder away from the interface between the package die paddle and the thermal pad on the PCB. There are different methods employed within the industry for this purpose, such as “via tenting” (from top or bottom side) using dry film solder mask, “via plugging” with liquid photo-imagible (LPI) solder mask from the bottom side, or “via encroaching”. These options are depicted in Figure 4-3. In case of via tenting, the solder mask diameter should be 100 microns larger than the via diameter.

Figure 4-2. Effect of Voids on Thermal Performance

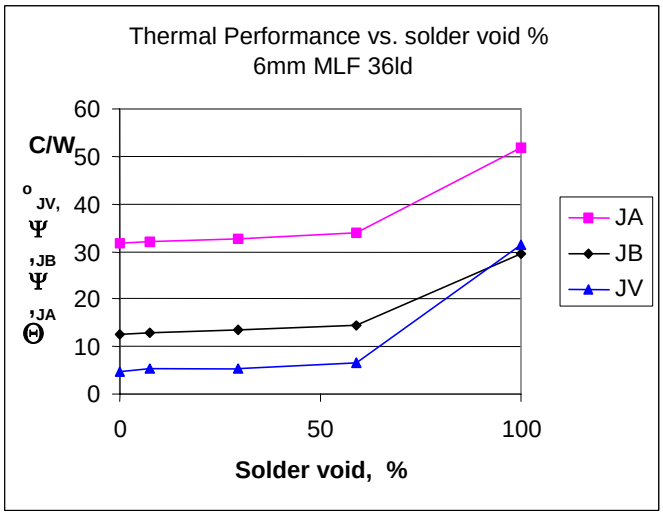


Figure 4-3. Solder Mask Options for Thermal Vias

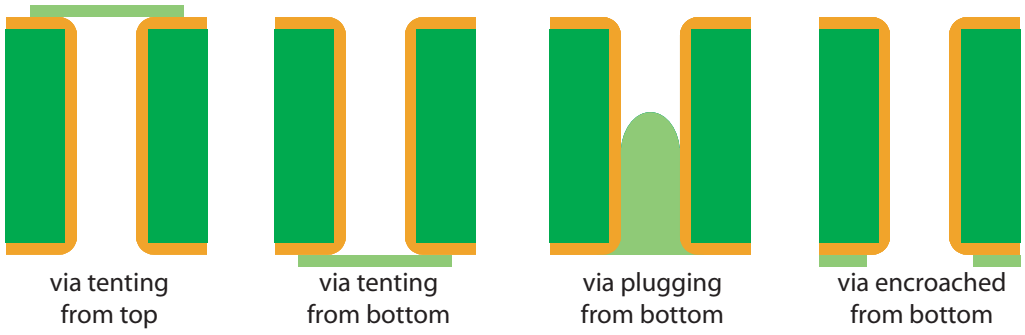
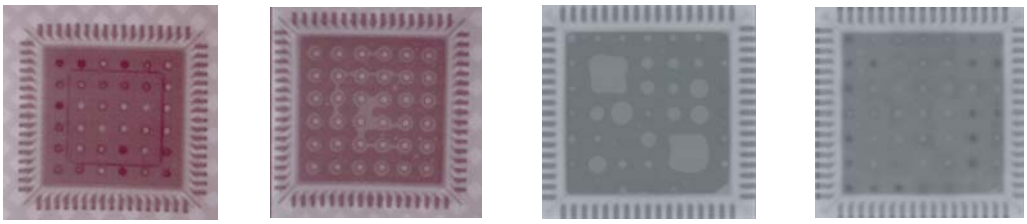


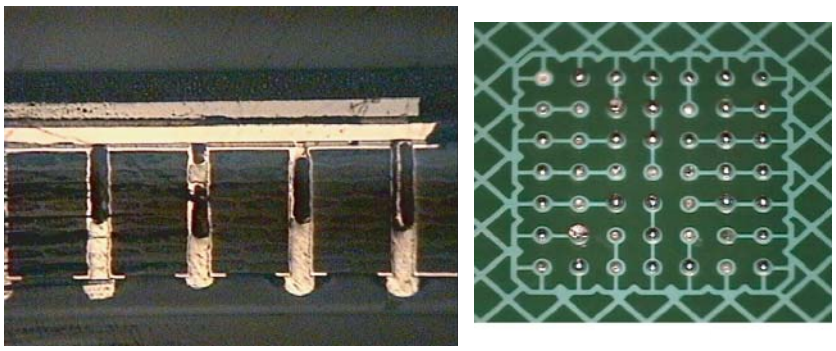
Figure 4-4. Voids in Thermal Pad Solder Joint



All of these options have pros and cons when mounting the MLF package on the board. While via tenting from the top side may result in smaller voids, the presence of the solder mask on the top side of the board may hinder proper paste printing. On the other hand, both via tenting from bottom or via plugging from bottom may result in larger voids due to out-gassing, covering more than two vias. Finally, encroached vias allow the solder to wick inside the vias and reduce the size of the voids. However, it also results in lower standoff of the package, which is controlled by the solder underneath the exposed pad. Figure 4-4 shows representative x-ray pictures of MLF packages mounted on the boards with the different via treatments.

Encroached via, depending on the board thickness and the amount of solder printed underneath the exposed pad, may also result in solder protruding from the other side of the board, as shown in Figure 4-5. Note that the vias are not completely filled with solder, suggesting that solder wets down the via walls until the ends are plugged. This protrusion is a function of the PCB thickness, the amount of paste coverage in the thermal pad region, and the surface finish of the PCB. Atmel's experience is that this protrusion can be avoided by using a lower volume of the solder paste and reflow peak temperature of less than 215°C. If solder protrusion cannot be avoided, the MLF components may have to be assembled on the top side (or final pass) assembly, as the protruded solder will impede acceptable solder paste printing on the other side of the PCB.

Figure 4-5. Solder Protrusion from the Bottom Side of PCB for Encroached Vias



4.4 Stencil Thickness and Solder Paste

A stencil thickness of 0.125 mm is recommended for 0.4 and 0.5 mm pitch parts and can be increased to 0.15-0.2 mm for the coarser pitch parts. A laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

Since not enough space is available underneath the part after reflow, it is recommended that the "No Clean", Type 3 paste be used for mounting MLF packages. Nitrogen purge is also recommended during the reflow.

4.5 Solder Joint Standoff Height and Fillet Formation

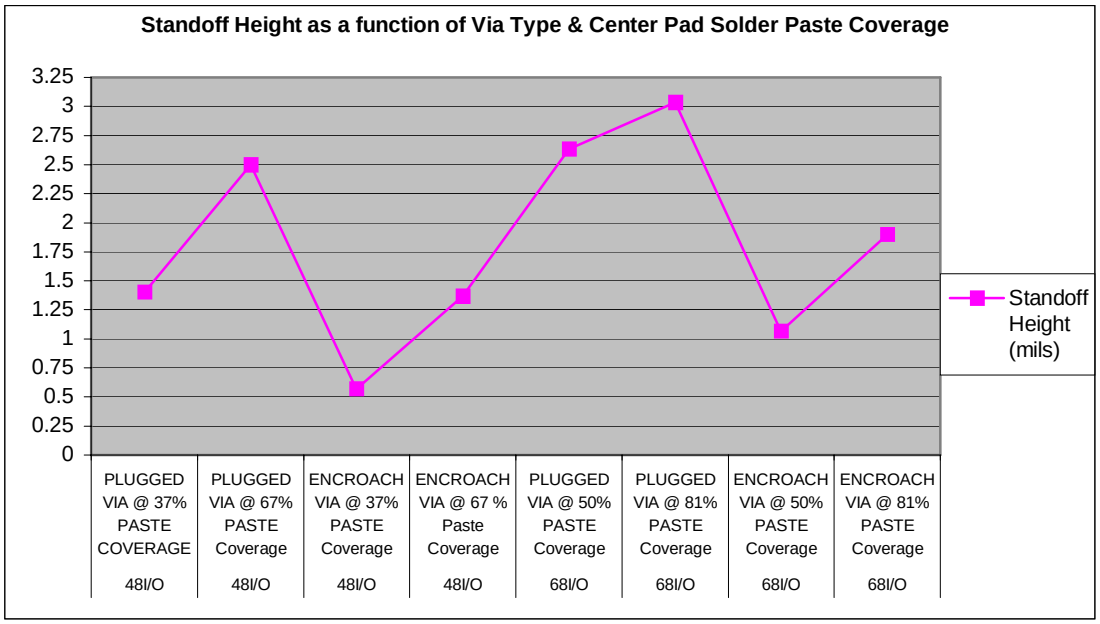
The solder joint standoff is a direct function of the amount of paste coverage on the thermal pad and the type of vias used for MLFs with the exposed pad at the bottom. Board mounting studies sponsored by Amkor® have clearly shown that the package standoff increases by increasing the paste coverage and by using the plugged vias in the thermal pad region. This is shown in Figure 4-6 below.

The standoff height varies by the amount of solder that wets or flows into the PTH via. The encroached via provides an easy path for solder to flow into the PTH and decreases the package standoff height while the plugged via impedes the flow of solder into the via due to the plugged via's closed barrel end. In addition, the number of vias and their finished hole size will also influence the standoff height for encroached via design. The standoff height is also affected by the type, the reactivity of the solder paste used during assembly, the PCB thickness, the surface finish, and the reflow profile.

To achieve 50 micron thick solder joints, which help in improving the board level reliability, it is recommended that that the solder paste coverage be at least 50% for the plugged vias and 75% for the encroached via types.

The peripheral solder joint fillets formation is also driven by multiple factors. It should be realized that only the bottom surface of the leads are plated with solder and not the ends. The bare Cu on the side of the leads may oxidize if the packages are stored in an uncontrolled environment. It is, however, possible that a solder fillet will be formed depending on the solder paste (flux) used and the level of oxidation.

Figure 4-6. Standoff Height as a Function of Via Type and Paste Coverage

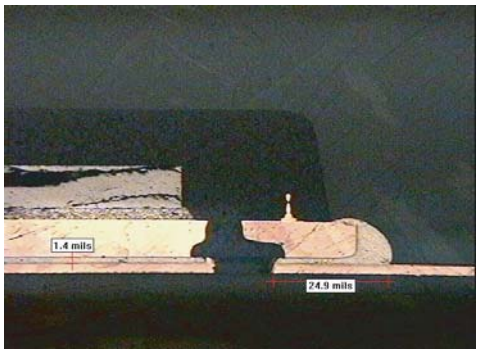


The fillet formation is also a function of the PCB land size, the printed solder volume, and the package standoff height. The land sizes listed in Figures 3-2 and 3-3 on page 3 will provide sufficient solder for the fillet information if the package standoff is not excessive. Since there is only limited solder available, higher standoff (controlled by the paste coverage on the thermal pad)

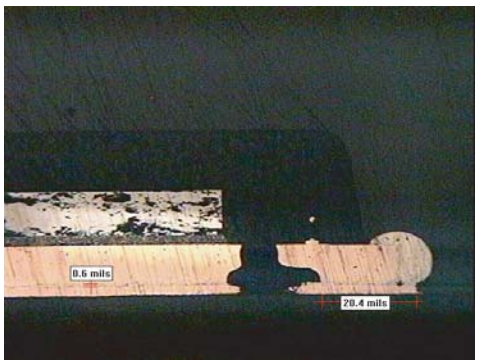
may not leave enough solder for fillet formation. Conversely, if the standoff is too low, large convex shape fillets may form. This is shown in Figure 4-7.

Since center pad coverage and via type were shown to have the greatest impact on the standoff height, the volume of solder necessary to create optimum fillet varies. The package standoff height and the PCB pads size will establish the required volume.

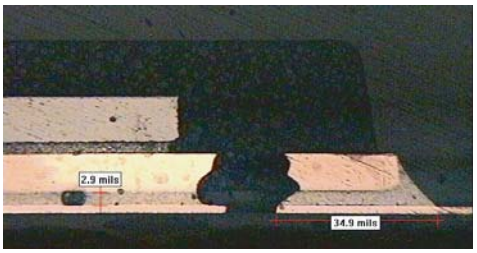
Figure 4-7. Solder Fillet Shape



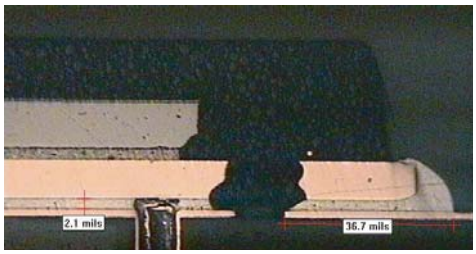
37% paste coverage, plugged via,
1.4 mil standoff



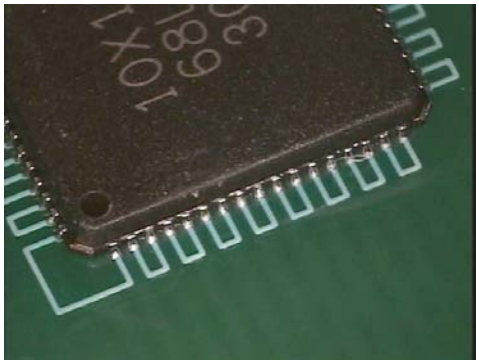
37% paste coverage, encroached via,
0.6 mil standoff



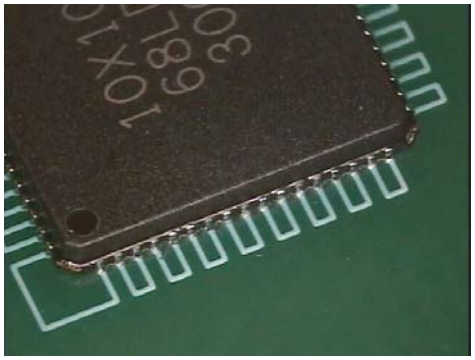
50% paste coverage, plugged via,
2.9 mil standoff



81% paste coverage, encroached via,
2.1 mil standoff



Large PCB pads, 81% paste coverage,
plugged vias



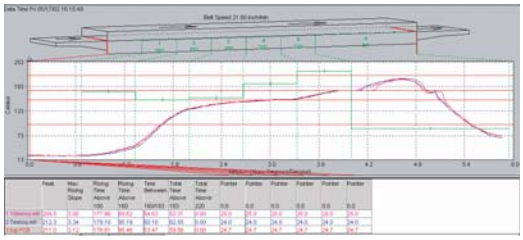
Small PCB pads, 81% paste coverage,
plugged vias

4.6 Reflow Profile

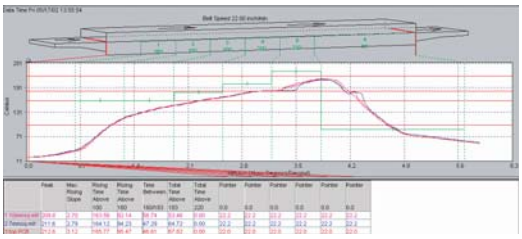
The reflow profile and the peak temperature have a strong influence on void formation. Amkor has conducted experiments with the different reflow profiles (ramp-to-peak vs. ramp-hold-ramp), the peak reflow temperatures, and the times above liquidus using Alpha Metal's UP78 solder paste. Some of the representative profiles are shown in Figure 4-8. Generally, it is found that the

voids in the thermal pad region for the plugged vias reduce as the peak reflow temperature is increased from 210°C to 215-220°C. For the encroached vias, it is found that the solder extrusion from the bottom side of the board reduces as the reflow temperature is reduced.

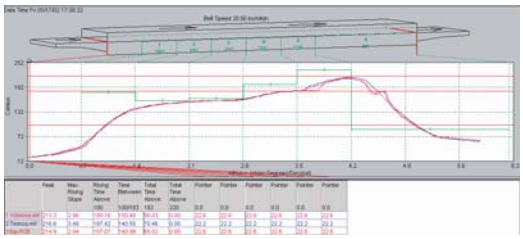
Figure 4-8. Various Reflow Profiles



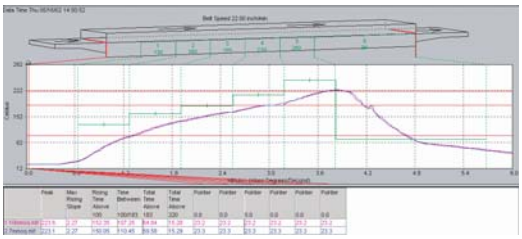
Ramp-Soak-Spike – 210°C peak



Ramp-Spike – 210°C peak



Ramp-Soak-Spike – 215°C peak



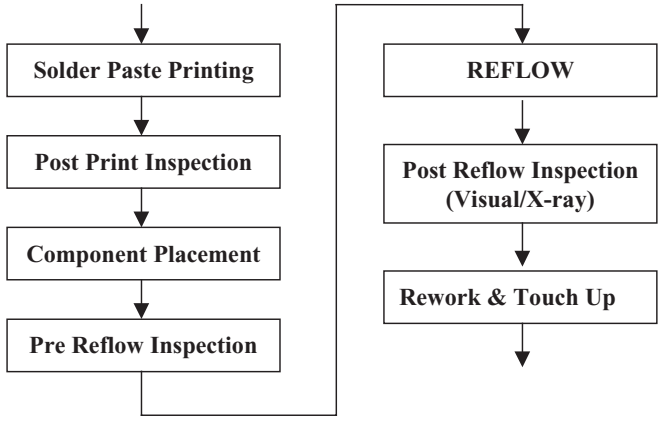
Ramp-Spike – 220°C peak

5. Assembly Process Flow

Figure 5-1 shows the typical process flow for mounting the surface mount packages to the printed circuit boards. The same process can be used for mounting the MLFs without any modifications. It is important to include the post print and the post reflow inspection, especially during the process development. The volume of paste printed should be measured either by the 2D or the 3D techniques. The paste volume should be around 80 to 90% of the stencil aperture volume to indicate a good paste release. After reflow, the mounted package should be inspected in the transmission x-ray for the presence of voids, solder balling, or other defects. Cross-sectioning may also be required to determine the fillet shape, size and the joint standoff height.

Typical reflow profiles for no-clean solder paste are shown in Figure 5-1. Since the actual reflow profile depends on the solder paste being used and the board density, Amkor does not recommend a specific profile. However, the temperature should not exceed the maximum temperature the package is qualified for according to the moisture sensitivity level. The time above the liquidus temperature should be around 60 seconds and the ramp rate during preheat should be 3°C/second or lower.

Figure 5-1. Typical PCB Mounting Process Flow



6. Rework Guidelines

Since solder joints are not fully exposed in the case of MLFs, any retouch is limited to the side fillet. For defects underneath the package, the whole package has to be removed. Rework of the MLF packages can be a challenge due to their small size. In most applications, the MLFs will be mounted on smaller, thinner, and denser PCBs that introduce further challenges due to the handling and the heating issues. Since reflow of the adjacent parts is not desirable during rework, the proximity of other components may further complicate this process. Because of the product dependent complexities, the following only provides a guideline and a starting point for the development of a successful rework process for these packages.

The rework process involves the following steps:

1. Component Removal
2. Site Redress
3. Solder Paste Application,
4. Component Placement, and
5. Component Attachment.

These steps are discussed in the following in more detail. Prior to any rework, it is strongly recommended that the PCB assembly be baked for at least 4 hours at 125°C to remove any residual moisture from the assembly.

6.1 Component Removal

The first step in removal of the component is the reflow of the solder joints attaching the component to the board. Ideally, the reflow profile for the part removal should be the same as the one used for the part attachment. However, the time above liquidus can be reduced as long as the reflow is complete.

In the removal process, it is recommended that the board should be heated from the bottom side using convective heaters and hot gas or air should be used on the top side of the component. Special nozzles should be used to direct the heating in the component area and the heating of adjacent components should be minimized. Excessive airflow should also be avoided since this may cause the CSP (chip-scale package) to skew. Air velocity of 15-20 liters per minute is a good starting point.

Once the joints have reflowed, the vacuum lift-off should be automatically engaged during the transition from the reflow to cooldown. Because of their small size the vacuum pressure should be kept below 15 inches of Hg. This will allow the component not to be lifted out if all joints have not been reflowed and avoid the pad liftoff.

6.2 Site Redress

After the component has been removed, the site needs to be cleaned properly. It is best to use a combination of a blade-style conductive tool and a desoldering braid. The width of the blade should be matched to the maximum width of the footprint and the blade temperature should be low enough not to cause any damage to the circuit board. Once the residual solder has been removed, the lands should be cleaned with a solvent. The solvent is usually specific to the type of paste used in the original assembly and the paste manufacturer's recommendations should be followed.

6.3 Solder Paste Printing

Because of their small size and the finer pitches, solder paste deposition for the MLFs requires extra care. However, a uniform and precise deposition can be achieved if a miniature stencil specific to the component is used. The stencil aperture should be aligned with the pads under 50 to 100X magnification. The stencil should then be lowered onto the PCB and the paste should be deposited with a small metal squeegee blade. Alternatively, the mini stencil can be used to print paste on the package side also. A 125 microns thick stencil with the aperture size and shape same as the package land should be used. Also, no-clean flux should be used, as small standoff of the MLFs does not leave much room for cleaning.

6.4 Component Placement

MLF packages are expected to have superior self-centering ability due to their small mass and the placement of this package should be similar to that of BGAs. As the leads are on the under-side of the package, the split-beam optical system should be used to align the component on the motherboard. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. Again, the alignment should be done at 50 to 100X magnification. The placement machine should have the capability of allowing fine adjustments in the X, Y, and the rotational axes.

6.5 Component Attachment

The reflow profile developed during original attachment or removal should be used to attach the new component. Since all reflow profile parameters have already been optimized, using the same profile will eliminate the need for thermocouple feedback and will reduce operator dependencies.

7. Disclaimer

These are only general guidelines Atmel received from its package vendor. Atmel does not make direct recommendation for board design nor does it take legal liability and responsibility for the information in this document. Please refer to the IPC website for more information.