

ML501 Getting Started Tutorial

For ML501 Evaluation Platforms

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/30/06	1.0	Initial Xilinx release.

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About This Guide

The *ML501 Getting Started Tutorial* provides step-by-step instructions for setting up and using the ML501 evaluation platform (the board). The ML501 board comes with a number of pre-installed demonstrations. This tutorial guides you through these demonstrations and provides instructions to run them on the ML501 evaluation platforms.

Additional Documentation

The following documents are also available for download at <http://www.xilinx.com/virtex5>.

- Virtex™-5 Family Overview
The features and product selection of the Virtex-5 family are outlined in this overview.
- Virtex-5 Data Sheet: DC and Switching Characteristics
This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.
- XtremeDSP™ Design Considerations
This guide describes the XtremeDSP slice and includes reference designs for using the DSP48E slice.
- Virtex-5 Configuration Guide
This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.
- Virtex-5 Packaging Specifications
This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at: <http://www.xilinx.com/support>.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
<i>Italic font</i>	References to other documents	See the <i>Virtex-5 Configuration Guide</i> for more information.
	Emphasis in text	The address (F) is asserted <i>after</i> clock event 2.
<u>Underlined Text</u>	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section “ Additional Documentation ” for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the <i>Virtex-5 Data Sheet</i>
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

ML501 Getting Started Tutorial

Overview

The ML501 evaluation platform (the board) comes with a number of pre-installed demonstration programs. This tutorial guides you through these demonstrations and provides instructions to run them on the ML501 evaluation platforms.

Some demonstrations interact with a computer or an external device. For these demonstrations, use a computer installed with:

- Xilinx ISE 8.2i (Service Pack 2)
- Xilinx Platform Studio 8.2i (Service Pack 1)
- ChipScope™ Pro 8.2i (Service Pack 2)

The following additional equipment is also recommended:

- DVI or VGA monitor
- Computer speaker with audio cable
- Ethernet port and an RJ-45 Ethernet cable
- USB keyboard (without a built-in USB hub)
- Null modem serial cable
- CompactFlash (CF) reader/writer for the computer
- Xilinx download cable (Parallel Cable III/IV or Platform Cable USB) with JTAG flying wires adapter

For current information about the ML501 evaluation platform, visit the ML501 Web page: www.xilinx.com/ml501.

Board Setup

1. Position the ML501 board so the Xilinx logo is in the upper left corner.
2. Make sure the power switch located in the upper right corner is in the OFF position.
3. Locate the CF card slot (on the back side of the ML501 board), and carefully insert the System ACE™ CF card with its front label facing away from the board. [Figure 1](#) shows the back side of the board with the CF card properly inserted.

Note: The CF card provided with your board might differ.

Caution! Be careful when inserting or removing the CF card from the slot. Do *not* force it.

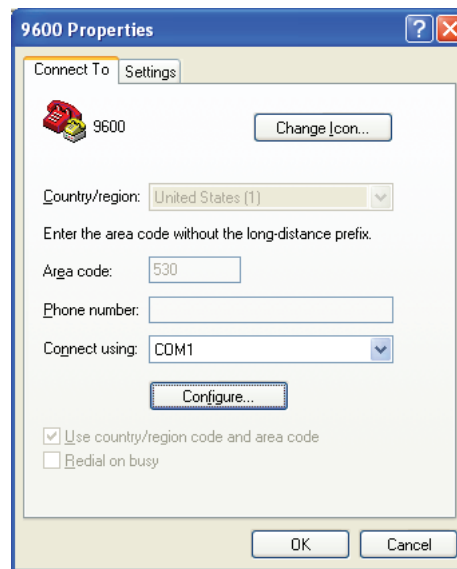


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Figure 1: ML501 Evaluation Platform with CF Card

4. Connect the AC power cord to the power supply brick. Plug the power supply adapter cable into the ML501 board. Plug in the power supply to AC power.
5. Set the configuration address and mode DIP switch (the 8-position DIP switch located above the other 8-position DIP switch) to 00010101.

6. Connect a null modem serial cable between your computer and the ML501 board, and open a serial terminal program:
 - ◆ Select **Start** → **Programs** → **Accessories** → **Communications** → **HyperTerminal**
 - ◆ In the Connection Description window, type **9600** in the Name box, then click **OK**
 - ◆ In the Connect To window, click **Cancel**
 - ◆ In the 9600-HyperTerminal window, select **File** → **Properties**
 - Select the **Connect To** tab
 - Select **COM1** in the Connect using box (see [Figure 2](#))
 - Click **Configure...**



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Figure 2: HyperTerminal Setup and Properties

Use the pull-down menu to set the COM1 properties (Figure 3) to the following:

- ◆ Bits per second = 9600
- ◆ Data bits = 8
- ◆ Parity = None
- ◆ Stop bits = 1
- ◆ Flow control = None
- ◆ Click **OK** → **OK** to accept settings

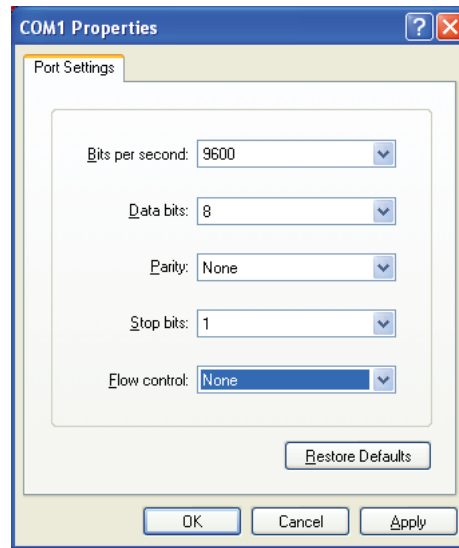
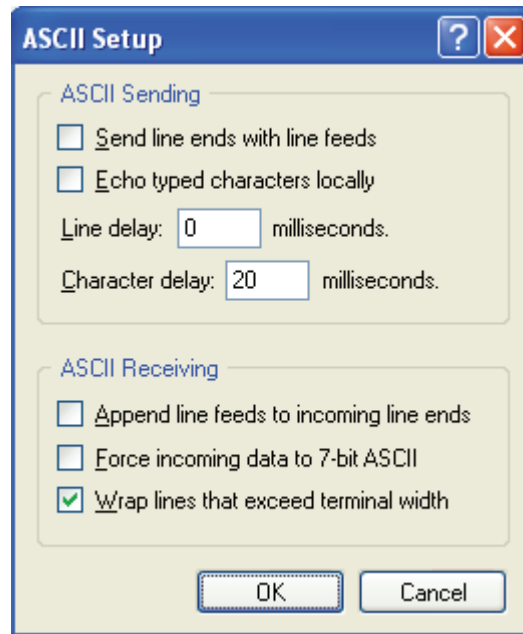


Figure 3: COM1 Properties Setup

7. Select **File** → **Properties**.
8. Select the Settings tab and click on **ASCII Setup** (Figure 4, page 11).



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Figure 4: ASCII Setup

9. For Character delay, enter 20.
10. Click **OK** → **OK** to accept the settings.
11. Connect the DVI monitor or the VGA monitor with DVI-to-VGA adapter to the board, if available.
12. Turn on the ML501 board's main power switch and press the SYSACE RESET button. After the FPGA has been programmed, the LEDs in the lower left corner should be:
 - ◆ Bus Error 1 and 2 = off
 - ◆ FPGA INIT = green
 - ◆ FPGA DONE = green
 - ◆ System ACE "Err" = off
 - ◆ System ACE "Stat" = green

Note: When the CF card is ejected or not installed, the System ACE "Err" LED blinks.

13. Extract the associated training lab files to your local computer.

Unzip the training lab files to a working directory, name the directory, and make note of the directory's name. This directory with the extracted files is referred to as <LAB_DIR> in this tutorial.

ML501 Demonstrations in System ACE CF

Bootloader Demonstrations

To select configuration using System ACE CF, set the configuration address and mode DIP switch (8-position DIP switch) to 00010101. To return to the ML501 Bootloader at anytime, press the SYSACE RESET button.

Location

System ACE configuration address 0.

Description

The ML501 Bootloader demonstration displays a menu of demonstration designs that can be loaded by using the System ACE controller's reconfiguration feature. The menu is displayed on the serial terminal, LCD, and VGA.

To choose a demonstration, use the North-East-South-West-Center-oriented pushbuttons on the board ([Figure 5](#)), then press the center button to start the demonstration. Alternatively, you can select a demonstration by entering its number into the serial terminal.

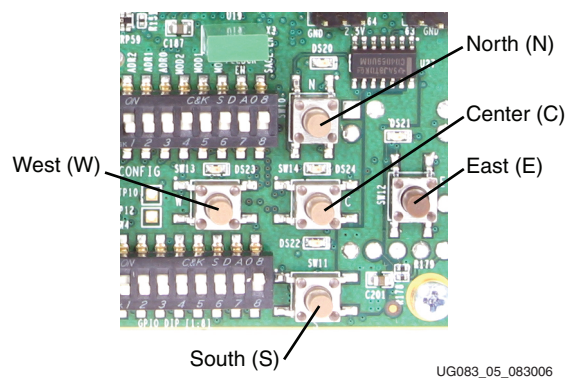


Figure 5: User Pushbuttons

The demonstrations are:

- “Virtex-5 Slide Show,” page 13
- “Web Server (Using Soft Ethernet MAC),” page 14
- “Simon Game,” page 16
- “ChipScope Pro Tools,” page 17
- “USB,” page 19
- “My Own ACE File,” page 20
- “Ring Tone Player,” page 21

Virtex-5 Slide Show

Location

System ACE configuration address 1.

From the Bootloader menu, select option **1** to start the Virtex™-5 Slide Show demonstration.

Description

This demonstration displays a sequence of picture files stored on the CF card accompanied by audio playback of a music file stored on the CF card. Pressing the East/West (E/W) buttons on the board manually switches to the previous/next slide. The North/South (N/S) buttons on the board change the volume. The center (C) button toggles between pausing and continuing the slide show.

Note: This demonstration requires a DVI monitor or a VGA monitor with a DVI-to-VGA adapter connected to the DVI port. It also requires a headphone or external speaker connected to the audio jacks.

In this program, the processor reads the CF file system through the System ACE MPU port and loads the audio/video data into DDR2 SDRAM. The processor then controls the flow of data to the VGA controller and audio controller connected to the internal CoreConnect bus.

Setup

To change or customize the slide show, follow these instructions:

1. Place the picture files in the root directory.
2. Name the picture files `image<XX>.bmp` where <XX> is a numerical sequence starting from 01 and counting up.

The program reads the picture files through the System ACE MPU interface starting from `image01.bmp` then counts upward. A maximum of 16 images can be read. The BMP files must be sized as 640 x 480 pixels with 24-bit color.

3. Give the sound file the name `sound.wav` and encode it as a 44.1 KHz, 16-bit stereo wave file (CD format). The sound file cannot be greater than 32 MB in size.

Note: When adding additional images or larger sound files, it might be necessary to use a higher capacity System ACE CF card than the one shipped with the ML501 board.

Try to add your own slides and music. For example, in Microsoft PowerPoint, you can export a presentation to HTML for a 640 x 480 screen. You can then convert the JPG or GIF slides to BMP format using Microsoft Photo Editor that is installed on many computers. Rename the BMP files to `image<XX>.bmp` and copy to the System ACE CF card. Now you can run your own customized slide show. For audio, try to extract a song from a CD into a WAV file. Copy the WAV file into the System ACE CF card and name it `sound.wav`.

Web Server (Using Soft Ethernet MAC)

Location

System ACE configuration address 2.

From the Bootloader menu, select option 2 to start the Web Server demonstration.

Description

In this demonstration, an Ethernet-controlled GPIO interface application uses the ML501 board as a Web server. A remote host, such as a computer running a Web browser, can communicate with the ML501 board using the Ethernet to read the value of the ML501 board's DIP switches or to set the LEDs on the board. Refreshing or reloading the remote computer's Web browser causes the background color to change and the current DIP switch values to be re-read. By default, the IP address of the ML501 board is 1.2.3.4, but it can be changed by recompiling the software.

Setup

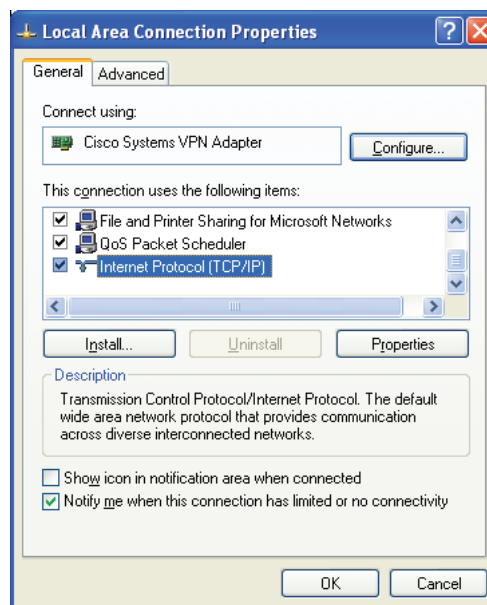
1. Connect an Ethernet cable (straight or crossover) from your host computer to the ML501 board.

Note: The Ethernet PHY chip on the ML501 board has an auto-crossover feature.

2. Configure the remote computer host's IP address to 1.2.3.9 (Subnet mask can be 255.0.0.0).

Note: Record the previous network settings so they will be easier to restore after the lab. The screen shots and icon names might be slightly different depending on your computer's operating system version.

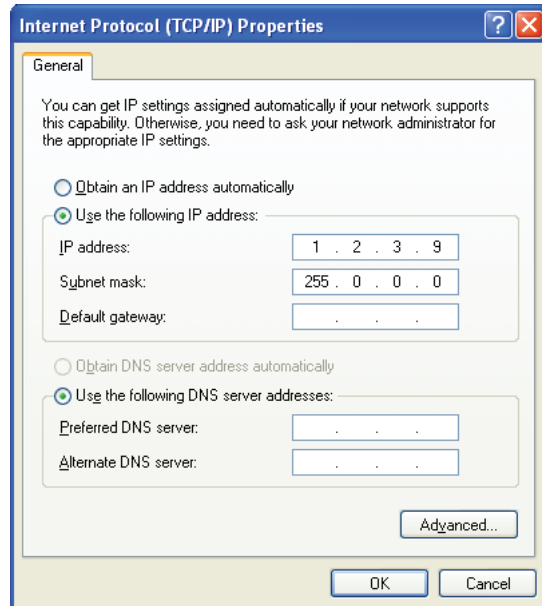
- ◆ Right-click **My Network Places** on your computer, and select **Properties**
- ◆ Right-click **Local Area Connection**, and select **Properties**
- ◆ Select **Internet Protocol (TCP/IP)**, and click **Properties** ([Figure 6](#))



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Figure 6: Local Area Connection Properties Setup

- ◆ Select **Use the following IP address:** (see [Figure 7](#))
- ◆ Enter this information: IP address = **1.2.3.9** and Subnet mask = **255.0.0.0**
- ◆ Click **OK** → **OK** to accept settings



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Figure 7: IP Settings

3. Make sure the connection is running at 10 or 100 Mb/s and the ML501 board's link lights are on (the lights are located in the upper left corner of the board). The link LEDs labeled 10, 100, and 1000 indicate the link is established at that speed.
 - ◆ You might need to force your computer to link in 10 or 100 Mb/s (duplex) mode. If so, then:
Right-click **Local Area Connection** → **Properties** → **Configure** → **Advanced tab** → **Speed**
4. On the remote computer host, open a Web browser connection to **http://1.2.3.4:8080**, and follow the instructions on the loaded Web page.
 - ◆ You might need to turn off your browser's proxy (use direct Internet connection mode) especially if you have multiple networking devices on your computer.
 - ◆ On the remote computer host, you can ping **1.2.3.4** to confirm that the network connection is alive.
5. Restore your computer's network settings when finished.

Simon Game

Location

System ACE configuration address 3.

From the Bootloader menu, select option 3 to start the Simon game demonstration.

Description

This demonstration displays the Simon game both through the DVI port and the button LEDs. Players input the correct sequence with the North-East-South-West-Center pushbuttons. Game sounds are produced on the piezo transducer. Messages are displayed on the character LCD and on the video screen.

Note: Note: This demonstration requires a DVI monitor or a VGA monitor with DVI-to-VGA adapter connected to the DVI port.

Instructions

At the beginning of the game, all the LEDs blink rapidly.

1. Press any button to start the game.
2. In each round, the LEDs blink and video graphics move in a given sequence. The player must press the buttons to repeat this displayed sequence.
3. Correctly repeating the sequence gives the player one point, and a new round is started. Each sequence becomes increasingly complex.
4. If a mistake is made, the score resets to 0 on the screen, the high score is updated, and all the LEDs blink rapidly to signify a new game.

ChipScope Pro Tools

Location


System ACE configuration address 4.

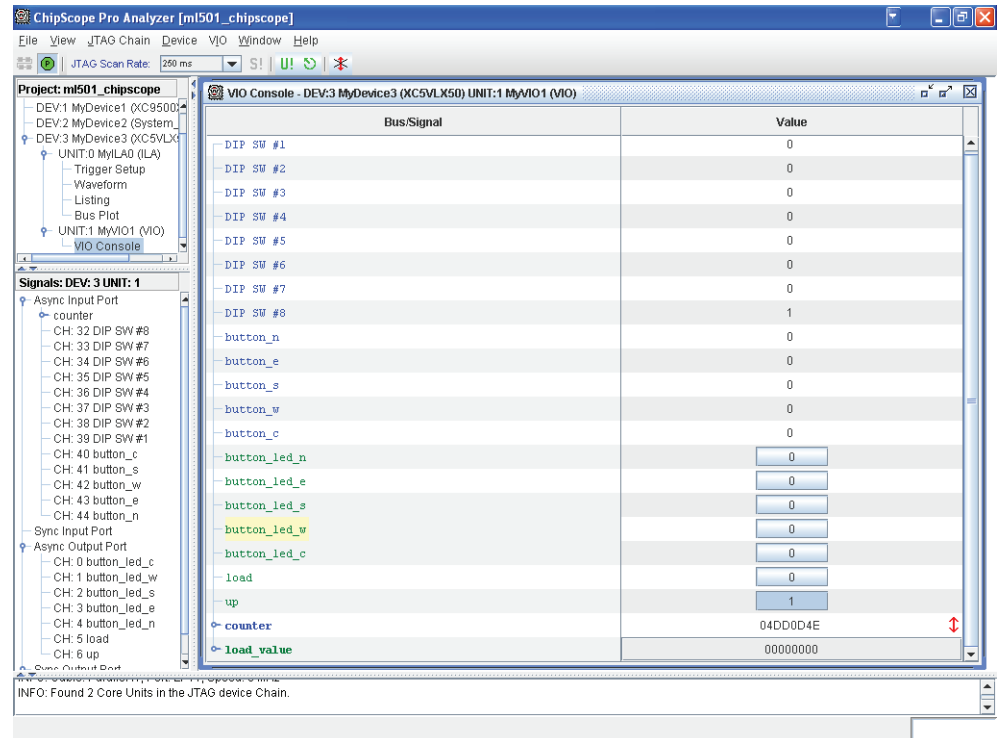
From the Bootloader menu, select option 4 to start the ChipScope Pro tools demonstration.

Description

This demonstration contains a loadable 32-bit binary counter that can be read and controlled using the ChipScope Pro Virtual I/O (VIO) feature. The LEDs show the upper bits of the counter. The inputs and outputs of the counter are also shown in the ChipScope Pro logic analyzer mode.


Setup

1. Connect the Xilinx download cable from the computer to the ML501 board.
2. Open the ChipScope Pro Analyzer.
3. Open the `ML501_chipscope_demo.cpj` file in `<LAB_DIR>` using **File** → **Open Project**.
4. Establish a JTAG connection with the ChipScope Pro ILA core running on the ML501 board. Click the left-most icon in the ChipScope Pro Analyzer icon bar: 
5. Look at the Virtual I/O (VIO) console ([Figure 8, page 18](#)). In the top-left window labeled **Project: ml501_chipscope**, scroll to the bottom and double-click on VIO console. You should see `32_bit_counter_count_val` changing as the 32-bit counter runs at 100 MHz. Click the **load** button (box to the right of the signal name) to force the counter to `0x00000000` where it resumes counting. Clicking the buttons associated with `button_led_*` turns on/off the corresponding LED on the board. Changing the DIP switches or pushing the directional buttons on the board also updates the status values in the VIO console.



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Figure 8: ChipScope Pro Analyzer

6. Look at the waveform window. Select **Window** → **Waveform - DEV:3 My...(ILA)**
7. Click the trigger immediate (T!) button. **T!**
8. Use the magnifying glass icon  to zoom in to see the individual 32-bit counter values.

USB

Location

System ACE configuration address 5.

From the Bootloader menu, select option 5 to start the USB demonstration.

Description

This demonstration uses the processor and the USB controller chip on the ML501 board to communicate with a USB keyboard.

The program functions by first reading the file `demo.bin` from the CompactFlash card. This file contains the software for the internal microprocessor inside the USB controller (Cypress CY7C76300). The FPGA's processor reads this file and writes the data to the memory inside the USB controller through its HPI port. The USB controller's internal processor then starts and can begin implementing low-level USB commands to communicate with the USB keyboard. Data from the USB keyboard is transferred to the FPGA's processor using mailbox registers over the HPI port.

Setup

Connect a standard USB keyboard to the ML501 board. Keys typed on the USB keyboard are then displayed on the character LCD and serial port.

Note: This demonstration requires a USB keyboard without a built-in hub.

My Own ACE File

Location

System ACE configuration address 6.

From the Bootloader menu, select option **6** to start the demonstration of the *My own ACE file* program.

Description

This program is a placeholder design to be replaced by a user design.

Setup

Take a bitstream and make your own ACE file:

1. Open a DOS command shell. Click **Start Menu** → **Run**, then enter **cmd** as the program to run, and click **OK**.
2. Change directory to your lab directory. Type **cd <LAB_DIR>**.
In this directory, there is a bitstream called `button_led_test_hw.bit`. This program tests the GPIO DIP switches and pushbuttons.
3. Convert this bitstream to an ACE file. On one line, type:

```
xmd -tcl ./genace.tcl -jprog -hw button_led_test_hw.bit -board ml501 -target mdm -ace my_button_led_test_hw.ace
```


This creates the `my_button_led_test_hw.ace` file.
4. Carefully remove the System ACE CF card from the ML501 board (preferably with the power off). Open the CF card on your computer. This requires either a PC card adapter or a USB CompactFlash reader (not included with ML501 board, but available at computer stores).
5. Copy `my_button_led_test_hw.ace` to the CF card into the **ML50X/cfg6** directory.
6. In the **ML50X/cfg6** directory on the CF card, rename `system_my_ace.ace` to `system_my_ace.bak`. This ensures that there is only one ACE file in this directory.
7. Eject the CF card from your computer (right-click on the CF card in Windows Explorer and click **Eject**). This shuts down the CF card to prevent data corruption. Carefully reinsert the CF card into the ML501 board (preferably with the power off).
8. Turn the power back on, if necessary, and press the SYSACE RESET button to restart the Bootloader. Select Option 6 to start the *My own ACE file* program. In this design, flipping a GPIO DIP switch or pressing a GPIO button will light a corresponding LED.

Ring Tone Player

Location

System ACE configuration address 7.

From the Bootloader menu, select option 7 to start the demonstration of the *Ring Tone Player* program.

Description

This program inputs a Ringing Tones Text Transfer Language (RTTTL) ring tone and creates the melody using the piezo transducer. Through a serial terminal program, users can play ring tones from a CF card or type in their ring tones.

Setup

1. The start screen ask you to insert the CF card, which contains the ring tones in the **ringtone** folder. When the CF is inserted, press any key.
2. A program menu appears with eight options. Entering 1, 2, 3, 4, 5, or 6 plays ring tones stored on the CF card.

If you have the RTTTL code of a ring tone, you have two options to play it:

- ◆ Replace the User.txt file on the CF card with the RTTTL code (Option 7)
- ◆ With a serial terminal program, paste or type in the RTTTL code (Option 8)

```

9600 - HyperTerminal
File Edit View Call Transfer Help
[Icons]
3. Simon Game
4. Chipscope Pro Demo
5. USB Demo
6. My own ACE file
7. Ring Tone Player
Rebooting to System ACE Configuration Address 7...

This program attempts to access the CF card's file system
Please insert a CF card with folder 'ringtones', which contains RTTTL ringtone f
iles:
a:\ringtone\5thSym.txt
a:\ringtone\OdeToJoy.txt
a:\ringtone\MozartE.txt
a:\ringtone\MozartR.txt
a:\ringtone\BachAir.txt
a:\ringtone\BachMin.txt
a:\ringtone\User.txt

Press any key to continue after CF is inserted.

***** Pick a Ringtone *****

1. Beethoven - 5th Symphony
2. Beethoven - Ode to Joy
3. Mozart - Eine Kleine Nachtmusik
4. Mozart - Rondo Alla Turca
5. Bach - Air on the G String
6. Bach - Minuet
7. User - From file 'User.txt'
8. User - Type in your ringtone
-
Connected 0:40:30 Auto detect 9600 8-N-1 SCROLL CAPS NUM Capture Print echo

```

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Figure 9: RTTTL Setup

RTTTL Specification

The RTTTL specification denotes the ring tone with a string containing three fields separated by a colon.

`<Name Field>:<Options Field>:<Notes Field>`

The following is an example of an RTTTL ring tone using the fields and parameters defined in [Table 1](#):

Beethoven:d=4,o=6,b=100:16g5,16g5,16g5,d5,16f5,16f5,16f5,d5,16g5,16g5,16g5,16d5,16g5,16g5,16g5,16g5,16d,16d,16d,c,16g5,16g5,16g5,16d5,16g5,16g5,16g5,16f,16f,16f,d.

Table 1: RTTTL Ring Tone Fields

Field	Parameter	Description
Name		The <i>Name</i> field specifies the name of the ring tone.
Options		The <i>Options</i> field uses three parameters to specify the duration, octave, and tempo of each note.
	d = {1,2,4,8,16,32,64}	Parameter d specifies the duration of each note as follows: <ul style="list-style-type: none"> • 1 is a whole note • 2 is a half note • 4 is a quarter note, and so forth If the duration is not specified, the default is d = 4.
	o = {4,5,6,7}	Parameter o specifies the octave of a note. Note <i>a</i> for each octave is as follows: <ul style="list-style-type: none"> • Octave 4 is 440 Hz • Octave 5 is 880 Hz • Octave 6 is 1760 Hz • Octave 7 is 3520 Hz If the octave is not specified, the default is o=6.
	b = {0,1,2,3...}	Parameter b specifies the beats per minute (tempo). If the tempo is not specified, the default is b=63.
Notes		The <i>Notes</i> field uses the letter of the note plus three optional parameters to define each note using the following format: [duration] <i>note</i> [scale] [extend duration]
	note = {a,b,c,d,e,f,g,p}	The note parameter defines a note on the musical scale, except the letter p which represents a rest.
		The duration and scale parameters take on the range specified in the Options field. If unspecified, these parameters take on the default value of the Options field.
	.	The extend duration parameter (a dot) defines a dotted note and lengthens the duration by 50 percent.

ML501 Demonstrations in Linear Flash

Linear Flash LCD Demonstration

Description

This demonstration shows the FPGA being configured by an external linear flash device and a CPLD. This method of download is used in some embedded processor systems where it is necessary to keep software and bitstream data in one non-volatile device.

Setup

1. To load a pre-loaded bitstream, change to the corresponding address configuration / mode dip switches listed below.
Configuration 0: 00001001
Configuration 1: 00101001
Configuration 2: 01001001
Configuration 3: 01101001
2. Press the **Prog** button.
3. After the bitstream has loaded, the character LCD should say "Design #x Loaded using Flash," where x is the bitstream number.

My Own Linear Flash Image Demonstration

Description

This exercise shows you how to store your own design into linear flash and how to program it onto the FPGA. This exercise overwrites the contents of linear flash.

To program your own bit file into linear flash:

1. Open a DOS command shell. Click **Start Menu** → **Run**, then enter **cmd** as the program to run, and click **OK**.
2. Change directory to your lab directory. Type **cd <LAB_DIR>**.
3. Copy your bit file into this folder.
`Copy <file_name>.bit .`
4. Create a BIN file, which will be used to program the linear flash device.
`promgen -w -p bin -o <file_name>.bin -u 0 <file_name>.bit`
5. Program the linear flash device with your bin file.

To store at a specific configuration, look up the specific configuration below:

```
configuration 0: type  jtagflasher -b 10 0          <file_name>.bin
configuration 1: type  jtagflasher -b 10 0x800000  <file_name>.bin
configuration 2: type  jtagflasher -b 10 0x1000000 <file_name>.bin
configuration 3: type  jtagflasher -b 10 0x1800000 <file_name>.bin
```

6. Change the configuration address /mode to your configuration to load your bit file.
configuration 0 : DIP switch = 00001001
configuration 1 : DIP switch = 00101001
configuration 2 : DIP switch = 01001001
configuration 3 : DIP switch = 01101001
7. Press **prog** to program the FPGA. Your design should now be running.

ML501 Demonstrations in Platform Flash

The Platform Flash PROM contains advanced features, such as revision control, and is a convenient and easy-to-use method of configuring FPGAs.

The Platform Flash on the ML501 board can hold multiple bitstreams:

- [“Platform Flash LCD Demonstration”](#)
- [“Platform Flash XROM Demonstration”](#)
- [“My Own Platform Flash Image Demonstration”](#)

To select configuration using Platform Flash, set the configuration address and mode DIP switch (8-position DIP switch) to 00011001.

Platform Flash LCD Demonstration

Location

Platform Flash configuration address 0.

Description

This demonstration displays to the character LCD the message “Put Your Design Here”.

Setup

1. Set the configuration address DIP switches to the binary value 00011001.
2. Press the **Prog** button to see the message “Put Your Design Here” displayed on the character LCD.

Platform Flash XROM Demonstration

Location

Platform Flash configuration address 1.

Description

The XROM program presents a menu over the serial port offering various diagnostic tests of the ML501 board features.

Setup

1. Set the configuration address DIP switches to the binary value 00111001.
2. Press the **Prog** button to run this demonstration.
3. Select from the menu presented on the serial terminal to run various diagnostic tests.

My Own Platform Flash Image Demonstration

Description

This exercise shows you how to store your own design into platform flash and how to program it onto the FPGA. This exercise overwrites the contents of platform flash.

To program your own BIT file into linear flash:

1. Change the Configuration Address / Mode DIP switches to 00011001.
2. Open a DOS command shell. Click **Start Menu** → **Run**, then enter **cmd** as the program to run, and click **OK**.
3. Change directory to your lab directory. Type **cd <LAB_DIR>**.
4. Copy your bit file into this folder.
Copy <file_name>.bit .
5. Format the BIT file to an MCS file. Type in the command prompt:
promgen -w -p mcs -o <file_name>.mcs -s 16384 -u 0 <file_name>.bit
6. Now you need to change the batch file to load your design. Click **Start Menu** → **My Computer** . Navigate to <LAB_DIR>.
7. Right-click the ml501_plat_flash file and select **Edit**.
8. In the file, replace the line:

```
setAttribute -position 1 -attr configFileName -value "<LAB_DIR>\production_ml501.mcs"  
with
```

```
setAttribute -position 1 -attr configFileName -value "<LAB_DIR>\<file_name>.mcs"
```

9. Program the Platform Flash. Go back to the command prompt and type:
Program_ML501_PlatFlash.bat
10. Press **Prog** and your design should now be running.

Note: ISE iMPACT also offers a method for programming the Platform Flash.

ML501 Demonstrations in SPI Flash

SPI Flash memory can be used for FPGA configuration or to hold user data. The SPI Flash on the ML501 board contains the following bitstreams:

- “SPI Flash Hello Demonstration”
- “My Own SPI Flash Image Demonstration”

To select configuration using SPI Flash, set the configuration address and mode DIP switch (8-position DIP switch) to 00000101.

SPI Flash Hello Demonstration

Location

SPI Flash configuration address 0.

Description

This program displays to the character LCD the “Design Loaded Using SPI Mem” message.

Setup

Press the **Prog** button to see the “Design Loaded Using SPI Mem” message displayed on the character LCD.

My Own SPI Flash Image Demonstration

SPI is a flash device that can store your configuration file and program it to the FPGA. This demonstration shows you how to store your own design into the SPI Flash and how to program it onto the FPGA. This exercise overwrites the contents of the SPI Flash.

1. Disconnect the cable attached to header J1 (the header on the left side of the board) from the Xilinx download cable.
2. Connect JTAG flying wires from the Xilinx download cable to the header J2 (7-pin header to the right of the FPGA).
There is a label northwest of the FPGA labeled **J2 SPI Prog** that shows you how to connect the wires from the Xilinx download cable to the header pins.
3. Set the configuration address DIP switches to 00010101
4. Remove the inserted ML501 CF card if present, and press the **Prog** button to erase the FPGA.
5. Open a DOS command shell. Click **Start Menu** → **Run**, then enter **cmd** as the program to run, and click **OK**.
6. Change directory to your lab directory. Type **cd <LAB_DIR>**.
7. Copy your BIT file into this folder.
Copy <file_name>.bit .

8. Format the BIT file to an MCS file.

```
promgen -spi -p mcs -o <file>.mcs -s 16384 -u 0 <file>.bit
```
9. Launch iMPACT and double-click **Direct SPI Configuration** in the iMPACT Modes window to program the SPI Flash device.
10. Right-click the Direct SPI Configuration tab and select **Add SPI Device...**
11. Navigate to `<file_name>.mcs` created above and click **Open**.
12. In the Select Device Part Name drop-down dialog box, select M25P16 and click **OK**.
13. The Direct SPI Configuration tabbed window displays a diagram of a single SPI PROM. Right-click on the SPI PROM and select **Program**.
14. Click **OK** to program the SPI Flash device.
15. On the board, change the configuration address / mode DIP switches to 00000101.
16. Press the **Prog** button. The design takes about 6 seconds to finish loading and begin to run.

