Features

- ARM7TDMI® ARM® Thumb® Processor Core
  - In-Circuit Emulator, 40 MHz operation
- 16-bit Fixed-point OakDSPCore®
  - Up to 60 MHz operations
  - 104K bytes of Integrated Fast RAM, Codec Interface
- Ethernet Bridge
  - Dual Ethernet 10/100 Mbps MAC Interface
  - 32-Kbyte Frame Buffer
- 1 K-Byte Boot ROM, Embedding a Boot Program
  - Enable Application Download from DataFlash®
- External Bus Interface
  - On-chip 32-bit SDRAM Controller
  - 4 Chip Select Static Memory Controller
- Multi-level Priority, Individually Maskable, Vectored Interrupt Controller
- Three 16-bit Timer/Counters
- Two UARTs with Modem Control Lines
- Serial Peripheral Interface (SPI)
- Two PIO Controllers, Managing up to 48 General-purpose I/O Pins
- Available in a 208-lead PQFP Package
- Power Supplies
  - VDDIO 3.3V nominal
  - VDDCORE and VDDOSC 1.8V nominal
- 0°C to + 70°C Operating Temperature Range

AT75C ARM®-based Microcontrollers

AT75C221 Electrical and Mechanical Characteristics

1. Description

Atmel's AT75C221 is a member of a series of highly integrated microcontrollers based on the 32-bit ARM RISC processor. It features a 16-bit fixed-point OakDSPCore® and an Ethernet bridge comprising a dual Ethernet 10/100 Mbps MAC interface and 16-Kbyte frame buffer.

The AT75C221 is aimed at networking applications with high data throughputs, including Voice over IP (VoIP). Its integrated OakDSPCore runs signal-processing tasks in parallel to the ARM7TDMI core, which can be dedicated to control functions. This configuration eliminates bottlenecks while keeping power consumption to a minimum.

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2. Absolute Maximum Ratings

Operating Temperature (Commercial) .....0° C to +70° C
Storage Temperature ..... -60° C to +150° C
DC Supply Voltage V_{DDCORE}(Core and PLL).....-0.3V to 1.95V V_{DDIO}(I/Os) .....-0.3V to 3.6V
DC Input Voltage, 3.3VI/Os.... -0.3V to V_{DDIO} + 0.3V, 3.6V max
DC Output Voltage, 3.3VI/Os. -0.3V to V_{DDIO} + 0.3V, 3.6V max

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3. DC Characteristics

3.1 Recommended Operating Conditions

Table 3-1 gives the recommended operating conditions for I/Os.

Table 3-1. Recommended Operating Conditions

Symbol	Parameter		Conditions		Min	Max	Unit
V_{DDCORE}	DC Supply Voltage Core Logic				1.65	1.95	V
V_{DDIO}	DC Supply Voltage I/Os				3.0	3.6	V
T_A	Ambient Temperature				0	+70	°C
V_{IL}	Low Level Input Voltage				-0.3	+0.8	V
V_{IH}	High Level Input Voltage				2.0	V_{DDIO} + 0.3	V
V_{OL}	Low Level Output Voltage	01 drives(1)	I_{OL} = 2 mA			0.4	V
		02 drives(1)	I_{OL} = 4 mA			0.4	V
V_{OH}	High Level Output Voltage	01 drives(1)	I_{OL} = 2 mA		V_{DDIO} - 0.4		V
		02 drives(1)	I_{OL} = 4 mA		V_{DDIO} - 0.4		
C_{IN}	Input Capacitance, inputs and bidir I/Os					5.26	pF
I_{SC}	Static Current		On VDDCORE = 1.8V, ACLK = 0 Hz, DSPCLK = 0 Hz, all inputs driven at 1 (including TMS, TDI, TCK, NRST)	T_A = 25° C		3	mA
				T_A = 70° C		6	mA

Note: 1. For drive levels, see Table 3-2 and Table 3-3.

3.2 Drive Levels

Table 3-2 and Table 3-3 give drive levels for both package options.

Table 3-2. 01 Drive Levels

FSA	PA1	PA7	PA23	PA29	PB3	PB9	PB15
MA_MDIO	PA2	PA8	PA24	PA30	PB4	PB10	SCLKA
MB_MDIO	PA3	PA9	PA25	PA31	PB5	PB11	SPCK
MISO	PA4	PA20	PA26	PB0	PB6	PB12	
MOSI	PA5	PA21	PA27	PB1	PB7	PB13	
PA0	PA6	PA22	PA28	PB2	PB8	PB14	

Table 3-3. 02 Drive Levels

A0	A14	D4	D18	SDCK	MB_TXD1	NRTSA	PA15
A1	A15	D5	D19	DQM0	MB_TXD2	NRTSB	PA16
A2	A16	D6	D20	DQM1	MB_TXD3	NSOE	PA17
A3	A17	D7	D21	DQM2	MB_TXEN	WE	PA18
A4	A18	D8	D22	DQM3	MB_TXER	NWE0	PA19
A5	A19	D9	D23	MA_MDC	CAS	NWE1	STXA
A6	A20	D10	D24	MA_TXD0	NCE0	NWE2	TDO
A7	A21	D11	D25	MA_TXD1	NCE1	NWE3	TXDA
A8	A22	D12	D26	MA_TXD2	NCE2	NWR	TXDB
A9	A23	D13	D27	MA_TXD3	NCE3	PA10	
A10	D0	D14	D28	MA_TXEN	SDCS	PA11	
A11	D1	D15	D29	MA_TXER	NDTRA	PA12	
A12	D2	D16	D30	MB_MDC	NDTRB	PA13	
A13	D3	D17	D31	MB_TXD0	RAS	PA14	

3.3 I/O Circuit Pullups

Unless otherwise specified, the following current values are used for I/Os with internal pullup devices. (Note: The values given are at min and max temperature.)

Table 3-4. I/O Circuit Pullups

Min Current (at Pad = 0V) V_{DDIO} = 3.0V	Max Current (at Pad = 0V) V_{DDIO} = 3.6V
133 µA	350 µA

3.4 I/O Circuit Pulldowns

Unless otherwise specified, the following current values are used for I/Os with internal pull-down devices. (Note: The values given are at min and max temperature.)

Table 3-5. I/O Circuit Pulldowns

Min Current (at Pad = 3.0V) V_{DDIO} = 3.0V	Max Current (at Pad = 3.6V) V_{DDIO} = 3.6V
150 µA	460 µA

3.5 I/O Leakage Currents

The following maximum currents are present at all times when a device is powered up.

Table 3-6. Leakage Currents for All Inputs and Bidirectional Cells

Conditions	Commercial (0 to +70° C)
Leakage Current	-1 µA

4. Power Consumption

The values in Table 4-1 are values measured under typical operating conditions (T_A = 25° C, V_{DDCORE} = 1.8V).

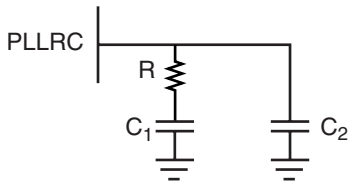
Table 4-1. Power Consumption

Condition			
ARM Clock	OakDSPCore Clock	OakDSPCore Status	$P_{VDDCORE}$
40 MHz	60 MHz	Running	150 mW
40 MHz	60 MHz	Held in reset	146 mW
40 MHz	0 Hz	Held in reset	100 mW

5. PLL Filter

The PLL filter in Figure 5-1 must be used when the crystal oscillator is running at 16 MHz and the PLL output frequency is 240 MHz.

Figure 5-1. PLL Filter



where R = 270 Ohm, C_1 = 47 nF and C_2 = 4.7 nF.

6. 16 MHz Crystal Oscillator Characteristics

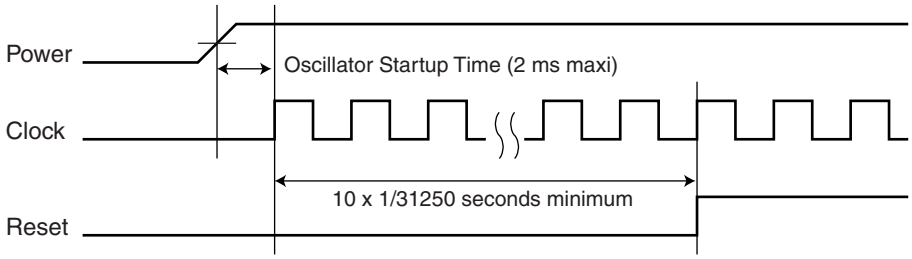
The characteristics in Table 6-1 are applicable for commercial temperature range unless otherwise noted.

Table 6-1. 16 MHz Crystal Oscillator Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Operating Frequency		8		16	MHz
Current Consumption	@ 16 MHz		1	1.8	mA
Duty Cycle		40	50	60	%
Startup Time	With crystal as defined herein			2	ms
Drive Level				150	µW
Equivalent Series Resistance				80	Ohm
Motional Capacitance		5		9	fF
Shunt Capacitance				7	pF
Load Capacitance	Max external capacitors: 40 pF	15		20	pF
Standby Power Dissipation				1	µA

7. Timing Reset

Figure 7-1. Timing Reset



8. Memory Timing Waveforms

Figure 8-1. SDRAMC Read and Write Cycles Timing Diagram

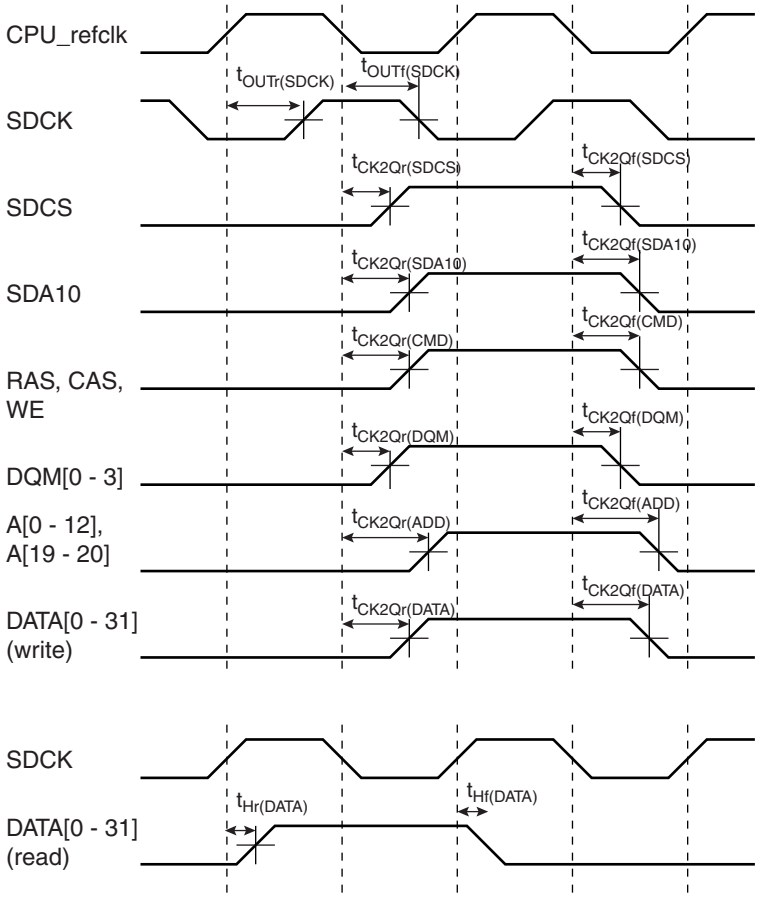
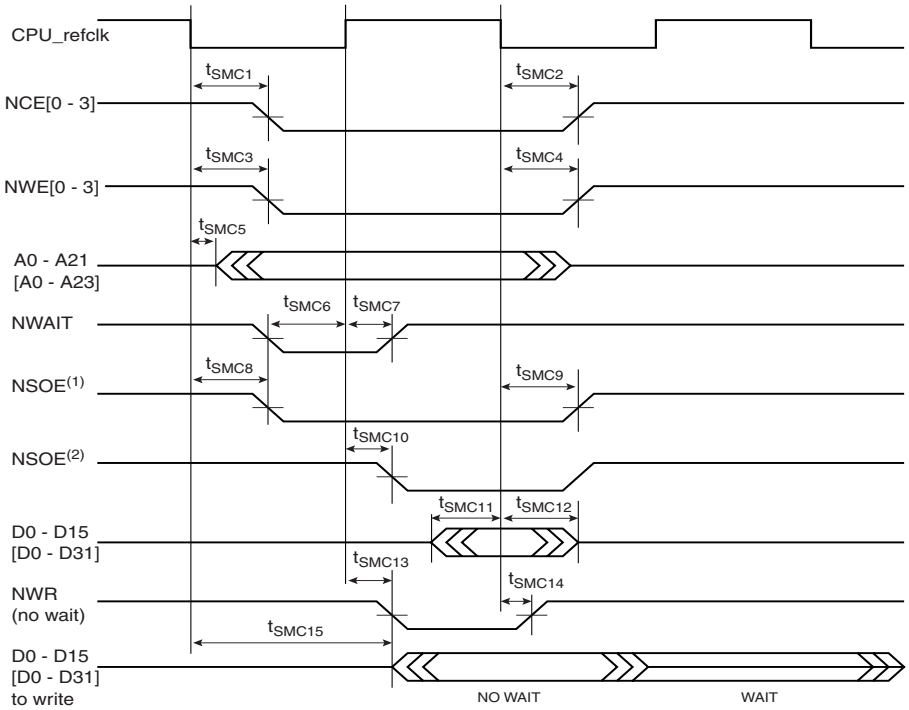


Table 8-1. Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
$t_{OUTr(SDCK)}$ (1, 2)	CPU_refclk rising to SDCK rising			10.78	ns
$t_{OUTf(SDCK)}$ (1, 2)	CPU_refclk falling to SDCK falling			11.68	ns
$t_{CK2Qr(SDCS)}$ (1, 2)	CPU_refclk falling to SDCS rising			6.73	ns
$t_{CK2Qf(SDCS)}$ (1, 2)	CPU_refclk falling to SDCS falling			6.38	ns
$t_{CK2Qr(SDA10)}$ (1, 2)	CPU_refclk falling to SDA10 rising			10.05	ns
$t_{CK2Qf(SDA10)}$ (1, 2)	CPU_refclk falling to SDA10 falling			10.31	ns
$t_{CK2Qr(CMD)}$ (1, 2)	CPU_refclk falling to any command(4) rising			7.77	ns
$t_{CK2Qf(CMD)}$ (1, 2)	CPU_refclk falling to any command(4) falling			7.32	ns
$t_{CK2Qr(DQM)}$ (1, 2)	CPU_refclk falling to DQM[0 - 3] rising			5.20	ns
$t_{CK2Qf(DQM)}$ (1, 2)	CPU_refclk falling to DQM[0 - 3] falling			5.30	ns
$t_{CK2Qr(ADD)}$ (1, 2)	CPU_refclk falling to any address(5) rising			10.05	ns
$t_{CK2Qf(ADD)}$ (1, 2)	CPU_refclk falling to any address(5) falling			10.31	ns
$t_{CK2Qr(DATA)}$ (1, 3)	CPU_refclk falling to any data (write) rising			8.91	ns
$t_{CK2Qf(DATA)}$ (1, 3)	Refclk falling to any data (write) falling			8.90	ns
$t_{Hr(DATA)}$	Any data low hold (read) relative to SDCK rising	1.0			ns
$t_{Hf(DATA)}$	Any data high hold (read) relative to SDCK rising	1.0			ns

Notes:
1. Condition: Load = 0 pF
2. Derating: 0.085 ns/pF (max. 20 pF)
3. Derating: 0.115 ns/pF (max. 20 pF)
4. CAS, RAS, WE
5. A0 - A12, A19 - A20

Figure 8-2. SMC Signals Timing Diagram



Notes: 1. Early Read Protocol
2. Standard Read Protoco

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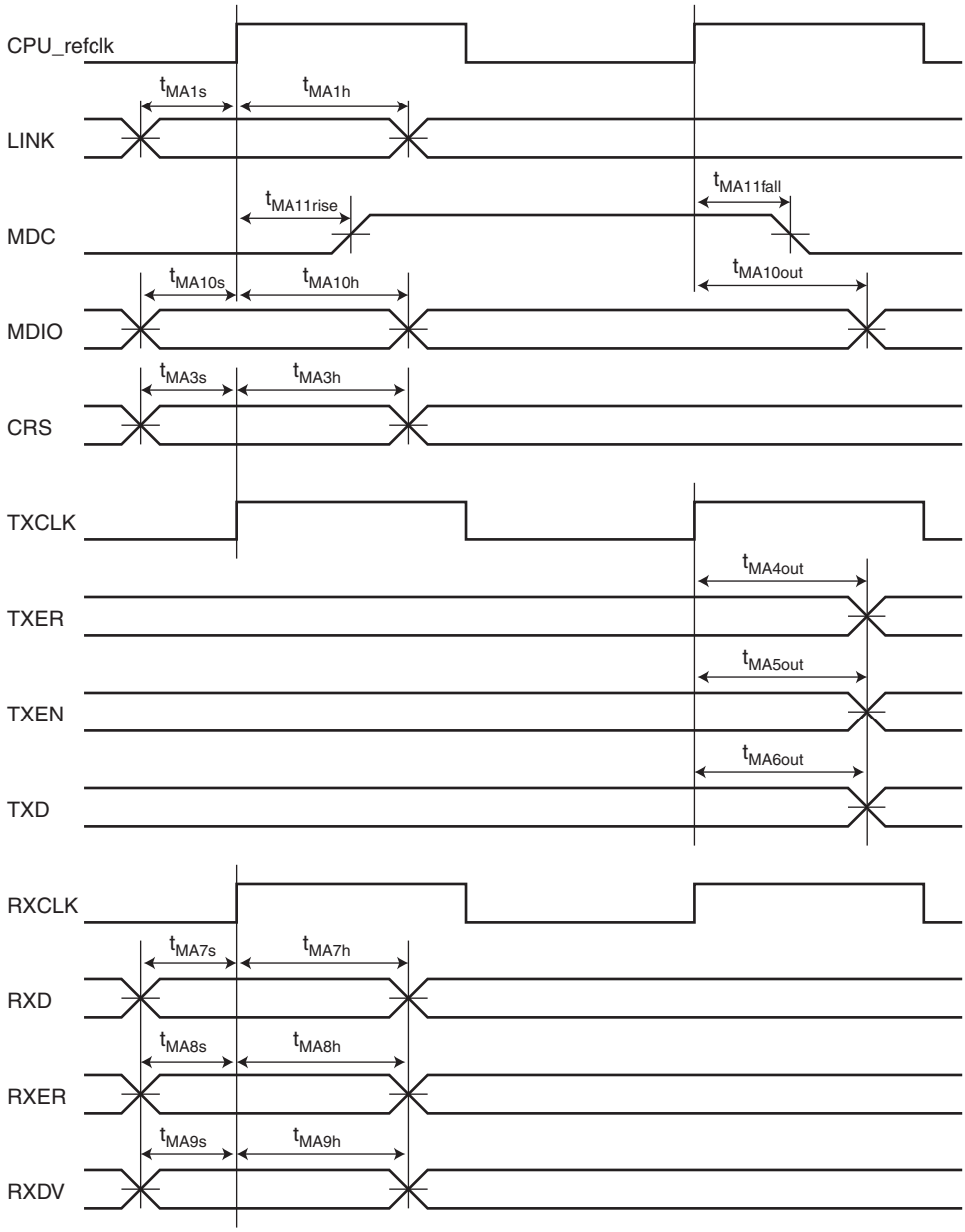
Table 8-2. Timing Parameters (Condition: Load = 0 pF, Derating = 0.085 ns/pF)

Symbol	Parameter	Min (ns)	Max (ns)
t_{SMC1}	CPU_refclk falling to NCE falling	–	8.61
t_{SMC2}	CPU_refclk falling to NCE rising	–	8.98
t_{SMC3}	CPU_refclk falling to NWE falling		8.79
t_{SMC4}	CPU_refclk falling to NWE rising		8.68
t_{SMC5}	CPU_refclk falling to A0 - A21 [A0 - A23](3) valid	–	10.82
t_{SMC6}	NWAIT setup before CPU_refclk rising	6.64	
t_{SMC7}	NWAIT hold after CPU_refclk rising	1.50	
t_{SMC8}	CPU_refclk falling to NSOE falling (1)	–	7.61
t_{SMC9}	CPU_refclk falling to NSOE rising (1) and (2)	–	7.54
t_{SMC10}	CPU_refclk rising to NSOE falling (2)	–	8.10
t_{SMC11}	D0 - D15 setup before CPU_refclk falling	5.81	
t_{SMC12}	D0 - D15 hold after CPU_refclk falling	11.0	
t_{SMC13}	CPU_refclk rising to NWR active	–	8.35
t_{SMC14}	CPU_refclk rising to NWR inactive	–	7.83
t_{SMC15}	CPU_refclk rising to D0 - D15 [D0 - D31](3) out valid	–	17.43

Notes: 1. Early Read Protocol
2. Standard Read Protocol

Figure 8-3. MAC Timing Diagrams



For MAC timing parameters, refer to Table 8-3 on page 10.

Table 8-3. MAC Timing Parameters

Symbol	Parameter	Min (ns)	Max (ns)
t_{MA1s}	Setup for LINK from BCLK	–	0.35
t_{MA1h}	Hold for LINK from BCLK	8.5	–
t_{MA3s}	Setup for CRS from TXCLK rising	–	23.05
t_{MA3h}	Hold for CRS from TXCLK rising	0.5	–
t_{MA4out}	TXER toggling from TXCLK rising, max load 30 pF	–	7.05
t_{MA5out}	TXEN toggling from TXCLK rising, max load 30 pF	–	7.05
t_{MA6out}	TXD toggling from TXCLK rising, max load 30 pF	–	7.15
t_{MA7s}	Setup for RXD from RXCLK	–	0.9
t_{MA7h}	Hold for RXD from RXCLK	1	–
t_{MA8s}	Setup for RXER from RXCLK	–	4.70
t_{MA8h}	Hold for RXER from RXCLK	1.5	–
t_{MA9s}	Setup for RXDV from RXCLK	–	3.2
t_{MA9h}	Hold for RXDV from RXCLK	0.5	–
t_{MA10s}	Setup for MDIO from CPU_refclk	–	3.1
t_{MA10h}	Hold for MDIO from CPU_refclk	8.55	–
$t_{MA10out}$	MDIO toggling from MDC rising	–	3.5
$t_{MA11rise}$	Rising edge of CPU_refclk to rising edge of MDC	–	7.8
$t_{MA11fall}$	Rising edge of CPU_refclk to falling edge of MDC	–	7.8

9. Packaging Information

Figure 9-1. PQFP Package Drawing

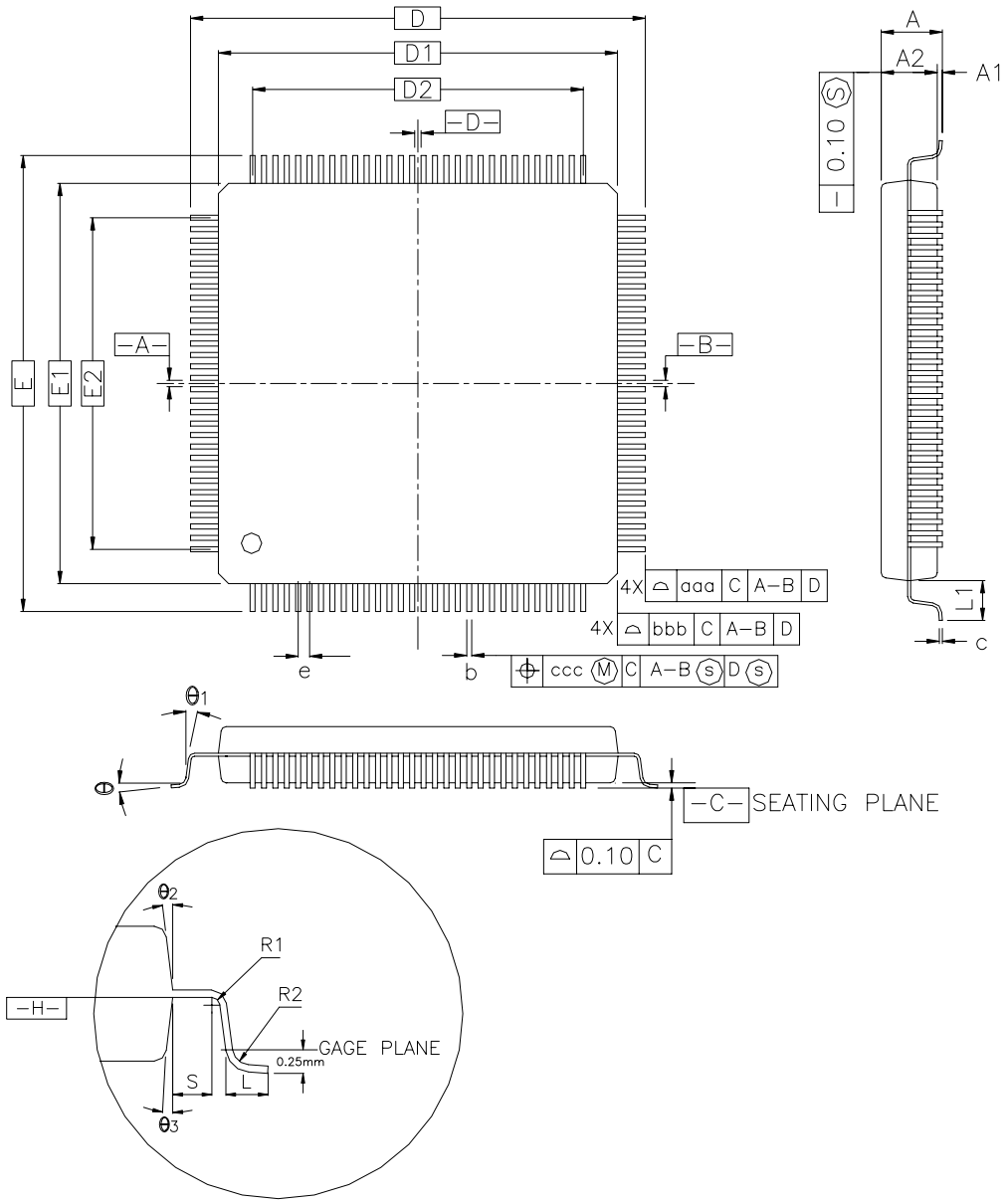


Table 9-1. Package Dimensions for 208-lead PQFP Package (in mm)

Symbol	Min	Nom	Max
A			4.10
A1	0.25		
A2	3.20	3.32	3.60
D	31.20 BASIC		
D1	28.00 BASIC		
E	31.20 BASIC		
E1	28.00 BASIC		
R2	0.13		0.30
R1	0.13		
Q	0°		7°
Q_1	0°		
Q_2	8° Ref		
Q_3	8° Ref		
c	0.11	0.15	0.23
L	0.73	0.88	1.03
L1	1.60 REF		
S	0.20		
b	0.17	0.20	0.27
e	0.50 BSC		
D2	25.50		
E2	25.50		
Tolerances of form and position			
aaa	0.25		0.010
bbb	0.20		0.008
ccc	0.08		0.003

10. Ordering Information

Table 10-1. Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT75C221 - QC - 001	PQFP208	Green	Commercial (0° to +70° C)

Revision History

Doc. Rev.	Date	Comments	Change Request Ref.
6068A	16-Sep-04	First issue.	
6068B	14-Mar-05	Removed all references to BGA package. Package no longer available. Page 1, Description: Updated Information on software modules. Table 3-1, page 2: Updated Static Current parameter values.	CSR 04-402 CSR 05-128
6068C	21-Sep-05	Product and Document reclassified as: “AT75C ARM®-based Microcontrollers” ”Features” on page 1: Reference to application software support removed. Section 1. ”Description” on page 1: The description conforms to product evolution.	Marketing/PBp CSR 05-427