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Features

- High Performance, Low Power AVR[®] 8-Bit Microcontroller
- Advanced RISC Architecture
 - 135 Powerful Instructions Most Single Clock Cycle Execution
 - 32 x 8 General Purpose Working Registers
 - Fully Static Operation
 - Up to 16 MIPS Throughput at 16 MHz
 - On-Chip 2-cycle Multiplier
- Non-volatile Program and Data Memories
 - 32/64/128K Bytes of In-System Self-Programmable Flash
 Endurance: 100,000 Write/Erase Cycles
 - Optional Boot Code Section with Independent Lock Bits
 - USB Bootloader programmed by default in the Factory
 - In-System Programming by On-chip Boot Program hardware activated after reset
 - True Read-While-Write Operation
 - All supplied parts are preprogramed with a default USB bootloader
 - 1K/2K/4K (32K/64K/128K Flash version) Bytes EEPROM
 - Endurance: 100,000 Write/Erase Cycles
 - 2.5K/4K/8K (32K/64K/128K Flash version) Bytes Internal SRAM
 - Up to 64K Bytes Optional External Memory Space
 - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 compliant) Interface
 - Boundary-scan Capabilities According to the JTAG Standard
 - Extensive On-chip Debug Support
 - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- USB 2.0 Full-speed/Low-speed Device and On-The-Go Module
 - Complies fully with:
 - Universal Serial Bus Specification REV 2.0
 - On-The-Go Supplement to the USB 2.0 Specification Rev 1.0
 - Supports data transfer rates up to 12 Mbit/s and 1.5 Mbit/s
- USB Full-speed/Low Speed Device Module with Interrupt on Transfer Completion
 - Endpoint 0 for Control Transfers : up to 64-bytes
 - 6 Programmable Endpoints with IN or Out Directions and with Bulk, Interrupt or Isochronous Transfers
 - Configurable Endpoints size up to 256 bytes in double bank mode
 - Fully independant 832 bytes USB DPRAM for endpoint memory allocation
 - Suspend/Resume Interrupts
 - Power-on Reset and USB Bus Reset
 - 48 MHz PLL for Full-speed Bus Operation
 - USB Bus Disconnection on Microcontroller Request
- USB OTG Reduced Host :
 - Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG dual-role devices
 - Provide Status and control signals for software implementation of HNP and SRP
 - Provides programmable times required for HNP and SRP
- Peripheral Features
 - Two 8-bit Timer/Counters with Separate Prescaler and Compare Mode
 - Two16-bit Timer/Counter with Separate Prescaler, Compare- and Capture Mode





8-bit **AVR**[®] Microcontroller with 64/128K Bytes of ISP Flash and USB Controller

ATmega32U6* AT90USB646 AT90USB647 AT90USB1286 AT90USB1287

*Preliminary Summary



- Real Time Counter with Separate Oscillator
- Four 8-bit PWM Channels
- Six PWM Channels with Programmable Resolution from 2 to 16 Bits
- Output Compare Modulator
- 8-channels, 10-bit ADC
- Programmable Serial USART
- Master/Slave SPI Serial Interface
- Byte Oriented 2-wire Serial Interface
- Programmable Watchdog Timer with Separate On-chip Oscillator
- On-chip Analog Comparator
- Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
 - Power-on Reset and Programmable Brown-out Detection
 - Internal Calibrated Oscillator
 - External and Internal Interrupt Sources
 - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby, and Extended Standby
- I/O and Packages
 - 48 Programmable I/O Lines
 - 64-lead TQFP and 64-lead QFN
- Operating Voltages
 - 2.7 5.5V
- Operating temperature
- Industrial (-40°C to +85°C)
- Maximum Frequency
 - 8 MHz at 2.7V Industrial range
 - 16 MHz at 4.5V Industrial range

1. Pin Configurations

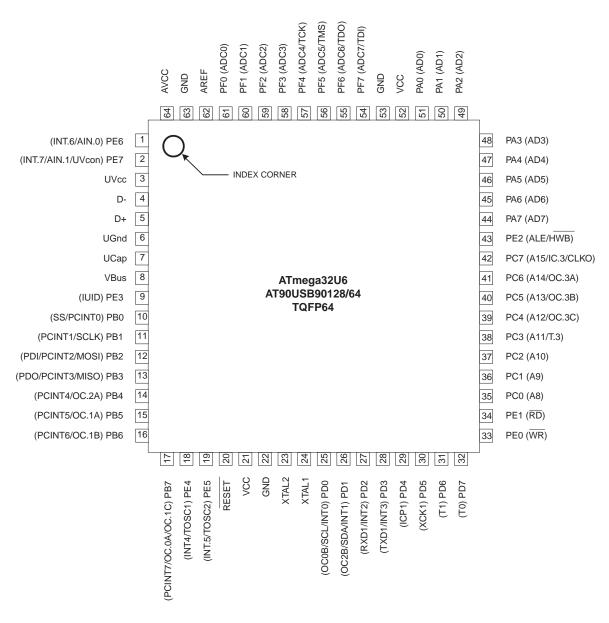
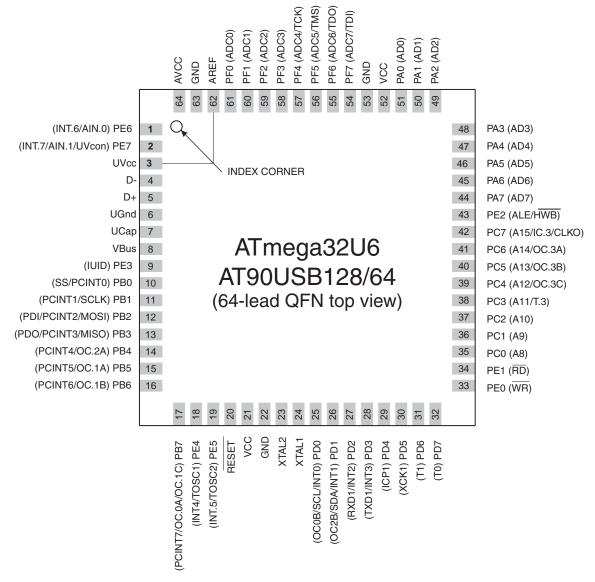


Figure 1-1.Pinout ATmega32U6/AT90USB64/128-TQFP





Figure 1-2. Pinout ATmega32U6/AT90USB64/128-QFN



Note: The large center pad underneath the MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the board to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the board.

1.1 Disclaimer

Typical values contained in this datasheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

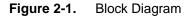
2. Overview

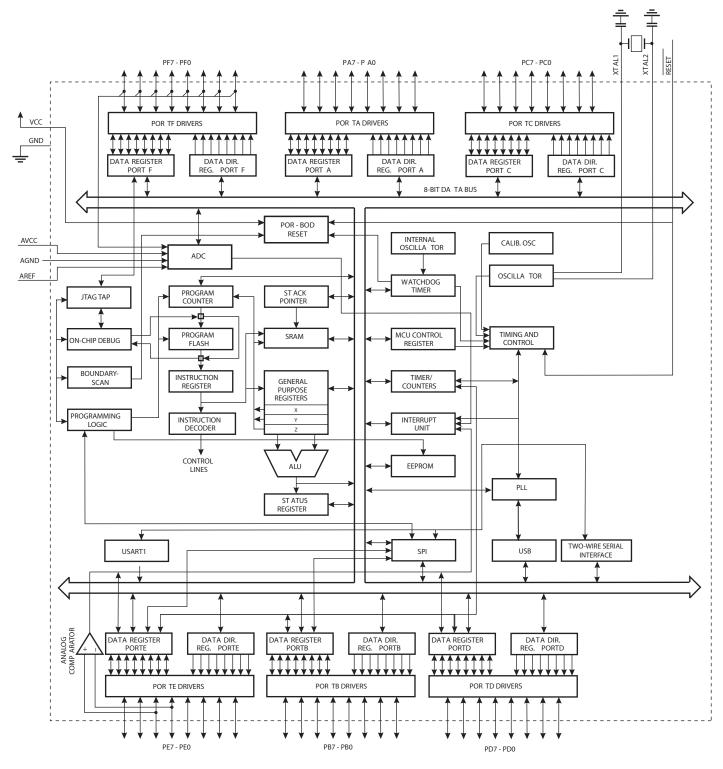
The ATmega32U6/AT90USB64/128 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the

4 ATmega32U6/AT90USB64/128

ATmega32U6/AT90USB64/128 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram









The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega32U6/AT90USB64/128 provides the following features: 32/64/128K bytes of In-System Programmable Flash with Read-While-Write capabilities, 1K/2K/4K bytes EEPROM, 2.5K/4K/8K bytes SRAM, 48 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), four flexible Timer/Counters with compare modes and PWM, one USART, a byte oriented 2-wire Serial Interface, a 8-channels, 10-bit ADC with optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Powersave mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The Onchip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega32U6/AT90USB64/128 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega32U6/AT90USB64/128 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, incircuit emulators, and evaluation kits.

2.2 Pin Descriptions

2.2.1 VCC

Digital supply voltage.

2.2.2 GND

Ground.

2.2.3 AVCC Analog supply voltage.

2.2.4 Port A (PA7..PA0)

Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATmega32U6/AT90USB64/128 as listed on page 79.

2.2.5 Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B has better driving capabilities than the other ports.

Port B also serves the functions of various special features of the ATmega32U6/AT90USB64/128 as listed on page 80.

2.2.6 Port C (PC7..PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of special features of the ATmega32U6/AT90USB64/128 as listed on page 83.

2.2.7 Port D (PD7..PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega32U6/AT90USB64/128 as listed on page 84.





2.2.8 Port E (PE7..PE0)

Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the ATmega32U6/AT90USB64/128 as listed on page 87.

2.2.9 Port F (PF7..PF0)

Port F serves as analog inputs to the A/D Converter.

Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a reset occurs.

Port F also serves the functions of the JTAG interface.

2.2.10	D-	USB Full speed / Low Speed Negative Data Upstream Port. Should be connected to the USB D- connector pin with a serial 22 Ohms resistor.
2.2.11	D+	USB Full speed / Low Speed Positive Data Upstream Port. Should be connected to the USB D+ connector pin with a serial 22 Ohms resistor.
2.2.12	UGND	USB Pads Ground.
2.2.13	UVCC	USB Pads Internal Regulator Input supply voltage.
2.2.14	UCAP	USB Pads Internal Regulator Output supply voltage. Should be connected to an external capacitor (1 μ F).
2.2.15	VBUS	USB VBUS monitor and OTG negociations.
2.2.16	RESET	Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 8-1 on page 58. Shorter pulses are not guaranteed to generate a reset.
2.2.17	XTAL1	Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

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2.2.18	XTAL2	Output from the inverting Oscillator amplifier.
2.2.19	AVCC	AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to V_{CC} , even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.
2.2.20	AREF	This is the analog reference pin for the A/D Converter.

3. About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

These code examples assume that the part specific header file is included before compilation. For I/O registers located in extended I/O map, "IN", "OUT", "SBIS", "SBIC", "CBI", and "SBI" instructions must be replaced with instructions that allow access to extended I/O. Typically "LDS" and "STS" combined with "SBRS", "SBRC", "SBR", and "CBR".





4. Register Summary

OWF: Restrict ·<	Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
Burnolis Reserved .	(0xFF)	Reserved	-	-	-	-	-	-	-	-	
Import Reserved Image: second secon		Reserved	-	-	-	-	-	-	-	-	
OP/B0 Reserved · <	(0xFD)	Reserved	-	-	-	-	-	-	-	-	
Output Reserved Output Perton Value (0x98) UPNCT PROCK PROCK PROCK (0x98) UPNCT PROCK PROCK PROCK (0x98) UPNCK PROCK PROCK PROCK (0x98) UPNCK PROCK PROCK PROCK (0x98) UPNCK PROCK PROCK PROCK (0x94) UENK PROCK PROCK PROCK (0x94) UENK PROCK PROCK PROCK (0x92) UESAX PCOCK VERN PROCK PROCK (0x15) UESTAX PCOCK VERN PROCK PROCK PROCK (0x15) UESTAX PCOCK VERN PROCK PROCK PROCK (0x15) UESTAX PCOCN VERN NAUCE PROCK PROCK (0x15) UESTAX PCOCN NAUNN NAUCE PROCK PROCK (0x15) UESTAX PCOCN	(0xFC)	Reserved	-	-	-	-	-	-	-	-	
(be/B) OTGTORN PAGE PR/TE PR/TE (be/B) UPBCLX - - PBCT33 (be/B) UPBCLX - - PBCT33 (be/B) UPBCLX - - PBCT33 (be/B) UPBCLX - - - PBCT3 (be/B) UPBCLX - - - - - (be/B) UBBCLX - - - - - - (be/B) UBBCLX - - - - - - - (be/B) UBBCLX - NACOTE PASTPC TOTACITE TSTALED TOTACITE TSTALED - </td <td>(0xFB)</td> <td>Reserved</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td>-</td> <td></td>	(0xFB)	Reserved	-	-	-	-	-	-	-	-	
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(br/r) UPBCX Image: state of the state				PA	GE				VA	LUE	
OMPS UPSRX CONNTREH0 PPVCT0 OMPS UERDN CONNTREH0 CONNTREH0 ERNT0 OMPS UERDN S SVCT00 SVCT00 OMPS UERDN S SVCT00 SVCT00 OMPS UERDN FLERR NAMOUT RXSTPE RXCUTE STALLDDE TAINE OMPS UERDNX CFLORD DATA0 DATA0 COURSENTO OMPS UERDNX FLERRE NAMOUTE RXSTPE RXCUTE STALLDDE TAINE OMPS UERTAX CFLORDE STALLDD TAILAGE RSTD EPNRT0 OMES UERTAX CFLORDE STALLDD TAILAGE RSTD EPNRT0 OMES UERTAX CFLORDE STALLDD RSTD EPNRT0 EPNRT0 OMES UERTAX CFCON NAMOUT RSTD EPNRT0 EPNRT0 OMES UDNUM EPNZT0 RAMOUT EPNRT0 STALLDD TAILDD EPNRT0											
(b/Fg) UPERX - COUNTERT:0 CRUE THEOUT PID DATAPID DATAPID DATAPID (b/Fg) UEBCLK - - BVCTI0.8 BVCTI0.8 BVCTI0.8 (b/Fg) UEBCLK - BVCTI0.8 BVCTI0.8 BVCTI0.8 BVCTI0.8 (b/Fg) UEBCLK FLERKE NAKINE BVCTI0.8 CIRLING TAILEDE TAILEDE <t< td=""><td></td><td></td><td>-</td><td>-</td><td>-</td><td></td><td></td><td></td><td>PBYC110:8</td><td></td><td></td></t<>			-	-	-				PBYC110:8		
IDM-40 UBEN EPMID 0 IDM-20 UEBCX BYCT 10 BYCT 10 IDM-20 UEBCX DATT 3 STALLEDE TAILEDE IDM-20 UEBCX FLEME NAKINE NAKINE STALLEDE TAILEDE IDM-20 UESTAIX CFGOX OVERFI UNDERFI DTSED10 NULEVEST IDM-20 UESTAIX CFGOX OVERFI UNDERFI DTSED10 NULEVEST IDM-20 UECOXX EFPVER10 STALLEDE EFPVER10 ALLCO IDM-20 UECOXX EFPVER10 STALLEDE EFPVER10 FPVER10 IDM-20 UECOXX EFPVER10 STALLEDE EFPVER10 FPVER10 IDM-20 UECOXX EFPVER10 STALLEDE EFPVER10 FPVER10 IDM-20 UECOXX FFPVER10 STALLEDE TXNI FFVER10 IDM-20 UENDAR FFVER10 STALLEDE TXNI FFVER10 IDM-20 UENDAR FFVER10 NAKUPI				COUN	TED1:0			BID		DATATO	
(№3) UEBCIX .	. ,		-	COON	IERI.U	CRC10		FID	DATAFID	DATATGL	
(bF2) UEBATX DURATO (b4F) UEBATX FLERE NAKINE P.XSTPE RXSTPE RVUTE STALLEDE TXNE (b4F) UESTAX CFGOK OVERFI UNDERFI OTSEG10 NUUVEKIO (b4E) UESTAX CFGOK OVERFI UNDERFI OTSEG10 NUUVEKIO (b4E) UECOGX EFYPTE3 EFYSTD ALLOC EFYDTS (b4E) UECOGX EFYPTE3 EFYSTD EFYDTS EFYDTS (b4E) UECOGX EFYTA EFYSTD EFYDTS EFYDTS (b4E) UECOX EFYDTS EFYDTS EFYDTS EFYDTS (b4E) UECOX EFYDTS EFYDTS EFYDTS EFYDTS (b4E) UESTAX FFUCCO NAKIN NAVAL NACUTI EFYDTS EFYDTS (b4E) UENNA FFUCCO NAKIN RVAL NACUTI EFYDTS EFYDTS (b4E) UDFNIML FFUCCO NAKIN RVAL			-	-	-	-	-		BYCT10:8		
(b/F) UEBXX DAT/D RXDTE STALEDE TALEDE TALEDE <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>CT7:0</td> <td></td> <td></td> <td></td> <td></td>							CT7:0				
(b/F) UBETXAX - - - CTRLOR RXOUTE RXOUTE RXOUTE STALLERE TYNRE (b/EF) UESTAX CFG0K OVERPI UNDERRI DTSG19 NUSYBK10 (b/Eb) UECF01X FPG0K OVERPI NUSYBK10 ALLOC (b/Eb) UECF01X FPG0K STALLER STALLER FPG0K (b/Eb) UECF01X FPG0XN STALLER RSTT FPUN20 (b/Eb) UEC00XX FPF0XN STALLER RSTT FPUN20 (b/Eb) UENIM UENIM STALER STALER FPUN20 (b/Eb) UENIX FPO20N NAKIN RVALTIR RSTT STALER FVUN20 (b/Eb) UENIX FPO20N NAKIN RVALTIR RSTT STALER											
IMBER UBSTRO 10 NURSTRI 0 NURSTRI 0 NURSTRI 0 IMAED UECFORX EPSRES EPSRES EPRR ALLOS IMAED UECFORX EPSTRI 0 ALLOS EPRR IMAED UECRORX EPSRES EPRR EPRR IMAED UERDARX PIPOCON NAKINI RNATUR EPRL IMAED UENNAR PIPOCON NAKINI RNATUR RSATUR FIPULARZO IMAED UENNAR PIPOCON NAKINI RNATUR RSATUR STALLED TATALED IMAED UENNAR PIPOCON NAKINI RVATUR RSATUR STALLED TATALED IMAED UDENT UDENT UADDR TATALED STALLED STALLED TATALED IMAED UDENT UDENT UADDR STALLED STALLED </td <td></td> <td></td> <td>FLERRE</td> <td>NAKINE</td> <td>-</td> <td>1</td> <td>1</td> <td>RXOUTE</td> <td>STALLEDE</td> <td>TXINE</td> <td></td>			FLERRE	NAKINE	-	1	1	RXOUTE	STALLEDE	TXINE	
(NEC) UECFGX EPV/L0 EPV/L0<	(0xEF)	UESTA1X	-	-	-	-	-	CTRLDIR	CURF	RBK1:0	
(b6C) UECOX EPVPE10 rst rst< rst rst rst rst rst rst rst rst< rst rst< rst <td>(0xEE)</td> <td>UESTA0X</td> <td>CFGOK</td> <td>OVERFI</td> <td>UNDERFI</td> <td>-</td> <td>DTSE</td> <td>EQ1:0</td> <td>NBUS</td> <td>YBK1:0</td> <td></td>	(0xEE)	UESTA0X	CFGOK	OVERFI	UNDERFI	-	DTSE	EQ1:0	NBUS	YBK1:0	
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(0:E4) UDPNUML FRUM70 (0:K2) UDADR ADDR UPRSME EORSME WAKEUPE EORSTE SOFE SUSPE (0:K2) UDINT UPRSME EORSME WAKEUPE EORSTE SOFE SUSPE (0:K2) UDINT UPRSME EORSME WAKEUPE EORSTE SOFE SUSPE (0:K2) UDOCN EORSTE SOFE LSM RMWKUP DETACH (0:KDF) OTGINT STOE HNPERE ROLEEXE BCERRE VBERRE SRPE (0:KDC) Reserved HNPREQ SRPEE ROLEEXE BCERRE VBUSRCQ VBUSRQC (0:KDA) USBNT ID HNPREQ SRPEED IDT VBUSTE (0:KDB) USBCAN USBE HOST FRZCLK OTGPADE IDT VBUSTE (0:KDB) USBCAN UMOD UDE UVCONE IDTE VBUSTE (0:KD5) Reserved ID UVECONE IDTE						FNCERR					
(0xE3) UDADOR ADDEN UPRSME EORSME WAKEUPE EORSTE SOFE SUSP (0xE1) UDINT UPRSME EORSME WAKEUPE EORSTE SOFI SUSP (0xE0) UDCON STOI HNPERNI ROLEEXI BCERRI VBERRE SRPE (0xDF) OTGINT STOI HNPERNI ROLEEXI BCERRI VBERRE SRPE (0xDC) OTGION HNPERNI ROLEEXI BCERRI VBERRE SRPE (0xDC) Reserved HNPERO SRPEQ SRPED IDT VBUSRQC (0xDA) USBSTA SPEED ID VBUST (0xDA) USBSTA UDE UVCONE UVREGE UVREGE (0xDA) Reserved UVREGE UVREGE (0xD3) Reserved (0xD3) Reserved <						ENI	IM7:0		FINUMITU:8		
(bc2) UDEN UPRSME EORSME WAKEUPL EORSTI SOFE SUBPL (bx51) UDINT UPRSMI EORSMI WAKEUPL EORSTI SOFI SUSPL (bx65) UDCON INDERNI EORSTI SOFI LSM RMWRUP DETACH (bx0b) OTGINT STOI HNPERRI ROLEXE BCERRI VBERRI SRPE (bx0b) OTGOON HNPERRE ROLEXE BCERRI VBUSREQ VBUSRQC (bx0b) OTGOON HNPERRE SRPEQ SRPEQ SRPED VBUSHC VBUSRQC (bx0b) Reserved IDT VBUST IDT VBUST VBUST (bx0b) USBEON UBBE HOST FRZCLK OTGPADE IDT VBUST (bx0b) UBBCON UBBE HOST FRZCLK OTGPADE IDT VUSTE (bx0b) Reserved IDT VBUST IDT VBUSTE IDTE VBUSTE (bx						1 10					
(bcf) UDINT UPRSMI EORSMI WAKEUPI EORSTI SOFI SUSPI (0x60) UDCON Image: STOL STOL HNPERRI ROLEX. BCCRRI VBERRI SKPI (0x0F) OTGINT STOL HNPERRI ROLEX. BCCRRI VBERRI SKPI (0x0F) OTGION HNPRQ SRPEQ SRPEL VBUSNC VBUSNCQ VBUSNQQ (0x0D) Reserved Image: Stole SPEEQ SRPEL VBUSNCQ VBUSNQQQ (0x0B) Reserved Image: SPEQ SRPEQ SRPEL IDT VBUSTI (0x0B) USBSTA Image: SPECD ID VBUST VBUSTI VBUSTI VBUSTI (0x0D) USBCON UMOD UIDE U/CONE IDT VBUSTI (0x0D) Reserved Image: SPED IDT VBUSTI VREGE IDT (0x0D) Reserved Image: SPED IDT VVBUSE IDT VVBUSE IDT VVBUSE </td <td></td> <td></td> <td>ADDEN</td> <td>UPRSME</td> <td>FORSME</td> <td>WAKEUPE</td> <td>r</td> <td>SOFE</td> <td></td> <td>SUSPE</td> <td></td>			ADDEN	UPRSME	FORSME	WAKEUPE	r	SOFE		SUSPE	
(0xE0) UDCON and STOI HNPERI ROLEXI BCERR VBERR SRPI (0xDF) OTGINT STOI HNPERR ROLEXI BCERR VBERR SRPI (0xDD) OTGCON HNPERQ SRPEQ SRPEQ SRPEQ VBUSNC VBUSNC (0xDD) Reserved (0xDA) USBINT (0xDA) USBINT SPEED ID VBUST (0xDB) USBCON USBE HOST FRZCLK OTGPADE ID VBUST (0xD6) Reserved <td< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></td<>											
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(0xDD) OTGCON Image and the served Image and the served <th< td=""><td></td><td></td><td></td><td></td><td>STOI</td><td>HNPERRI</td><td>ROLEEXI</td><td></td><td></td><td></td><td></td></th<>					STOI	HNPERRI	ROLEEXI				
(0xDC) Reserved Image: constraint of the served Image: constr	(0xDE)	OTGIEN			STOE	HNPERRE	ROLEEXE	BCERRE	VBERRE	SRPE	
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(bxD7) UHWCON UIMOD UIDE UVCONE UVREE (0xD6) Reserved							SPEED				
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(bxD5) Reserved Image: Constraint of the served Image: Conserved Image: Constraint of the ser			UIMOD	UIDE		UVCONE				UVREGE	
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(0xCF) Reserved - <			-	-	-	-	-	-	-		
(0xCD)UBR1HUSART1Bud Rate Register High Byte(0xCC)UBR1LUSART1Bud Rate Register Low Byte<	, ,			-			-				
OXCC) UBR1L USART1 Baud Rate Register Low Byte (0xCB) Reserved -		UDR1				USART1 I/C	Data Register				
(0xCB) Reserved - <	(0xCD)	UBRR1H	-	-	-	-	U	SART1 Baud Ra	te Register High B	syte	
(0xCA) UCSR1C UMSEL11 UMSEL10 UPM11 UPM10 USS1 UCS211 UCS210 UCPOL1 (0xC9) UCSR1B RXCIE1 TXCIE1 UDRIE1 RXEN1 TXEN1 UCS212 RXB81 TXB81 (0xC8) UCSR1A RXC1 TXCI UDRE1 FE1 DOR1 PE1 U2X1 MPCM1 (0xC7) Reserved - - - - - - - (0xC6) Reserved - - - - - - - - (0xC6) Reserved - <	(0xCC)	UBRR1L			l	JSART1 Baud Ra	ate Register Low I	Byte			
(0xC9) UCSR1B RXCIE1 TXCIE1 UDRIE1 RXEN1 TXEN1 UCSZ12 RXB81 TXB81 (0xC8) UCSR1A RXC1 TXC1 UDRE1 FE1 DOR1 PE1 U2X1 MPCM1 (0xC7) Reserved - - - - - - - (0xC6) Reserved -						-	-				
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10 ATmega32U6/AT90USB64/128

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(bbb) TWAMB TWAM5 TWAM5 <th< th=""><th></th><th>_</th><th></th><th></th><th></th><th></th><th></th><th>· · · · ·</th><th></th><th>i age</th></th<>		_						· · · · ·		i age
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(0.097) Reserved -			TWS4	Ļ		TWS3	-	TWPS1	TWPS0	
(DeB) ASR EXCLK AS2 TONUB OCR2AUB OCR2AUB TOR2UB	nterfa	2-wire	wire Serial Int	Interfa	face B	Bit Rate Regi	ster			
(D0B5) Reserved . <			-			-	-	-	-	
(i) Bit OCR28 Times/Counter2 Output Compare Register A (i) BitS) OCR2A Times/Counter2 (B Bit) (i) BitS) TCCR2B FOC2A FOC2B WGM22 CS22 CS21 CS22 (i) BitS) TCCR2B COM2A1 COM2B0 WGM22 CS22 CS21 CS22 (i) BitS) TCCR2B COM2A1 COM2B0 WGM22 CS22 CS21 CS22 (i) BitS) TCCR2B COM2A1 COM2B0 WGM22 CS22 CS21 CS22 (i) MAD UPERXA FLERRE<	В	_	TCN2UB	IB	0	OCR2AUB	OCR2BUB	TCR2AUB	TCR2BUB	
(DB3) OCR2A TimerCounter2 Output Compare Register A (DB3) TCKT2 TimerCounter2 Dign Compare Register A (DB4) TCCR2B FOC2A FOC2A COM2A COM2A COM2A COM2A (DM4F) UPDATX. PDAT7.0 WGM2 CS22 CS21 CS22 (DM4F) UPDATX. PDAT7.0 WGM2 CS22 CS21 CS22 (DMAF) UPERGX PERRE TXSTPE TXOUTE RXSTALLE RXIN (DAAG) UPCFGX PEREZE INMODE PERTO NBUSYBK1.0 NBUSYBK1.0 (DAAB) UPCFGX PFREZE INMODE PERTO PERTO PERTO (DAAB) UPCGX PFREZE INMODE PERTO PERTO PERTO (DAA4) UPENTX FFCCON NAKEDI RVAL PERTO PENUM20 PE			-			-	-	-	-	
(bB2) TCKT2 Time#Counter2 (B B) (bB3) TCCR2A COM2A1 COM2A0 COM2B0 VGM22 CS22 CS21 CS21 CS22 CS21 VGM21 VGM21<										
IDB11 TCCR28 FOC28 FOC28 COM291 COM281 COM281 <td></td> <td>imer/C</td> <td></td> <td></td> <td></td> <td>1 0</td> <td>ister A</td> <td></td> <td></td> <td></td>		imer/C				1 0	ister A			
(b)(b) TCOR2A COM2A1 COM2A0 COM2B1 COM2D1 PDAT70 (b)(AF) UPPENX FLERRE NAKEDE PERRE TXSTPE TXOUTE RXSTALLE RXINI (b)(AG) UPCFG2X CFGOK OVERRI UNDERFI DTSEC1:0 NBUSYBK1:0 (b)(AG) UPCFG2X CFGOK OVERRI UNDERFI PERLEZ:0 PBN1:0 ALLOC (b)(AA) UPCFG3X PTVPE1:0 PTVEN1:0 PERNUM3:0 PENNUM3:0 (b)(AA) UPCFG3X PTVPE1:0 PTVEN1:0 RSTOT PENNUM3:0 (b)(AA) UPCRG3X PTREEZE INMODE RSTOT PENNUM2:0 (b)(AA) UPNTX FIFCON NAKEDI RWAL PERI TXSTPI TXOUTI RXSTALL RXIN (b)(AA) UHPNX FIFCON NAKEDI RWAL PERN INRC2:0 INRC2:0 (b)(AA) UHPNX FIFCON NAKEDI RSTE DDISCE DDISCE INRC2:0 INRC2:0 <t< td=""><td>er/Cou</td><td></td><td></td><td>er/Cou</td><td></td><td></td><td>6833</td><td>0821</td><td>6820</td><td></td></t<>	er/Cou			er/Cou			6833	0821	6820	
(IDAAF) UPEATX PLERRE NAKEDE PERRE TXSTPE TXOUTE RXSTALLE RXINUTE (IDAAF) UPCGG2X FLERRE NAKEDE INTFR070 INTFR070 (IDAAF) UPCGG1X CFG0K OVERFI UNDERFI DTSE01:0 NBUSVEK1:0 (IDAAF) UPCG61X PTYPE1:0 PFIXE2:0 PFIXI.3 ALLOC (IDAAF) UPCG0X PTYPE1:0 PTOREN1:0 PENUM3:0 ALLOC (IDAAF) UPCG1X PTREEZE INMODE RSTOT PENUM2:0 (IDAAF) UPOXXX PTREEZE INMODE PRIST:0 PNUM2:0 (IDAAF) UPNUM PREEXT:0 NAKEDI RSTOT RSTALLI RXIN (IDAAF) UPNUM2 FILENT:0 FNUM10:8 NUH7:0 FNUM10:8	0			20		WGIVIZZ	0322			
(IVAE) UPERX FLERR NAKEDE PERRE TXUTTE TXUTTE RXSTALLE RXINL (IVAD) UPGT2X CFGOK OVERFI UNDERFI DTSEQ1:0 NBUSYBK1:0 (IVAAB) UPCFGOX PTOKEN:0 PSIZE:0 PBK1:0 ALLOC (IVAAB) UPCFGOX PTYPE:0 PTOKEN:0 PENENUM3:0 PLANUM3:0 (IVAAB) UPCFGOX PTYPE:0 PTOKEN:0 RSTDT PEN (IVAA) UPCROX PTYPE:0 PRNE7:0 PUNMA:0 PLANUM2:0 (IVAA) UPINIX FIFCON NAKEDI RWAL PERRI TXSTPI TXOUTI RXSTALLI RXIN (IVAA) UPINIX FIFCON NAKEDI RWAL PERRI TXSTPI TXOUTI RXIALI RXIN (IVAA) UHINIX FIFCON NAKEDI RWAL PERRI TXSTPI TXOUTI RXIALI RXIALI RXIALI RXIALI RXIALI RXIALI RXIALI RXIALI RXIALI RXIALI<						-	-	WGIVI21	WGIWIZO	
(bxAD) UPCFG2X INTERG7:0 (bxAC) UPSTAX CFGOK OVERFI UNDERFI DTSE01:0 NBUSYBK10 (bxAA) UPCFG3X PTYPE1:0 PTOKEN1:0 PENUM3:0 ALLOC (bxAA) UPCFG3X PTYPE1:0 PTOKEN1:0 PENUM3:0 PENUM3:0 (bxAB) UPCG3X PTREEZE INMODE RSTDT PENUM3:0 (bxAB) UPNTX FIFOCON NAKEDI RWAL PERT TXSTPI TXOUTI RXSTALLI RXIN (bxA6) UPINTX FIFOCON NAKEDI RWAL PERT TXSTPI TXOUTI RXSTALLI RXIN (bxA6) UPINTX FIFOCON NAKEDI RWAL PERT TXSTPI TXOUTI RXSTALLI RXIN (bxA6) UHINTX FIFOCON NAKEDI RXIN RSMEDI RSTT DDISCE DCON (bxA7) UHINTMIN HWUPI HSOFE RXRSME RSMEDI RSTT DDISCI DCON							TXOUTE	RXSTALLE	RXINE	
(INAC) UPSTAX CFGOK OVERFI UNDERFI DTSEC10 NBUSYBK10 (IbxAB) UPCFG1X PSIZE20 PBK10 ALLOC I (IbxAB) UPCFG1X PTYPE10 PTOKEN10 PENUM30 I (IbxAB) UPCG0X PTYPE10 PTOKEN10 PST50 PENUM20 (IbxAD) UPNUM PREZZ INMODE RSTDT PENUM20 (IbxAD) UPINTY FIFOCON NAKEDI RWAL PERTI TXSTPI TXOUTI RXSTALLI RXILLI RXI										
(bxAa) UPCFG0X PTYPE1:0 PTOKEN1:0 PENUM3:0 (bxAg) UPCONX PFREEZE INMODE RSTDT PEN (bxAg) UPNUM PRST6.0 PNUM2:0 PNUM2:0 (bxAg) UPNUM RWAL PERE TXSTPI TXOUTI RXTALL RXIN (bxAg) UPINROX FFROCON NAKEDI RWAL PEREI TXSTPI TXOUTI RXTALL RXIN (bxAd) UHFNUMH FNUM7:0							EQ1:0	NBU	SYBK1:0	
(0xA9) UPCONX PFREEZE INMODE RST0 PEN (0xA8) UPRST PRST6.0 PRST6.0 PRST6.0 (0xA6) UPNTX FIFOCON NAKEDI RVAL PERI TXST1 TXOUTI RXSTALLI RXIN (0xA6) UPINTX FIFOCON NAKEDI RVAL PERI TXST1 TXOUTI RXSTALLI RXIN (0xA4) UHFLEN FILOZO NAKEDI RVAL FILOZO FNUM7.0 <		_			L			ALLOC		
(0xA8) UPRST PRST6:0 PRST6:0 (0xA7) UPNUM PIPOLO PAUMA PERT TXSTPI TXOUTI RXALL RXII (0xA6) UPINROX INRG7:0 TXSTPI TXOUTI RXIII RXII (0xA3) UHFNUM INRG7:0 FLEN7:0 FNUM10:8 FNUM10:8 (0xA2) UHFNUMH FNUM7:0 FNUM10:8 FNUM10:8 FNUM10:8 (0xA0) UHEN HADDR FNUM7:0 FNUM10:8 EXEMPT (0xA0) UHINT HYUPE HSOFE RXRSME RSMEDE RST DDISCE DCONT (0x40) UHINT HYUPI HSOFE RXRSME RSMEDE RST DDISCE DCONT (0x40) OCR3CH Timer/Counter3 - Output Compare Register C Low Byte SOFE OVAD RST DDISCE DCONT (0x90) OCR3CH Timer/Counter3 - Output Compare Register C Low Byte SOFE OVAD SOFE SOFE SOFE SOFE SOFE SOFE		KEN1	EN1:0				PEP	NUM3:0		
(0xA7) UPNUM PNUM2:0 (0xA6) UPNTX FIFOCON NAKEDI RWAL PERRI TXSTPI TXOUTI RXSTALLI RXIN (0xA6) UPNRXX FIFOCON NAKEDI RWAL PERRI TXSTPI TXOUTI RXSTALLI RXIN (0xA3) UHFNUMH FLEN7:0 FNUM10:8									PEN	
(0xA6) UPINTX FIFOCON NAKEDI RWAL PERRI TXSTPI TXOUTI RXSTALLI RXIN (0xA4) UHFRUMH INR07:0					1	PRST6:0				
(bxA5) UPINROX INRG7:0 (bxA4) UHFLEN FLEM7:0 (bxA2) UHFRNUMH FNUM7:0 (bxA1) UHADDR FNUM7:0 (bxA2) UHFNUML FNUM7:0 (bxA2) UHFNUML HWUPE HSOFE RXRSM RSMEDE RSTE DDISCE DCONN (bxA2) UHINT HWUPE HSOFE RXRSM RSMEDE RSTE DDISCE DCONN (bx9F) UHINT HWUPE HSOFE RXRSM RSMEDE RSTE DDISCE DCONN (bx9D) OCR3CH Timer/Counter3 - Output Compare Register C Low Byte SOFE (bx9D) OCR3CH Timer/Counter3 - Output Compare Register A High Byte SOFE (bx9D) OCR3CH Timer/Counter3 - Output Compare Register A High Byte SOFE (bx9D) OCR3CH Timer/Counter3 - Output Compare Register High Byte SOFE (bx9D) OCR3AL Timer/Counter3 - Input Capture Register High Byte SOFE (bx9D) CCR3AL Timer/Counter3 - Input Capture Register High Byte SOFE SOFE SOFE <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></t<>										
(0xA4) UHFLEN FLEN7:0 (0xA3) UHFNUML FNUM7:0 (0xA4) UHFNUML FNUM7:0 (0xA0) UHADDR HADDR:0 (0xA0) UHEN HWUPE (0x66) UHEN HWUPE (0x67) UHIN HWUPE (0x67) URIN HWUPE (0x67) URIN HWUPE (0x67) OCR3CH Timer/Counter3 - Output Compare Register C High Byte (0x68) OCR3CH Timer/Counter3 - Output Compare Register B Low Byte (0x68) OCR3L Timer/Counter3 - Output Compare Register Low Byte (0x68) OCR3L Timer/Counter3 - Input Capture Register High Byte (0x68) ICR3L Timer/Counter3 - Input Capture Register Low Byte (0x69) ICR3L Timer/Counter3 - Counter Register High Byte (0x69) TCNT3L Timer/Counter3							TXOUTI	RXSTALLI	RXINI	
(0xA3) UHFNUMH FNUM10.8 (0xA2) UHFNUML FNUM10.8 (0xA2) UHFNUML FNUM10.8 (0xA0) UHEN HWUPE HSOFE RXRSME RSMEDE RSTE DDISCE DCONI (0xA0) UHINT HWUPE HSOFE RXRSME RSMEDE RSTE DDISCE DCONI (0x46) UHINT HWUPE HSOFE RXRSME RSMEDE RSTE DDISCE DCONI (0x67) UHINT HWUPE HSOFE RXRSME RSMEDE RSTE DDISCE DCONI (0x69) OCCR3CL Timer/Counter3 - Output Compare Register C Low Byte (0x69) OCCR3AL Timer/Counter3 - Output Compare Register B High Byte (0x69) ICR3H Timer/Counter3 - Output Compare Register A Low Byte (0x69) ICR3H Timer/Counter3 - Output Compare Register A Low Byte (0x69) ICR3H Timer/Counter3 - Input Capture Register Low Byte (0x69) ICR3H Timer/Counter3 - Input Capture Register A Low Byte (0x69) ICR3L ITERCOUNTER3 - COM3A1 ICR3L ITERCOUNTER3 - COUNT										
(0xA2) UHFNUML FNUM7:0 (0xA1) UHADDR HADDR HADDR (0xA0) UHIEN HWUPE HSOFE RXRSME RSMEDE RSTE DDISCE DCONI (0x40) UHIEN HWUPI HSOFI RXRSMI RSMEDI RST DDISCI DCONI (0x9F) UHON HWUPI HSOFI RXRSMI RSMEDI RST DDISCI DCONI (0x9C) OCR3CL Timer/Counter3 - Output Compare Register C High Byte RESUME RESET SOFE (0x9B) OCR3BH Timer/Counter3 - Output Compare Register A High Byte (0x90) OCR3AL Timer/Counter3 - Output Compare Register A High Byte (0x97) ICR3L Timer/Counter3 - Output Compare Register A High Byte (0x97) ICR3L Timer/Counter3 - Output Compare Register A High Byte (0x97) ICR3L Timer/Counter3 - Output Compare Register A High Byte (0x97) ICR3L Timer/Counter3 - Output Compare Register How Byte (0x97) ICR3L Timer/Counter3 - Counter Register High Byte (0x97) ICR3L Timer/Counter3 - Counter Register High Byte (0x90) <td>FLE</td> <td></td> <td></td> <td>FLE</td> <td>EN7:0</td> <td>0</td> <td>[</td> <td>ENILIM10.9</td> <td></td> <td></td>	FLE			FLE	EN7:0	0	[ENILIM10.9		
(0xA1) UHADDR HMUPE HSOFE RXRSME RSMEDE RSTE DDISCE DCON (0xA0) UHIEN HWUPE HSOFI RXRSMI RSMEDI RSTI DDISCI DCON (0x9E) UHCON Imer Counter3 - Output Compare Register C High Byte RESUME RESET SOFE (0x9D) OCR3CH Timer/Counter3 - Output Compare Register C High Byte SOFE SOFE (0x9B) OCR3BH Timer/Counter3 - Output Compare Register B High Byte SOFE SOFE (0x9A) OCR3BL Timer/Counter3 - Output Compare Register B High Byte SOFE SOFE (0x9A) OCR3AL Timer/Counter3 - Output Compare Register A High Byte SOFE SOFE (0x9B) OCR3AL Timer/Counter3 - Output Compare Register A Low Byte SOFE SOFE SOFE (0x9B) OCR3AL Timer/Counter3 - Output Compare Register A High Byte SOFE SOFE SOFE (0x9B) ICR3L Timer/Counter3 - Output Compare Register A High Byte SOFE SOFE SOFE SOFE SOFE SOFE </td <td>ENU</td> <td></td> <td></td> <td>FNI</td> <td></td> <td>·n</td> <td></td> <td>FINUMITU.8</td> <td></td> <td></td>	ENU			FNI		·n		FINUMITU.8		
(0xA0) UHIEN HWUPE HSOFE RXRSME RSMEDE RSTE DDISCE DCONT (0x9F) UHINT HWUPI HSOFI RRSME RSTE DDISCE DCONT (0x9F) UHICON Immer/Counter3 - Output Compare Register C High Byte RESUME RESUME </td <td>1110</td> <td></td> <td></td> <td>1110</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td>	1110			1110						
(0x9F) UHINT HWUPI HSOFI RXRSMI RSMEDI RSTI DDISCI DCON (0x9E) UHCON Image: Construction of the second of the	E	1	RXRSME	1E			RSTE	DDISCE	DCONNE	
(0x9D) OCR3CH Timer/Counter3 - Output Compare Register C High Byte (0x9C) OCR3CL Timer/Counter3 - Output Compare Register C Low Byte (0x9B) OCR3BH Timer/Counter3 - Output Compare Register B High Byte (0x9A) OCR3BL Timer/Counter3 - Output Compare Register B Low Byte (0x99) OCR3AH Timer/Counter3 - Output Compare Register A Low Byte (0x97) ICR3H Timer/Counter3 - Output Compare Register A Low Byte (0x96) ICR3L Timer/Counter3 - Output Compare Register Low Byte (0x96) ICR3L Timer/Counter3 - Output Capture Register Low Byte (0x96) ICR3L Timer/Counter3 - Counter Register Low Byte (0x96) ICR3L Timer/Counter3 - Counter Register Low Byte (0x94) TCNT3L Timer/Counter3 - Counter Register Low Byte (0x92) TCCR3C FOC3A FOC3B FOC3C - - (0x91) TCCR3A COM3A1 COM3B1 COM3C1 COM3C0 WGM31 WGM32 (0x80) TCCR3A COM3A1 COM3B1 COM3C1 COM3C0 WGM31 WGM32		-			_				DCONNI	
(0x9C) OCR3CL Timer/Counter3 - Output Compare Register C Low Byte (0x9B) OCR3BH Timer/Counter3 - Output Compare Register B High Byte (0x9A) OCR3BL Timer/Counter3 - Output Compare Register B High Byte (0x9B) OCR3AH Timer/Counter3 - Output Compare Register A Low Byte (0x99) OCR3AL Timer/Counter3 - Output Compare Register A Low Byte (0x97) ICR3H Timer/Counter3 - Input Capture Register High Byte (0x96) TCNT3H Timer/Counter3 - Input Capture Register High Byte (0x95) TCNT3H Timer/Counter3 - Counter Register Low Byte (0x94) TCNT3L Timer/Counter3 - Counter Register Low Byte (0x92) TCCR3C FOC3A FOC3B FOC3C -							RESUME	RESET	SOFEN	
(0x9B) OCR3BH Timer/Counter3 - Output Compare Register B High Byte (0x9A) OCR3AL Timer/Counter3 - Output Compare Register A Low Byte (0x99) OCR3AH Timer/Counter3 - Output Compare Register A Low Byte (0x98) OCR3AL Timer/Counter3 - Output Compare Register A Low Byte (0x97) ICR3H Timer/Counter3 - Output Compare Register A Low Byte (0x96) ICR3L Timer/Counter3 - Input Capture Register Low Byte (0x96) TCNT3H Timer/Counter3 - Counter Register Low Byte (0x93) Reserved - - (0x94) TCNT3L Timer/Counter3 - Counter Register Low Byte (0x93) Reserved - - - (0x94) TCCR3A FOC3B FOC3C - - (0x90) TCCR3A COM3A1 COM3A1 COM3C0 WGM31 WGM32 (0x81) TCR3A COM3A1 COM3A0 COM3B1 COM3C0 WGM31 WGM32 (0x8D) OCR1CH - - - - - - - <td< td=""><td>out Co</td><td>ounte</td><td>inter3 - Outpu</td><td>put Co</td><td>Compa</td><td>are Register</td><td>C High Byte</td><td></td><td></td><td></td></td<>	out Co	ounte	inter3 - Outpu	put Co	Compa	are Register	C High Byte			
(0x9A) OCR3BL Timer/Counter3 - Output Compare Register B Low Byte (0x99) OCR3AH Timer/Counter3 - Output Compare Register A High Byte (0x98) OCR3AL Timer/Counter3 - Output Compare Register A Low Byte (0x97) ICR3H Timer/Counter3 - Input Capture Register A Low Byte (0x96) ICR3L Timer/Counter3 - Input Capture Register High Byte (0x96) TCNT3H Timer/Counter3 - Counter Register High Byte (0x93) Reserved - - (0x94) TCCR3Z FOC3A FOC3C (0x91) TCCR3B ICNC3 ICES3 - (0x91) TCCR3Z FOC3A FOC3C - - (0x91) TCCR3B ICNC3 ICES3 - WGM33 WGM32 CS32 CS31 CS30 (0x90) TCCR3A COM3A1 COM3A0 COM3B1 COM3C0 WGM31 WGM32 (0x8D) OCR1CH Timer/Counter1 - Output Compare Register C High Byte - - - - - - - -	put Co	Counte	unter3 - Outpu	tput C	Compa	are Register	C Low Byte			
(0x99) OCR3AH Timer/Counter3 - Output Compare Register A High Byte (0x98) OCR3AL Timer/Counter3 - Output Compare Register A Low Byte (0x97) ICR3H Timer/Counter3 - Input Capture Register Low Byte (0x96) ICR3L Timer/Counter3 - Input Capture Register Low Byte (0x95) TCNT3H Timer/Counter3 - Counter Register Low Byte (0x94) TCNT3L Timer/Counter3 - Counter Register Low Byte (0x93) Reserved - - - (0x94) TCNT3L Timer/Counter3 - Counter Register Low Byte (0x93) Reserved - - - - (0x94) TCCR3A FOC3A FOC3C - - - (0x90) TCCR3A COM3A0 COM3A1 COM3A0 COM3A1 COM3A0 (0x85) Reserved - - - - - (0x86) OCR1CH Timer/Counter1 - Output Compare Register C Low Byte - - - (0x81) OCR1CH Timer/Counter1 - Output Compare Register C Low Byte - </td <td></td> <td></td> <td></td> <td></td> <td><u> </u></td> <td>÷</td> <td>÷ ;</td> <td></td> <td></td> <td></td>					<u> </u>	÷	÷ ;			
(0x88) OCR3AL Timer/Counter3 - Output Compare Register A Low Byte (0x97) ICR3H Timer/Counter3 - Input Capture Register High Byte (0x96) ICR3L Timer/Counter3 - Input Capture Register Low Byte (0x95) TCNT3H Timer/Counter3 - Counter Register Low Byte (0x94) TCCNT3L Timer/Counter3 - Counter Register Low Byte (0x92) TCCR3C FOC3A FOC3B FOC3C -										
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(0x96) ICR3L Timer/Counter3 - Input Capture Register Low Byte (0x95) TCNT3H Timer/Counter3 - Counter Register High Byte (0x94) TCNT3L Timer/Counter3 - Counter Register Low Byte (0x93) Reserved - - - - (0x91) TCCR3C FOC3A FOC3B FOC3C -						÷				
(0x95) TCNT3H Timer/Counter3 - Counter Register High Byte (0x94) TCNT3L Timer/Counter3 - Counter Register Low Byte (0x93) Reserved - - - (0x92) TCCR3C FOC3A FOC3B FOC3C - - (0x91) TCCR3B ICNC3 ICES3 - WGM33 WGM32 CS32 CS31 CS33 (0x90) TCCR3A COM3A1 COM3A0 COM3B1 COM3B0 COM3C1 COM3C0 WGM31 WGM33 (0x8F) Reserved - </td <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>• •</td> <td></td> <td></td> <td></td>							• •			
(0x94) TCNT3L Timer/Counter3 - Counter Register Low Byte (0x93) Reserved - </td <td></td>										
(0x93) Reserved - <										
(0x91) TCCR3B ICNC3 ICES3 - WGM33 WGM32 CS32 CS31 CS30 (0x90) TCCR3A COM3A1 COM3A0 COM3B1 COM3B0 COM3C1 COM3C0 WGM31 WGM33 (0x8F) Reserved -						-		-	-	
(0x90) TCCR3A COM3A1 COM3A0 COM3B1 COM3B0 COM3C1 COM3C0 WGM31 WGM31 (0x8F) Reserved -			-			-	-	-	-	
(0x8F) Reserved - <	3		WGM33	3	V	WGM32	CS32	CS31	CS30	
(0x8E) Reserved - <	0		COM3B0	30	С	COM3C1	COM3C0	WGM31	WGM30	
(0x8D) OCR1CH Timer/Counter1 - Output Compare Register C High Byte (0x8C) OCR1CL Timer/Counter1 - Output Compare Register C Low Byte (0x8B) OCR1BH Timer/Counter1 - Output Compare Register B High Byte (0x8A) OCR1BL Timer/Counter1 - Output Compare Register B Low Byte (0x89) OCR1AH Timer/Counter1 - Output Compare Register A High Byte (0x88) OCR1AL Timer/Counter1 - Output Compare Register A Low Byte (0x87) ICR1H Timer/Counter1 - Output Compare Register Low Byte (0x86) ICR1L Timer/Counter1 - Input Capture Register Low Byte (0x85) TCNT1H Timer/Counter1 - Counter Register High Byte (0x84) TCNT1L Timer/Counter1 - Counter Register Low Byte (0x83) Reserved - -								-		
(0x8C) OCR1CL Timer/Counter1 - Output Compare Register C Low Byte (0x8B) OCR1BH Timer/Counter1 - Output Compare Register B High Byte (0x8A) OCR1BL Timer/Counter1 - Output Compare Register B Low Byte (0x89) OCR1AH Timer/Counter1 - Output Compare Register A High Byte (0x88) OCR1AL Timer/Counter1 - Output Compare Register A Low Byte (0x87) ICR1H Timer/Counter1 - Output Compare Register High Byte (0x86) ICR1L Timer/Counter1 - Input Capture Register Low Byte (0x85) TCNT1H Timer/Counter1 - Counter Register High Byte (0x84) TCNT1L Timer/Counter1 - Counter Register Low Byte (0x83) Reserved - -								-	-	
(0x8B) OCR1BH Timer/Counter1 - Output Compare Register B High Byte (0x8A) OCR1BL Timer/Counter1 - Output Compare Register B Low Byte (0x89) OCR1AH Timer/Counter1 - Output Compare Register A High Byte (0x88) OCR1AL Timer/Counter1 - Output Compare Register A Low Byte (0x87) ICR1H Timer/Counter1 - Output Compare Register High Byte (0x86) ICR1L Timer/Counter1 - Input Capture Register Low Byte (0x85) TCNT1H Timer/Counter1 - Counter Register High Byte (0x84) TCNT1L Timer/Counter1 - Counter Register Low Byte (0x83) Reserved -										
(0x8A) OCR1BL Timer/Counter1 - Output Compare Register B Low Byte (0x89) OCR1AH Timer/Counter1 - Output Compare Register A High Byte (0x88) OCR1AL Timer/Counter1 - Output Compare Register A Low Byte (0x87) ICR1H Timer/Counter1 - Input Capture Register High Byte (0x86) ICR1L Timer/Counter1 - Input Capture Register Low Byte (0x85) TCNT1H Timer/Counter1 - Counter Register High Byte (0x84) TCNT1L Timer/Counter1 - Counter Register Low Byte (0x83) Reserved -						0	,			
(0x89) OCR1AH Timer/Counter1 - Output Compare Register A High Byte (0x88) OCR1AL Timer/Counter1 - Output Compare Register A Low Byte (0x87) ICR1H Timer/Counter1 - Input Capture Register High Byte (0x86) ICR1L Timer/Counter1 - Input Capture Register Low Byte (0x85) TCNT1H Timer/Counter1 - Counter Register High Byte (0x84) TCNT1L Timer/Counter1 - Counter Register Low Byte (0x83) Reserved -					-		• •			
(0x88) OCR1AL Timer/Counter1 - Output Compare Register A Low Byte (0x87) ICR1H Timer/Counter1 - Input Capture Register High Byte (0x86) ICR1L Timer/Counter1 - Input Capture Register Low Byte (0x85) TCNT1H Timer/Counter1 - Counter Register High Byte (0x84) TCNT1L Timer/Counter1 - Counter Register Low Byte (0x83) Reserved - -			-	-		-	-			
(0x87) ICR1H Timer/Counter1 - Input Capture Register High Byte (0x86) ICR1L Timer/Counter1 - Input Capture Register Low Byte (0x85) TCNT1H Timer/Counter1 - Counter Register High Byte (0x84) TCNT1L Timer/Counter1 - Counter Register Low Byte (0x83) Reserved - -						÷	÷ ;			
ICR1L Timer/Counter1 - Input Capture Register Low Byte (0x85) TCNT1H Timer/Counter1 - Counter Register High Byte (0x84) TCNT1L Timer/Counter1 - Counter Register Low Byte (0x83) Reserved - - - -										
(0x85) TCNT1H Timer/Counter1 - Counter Register High Byte (0x84) TCNT1L Timer/Counter1 - Counter Register Low Byte (0x83) Reserved - - - -						-				
(0x83) Reserved	- Cour	mer/C	er/Counter1 - 0	- Cou	unter I	Register Hig	h Byte			
	- Cou	mer/C	er/Counter1 - (- Cou	unter	Register Lov	w Byte			
(0x82) TCCR1C FOC1A FOC1B FOC1C						-				
			-			-	-	-	-	
		_			-				CS10	
	0	-	COM1B0	30	C	COM1C1	COM1C0		WGM10	
	, -	-	-	-		-	-		AIN0D ADC0D	
(0x7E) DIDR0 ADC7D ADC6D ADC5D ADC4D ADC3D ADC2D ADC1D ADC00 (0x7D) - <	,			,	- '					





Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page	
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0		
(0x7B)	ADCSRB	ADHSM	ACME	-	-	-	ADTS2	ADTS1	ADTS0		
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0		
(0x79)	ADCH		ADC Data Register High byte								
(0x78)	ADCL		1	1	ADC Data Re	egister Low byte	-		1		
(0x77)	Reserved	-	-	-	-	-	-	-	-		
(0x76)	Reserved	-	-	-	-	-	-	-	-		
(0x75)	XMCRB	XMBK	-	-	-	-	XMM2	XMM1	XMM0		
(0x74)	XMCRA	SRE	SRL2	SRL1	SRL0	SRW11	SRW10	SRW01	SRW00		
(0x73)	Reserved	-	-	-	-	-	-	-	-		
(0x72)	Reserved	-	-	-	-	-	-	-	-		
(0x71)	TIMSK3	-	-	ICIE3	-	OCIE3C	OCIE3B	OCIE3A	TOIE3		
(0x70)	TIMSK2	-	-	-	-	-	OCIE2B	OCIE2A	TOIE2		
(0x6F)	TIMSK1	-	-	ICIE1	-	OCIE1C	OCIE1B	OCIE1A	TOIE1		
(0x6E)	TIMSK0	-	-	-	-	-	OCIE0B	OCIE0A	TOIE0		
(0x6D) (0x6C)	Reserved Reserved	-	-	-	-	-	-	-	-		
(0x6C) (0x6B)	PCMSK0	PCINT7	- PCINT6	- PCINT5	- PCINT4	- PCINT3	PCINT2	PCINT1	PCINT0		
(0x6A)	EICRB	ISC71	ISC70	ISC61	ISC60	ISC51	ISC50	ISC41	ISC40		
(0x69)	EICRA	ISC31	ISC30	ISC01	ISC00	ISC11	ISC30	ISC01	ISC00		
(0x68)	PCICR	-	-	-	-	-	-	-	PCIE0		
(0x68) (0x67)	Reserved	-	-	-	-	-	-	-	-		
(0x66)	OSCCAL			_	Oscillator Cal	ibration Register					
(0x65)	PRR1	PRUSB	-	-	-	PRTIM3	-	-	PRUSART1		
(0x64)	PRR0	PRTWI	PRTIM2	PRTIM0	-	PRTIM1	PRSPI	-	PRADC		
(0x63)	Reserved	-	-	-	-	-	-	-	-		
(0x62)	Reserved	-	-	-	-	-	-	-	-		
(0x61)	CLKPR	CLKPCE	-	-	-	CLKPS3	CLKPS2	CLKPS1	CLKPS0		
(0x60)	WDTCSR	WDIF	WDIE	WDP3	WDCE	WDE	WDP2	WDP1	WDP0		
0x3F (0x5F)	SREG	1	т	Н	S	V	N	Z	С		
0x3E (0x5E)	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8		
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0		
0x3C (0x5C)	Reserved	-	-	-	-	-	-	-	-		
0x3B (0x5B)	RAMPZ	-	-	-	-	-	-	RAMPZ1	RAMPZ0		
0x3A (0x5A)	Reserved	-	-	-	-	-	-	-	-		
0x39 (0x59)	Reserved	-	-	-	-	-	-	-	-		
0x38 (0x58)	Reserved	-	-	-	-	-	-	-	-		
0x37 (0x57)	SPMCSR	SPMIE	RWWSB	SIGRD	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN		
0x36 (0x56)	Reserved	-	-	-	-	-	-	-	-		
0x35 (0x55)	MCUCR	JTD	-	-	PUD	-	-	IVSEL	IVCE		
0x34 (0x54)	MCUSR	-	-	-	JTRF	WDRF	BORF	EXTRF	PORF		
0x33 (0x53)	SMCR	-	-	-	-	SM2	SM1	SM0	SE		
0x32 (0x52)	Reserved	-	-	-	-	-	-	-	-		
0x31 (0x51)	OCDR/	OCDR7	OCDR6	OCDR5	OCDR4	OCDR3	OCDR2	OCDR1	OCDR0		
	MONDR					ata Register			1		
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0		
0x2F (0x4F)	Reserved	-	-	-	-	-	-	-	-		
0x2E (0x4E)	SPDR		14/001			ta Register			ODIOY		
0x2D (0x4D)	SPSR	SPIF	WCOL	-	-	-		-	SPI2X		
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR Conorol Burno	CPOL	CPHA	SPR1	SPR0		
0x2B (0x4B)	GPIOR2 GPIOR1					se I/O Register 2 se I/O Register 1					
0x2A (0x4A) 0x29 (0x49)	PLLCSR	-	-	-	PLLP2	PLLP1	PLLP0	PLLE	PLOCK		
0x29 (0x49) 0x28 (0x48)	OCR0B	-	-			out Compare Reg		FLLE	FLOOK		
0x28 (0x48) 0x27 (0x47)	OCR0B OCR0A					out Compare Reg					
0x27 (0x47) 0x26 (0x46)	TCNT0			1111		unter0 (8 Bit)					
0x25 (0x45)	TCCR0B	FOC0A	FOC0B	-	-	WGM02	CS02	CS01	CS00		
0x24 (0x44)	TCCR0A	COM0A1	COM0A0	COM0B1	COM0B0	-	-	WGM01	WGM00		
0x23 (0x43)	GTCCR	TSM	-	-	-	-	-	PSRASY	PSRSYNC		
0x22 (0x42)	EEARH	-	-	-	-		EPROM Addres	s Register High B			
0x21 (0x41)	EEARL				EEPROM Addres	s Register Low B			,		
0x20 (0x40)	EEDR	1				Data Register					
0x1F (0x3F)	EECR	-	-	EEPM1	EEPMO	EERIE	EEMPE	EEPE	EERE		
0x1E (0x3E)	GPIOR0					se I/O Register 0					
0x1D (0x3D)	EIMSK	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0		
0x1C (0x3C)	EIFR	INTF7	INTF6	INTF5	INTF4	INTF3	INTF2	INTF1	INTF0		
- (· · · ·	· · · ·		· · ·	·	· ·		·	· · ·		



Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x1B (0x3B)	PCIFR	-	-	-	-	-	-	-	PCIF0	
0x1A (0x3A)	Reserved	-	-	-	-	-	-	-	-	
0x19 (0x39)	Reserved	-	-	-	-	-	-	-	-	
0x18 (0x38)	TIFR3	-	-	ICF3	-	OCF3C	OCF3B	OCF3A	TOV3	
0x17 (0x37)	TIFR2	-	-	-	-	-	OCF2B	OCF2A	TOV2	
0x16 (0x36)	TIFR1	-	-	ICF1	-	OCF1C	OCF1B	OCF1A	TOV1	
0x15 (0x35)	TIFR0	-	-	-	-	-	OCF0B	OCF0A	TOV0	
0x14 (0x34)	Reserved	-	-	-	-	-	-	-	-	
0x13 (0x33)	Reserved	-	-	-	-	-	-	-	-	
0x12 (0x32)	Reserved	-	-	-	-	-	-	-	-	
0x11 (0x31)	PORTF	PORTF7	PORTF6	PORTF5	PORTF4	PORTF3	PORTF2	PORTF1	PORTF0	
0x10 (0x30)	DDRF	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	
0x0F (0x2F)	PINF	PINF7	PINF6	PINF5	PINF4	PINF3	PINF2	PINF1	PINF0	
0x0E (0x2E)	PORTE	PORTE7	PORTE6	PORTE5	PORTE4	PORTE3	PORTE2	PORTE1	PORTE0	
0x0D (0x2D)	DDRE	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	DDE1	DDE0	
0x0C (0x2C)	PINE	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0	
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	

Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. I/O registers within the address range \$00 - \$1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.

3. Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers 0x00 to 0x1F only.

4. When using the I/O specific commands IN and OUT, the I/O addresses \$00 - \$3F must be used. When addressing I/O registers as data space using LD and ST instructions, \$20 must be added to these addresses. The ATmega32U6/AT90USB64/128 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from \$60 - \$1FF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.





5. Instruction Set Summary

Vinemonics	Operands	Description	Operation	Flags	#Clock
	ARITHME	TIC AND LOGIC INSTRUCTIONS			
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.		Z,C,N,V,H	1
SBIW AND	Rdl,K Rd, Rr	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$ $Rd \leftarrow Rd \bullet Rr$	Z,C,N,V,S Z,N,V	2
AND	Rd, Ki	Logical AND Registers Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \lor R$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow 0xFF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \gets Rd \lor K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (0xFF - K)$	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
MUL	Rd, Rr	Multiply Unsigned	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULS	Rd, Rr	Multiply Signed	$R1:R0 \leftarrow Rd \times Rr$	Z,C	2
MULSU	Rd, Rr Rd, Rr	Multiply Signed with Unsigned	$\frac{R1:R0 \leftarrow Rd \times Rr}{R1:R0 \leftarrow (Rd \times Rr) << 1}$	Z,C	2
FMUL FMULS	Rd, Rr	Fractional Multiply Unsigned Fractional Multiply Signed	$R1:R0 \leftarrow (Rd x Rr) << 1$	Z,C Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	$R1:R0 \leftarrow (Rd \times Rr) << 1$	Z,C	2
T MICEOU		RANCH INSTRUCTIONS		2,0	
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
EIJMP		Extended Indirect Jump to (Z)	PC ←(EIND:Z)	None	2
JMP	k	Direct Jump	$PC \leftarrow k$	None	3
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	4
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	4
EICALL		Extended Indirect Call to (Z)	PC ←(EIND:Z)	None	4
CALL	k	Direct Subroutine Call	$PC \leftarrow k$	None	5
RET		Subroutine Return		None	5
RETI	212	Interrupt Return		1	5
CPSE CP	Rd,Rr	Compare, Skip if Equal Compare	if $(Rd = Rr) PC \leftarrow PC + 2 \text{ or } 3$ Rd – Rr	None Z, N,V,C,H	1/2/3 1
CPC	Rd,Rr Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC \leftarrow PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if $(Rr(b)=1) PC \leftarrow PC + 2 or 3$	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC \leftarrow PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC \leftarrow PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC+k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC \leftarrow PC + k + 1	None	1/2
	k	Branch if Not Equal	if (Z = 0) then PC \leftarrow PC + k + 1	None	1/2
BRNE		Branch if Carry Set	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
BRNE BRCS	k		if (C = 0) then PC \leftarrow PC + k + 1	None	1/2
BRNE BRCS BRCC	k	Branch if Carry Cleared			1/2
BRNE BRCS BRCC BRSH	k k	Branch if Same or Higher	if (C = 0) then PC \leftarrow PC + k + 1	None	
BRNE BRCS BRCC BRSH BRLO	k k k	Branch if Same or Higher Branch if Lower	if (C = 1) then PC \leftarrow PC + k + 1	None	1/2
BRNE BRCS BRCC BRSH BRLO BRMI	k k k k	Branch if Same or Higher Branch if Lower Branch if Minus	$\begin{array}{c} \text{if } (C=1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \text{if } (N=1) \text{ then } PC \leftarrow PC + k + 1 \end{array}$	None None	1/2
BRNE BRCS BRCC BRSH BRLO BRMI BRPL	k k k k k	Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus	$\begin{array}{c} \mbox{if } (C=1) \mbox{ then } PC \leftarrow PC + k + 1 \\ \mbox{if } (N=1) \mbox{ then } PC \leftarrow PC + k + 1 \\ \mbox{if } (N=0) \mbox{ then } PC \leftarrow PC + k + 1 \end{array}$	None None None	1/2 1/2
BRNE BRCS BRCC BRSH BRLO BRMI BRPL BRGE	k k k k k k	Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus Branch if Greater or Equal, Signed	$\begin{array}{l} \mbox{if } (C=1) \mbox{ then } PC \leftarrow PC + k + 1 \\ \mbox{if } (N=1) \mbox{ then } PC \leftarrow PC + k + 1 \\ \mbox{if } (N=0) \mbox{ then } PC \leftarrow PC + k + 1 \\ \mbox{if } (N \oplus V=0) \mbox{ then } PC \leftarrow PC + k + 1 \end{array}$	None None None None	1/2 1/2 1/2
BRNE BRCS BRCC BRSH BRLO BRMI BRPL BRGE BRLT	k k k k k k k	Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus Branch if Greater or Equal, Signed Branch if Less Than Zero, Signed	$\begin{array}{c} \text{if } (C=1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \text{if } (N=1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \text{if } (N=0) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \text{if } (N \oplus V=0) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \text{if } (N \oplus V=1) \text{ then } PC \leftarrow PC + k + 1 \end{array}$	None None None None None	1/2 1/2 1/2 1/2
BRNE BRCS BRCC BRSH BRLO BRMI BRPL BRGE BRLT BRHS	k k k k k k k k	Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus Branch if Greater or Equal, Signed Branch if Less Than Zero, Signed Branch if Half Carry Flag Set	$\begin{array}{c} \text{if } (C=1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \text{if } (N=1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \text{if } (N=0) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \text{if } (N \oplus V=0) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \text{if } (N \oplus V=1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \\ \text{if } (H=1) \text{ then } PC \leftarrow PC + k + 1 \end{array}$	None None None None None None	1/2 1/2 1/2 1/2 1/2
BRNE BRCS BRCC BRSH BRLO BRMI BRPL BRGE BRLT BRHS BRHC	k k k k k k k k k	Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus Branch if Greater or Equal, Signed Branch if Less Than Zero, Signed Branch if Half Carry Flag Set Branch if Half Carry Flag Cleared	$\begin{array}{c} \text{if } (C=1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \text{if } (N=1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \text{if } (N=0) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \text{if } (N \oplus V = 0) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \text{if } (N \oplus V = 1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \\ \text{if } (H=1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \\ \text{if } (H=0) \text{ then } PC \leftarrow PC + k + 1 \end{array}$	None None None None None None None	1/2 1/2 1/2 1/2 1/2 1/2
BRNE BRCS BRCC BRSH BRLO BRMI BRPL BRGE BRLT BRHS	k k k k k k k k	Branch if Same or Higher Branch if Lower Branch if Minus Branch if Plus Branch if Greater or Equal, Signed Branch if Less Than Zero, Signed Branch if Half Carry Flag Set	$\begin{array}{c} \text{if } (C=1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \text{if } (N=1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \text{if } (N=0) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \text{if } (N \oplus V=0) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \text{if } (N \oplus V=1) \text{ then } PC \leftarrow PC + k + 1 \\ \\ \\ \\ \text{if } (H=1) \text{ then } PC \leftarrow PC + k + 1 \end{array}$	None None None None None None	1/2 1/2 1/2 1/2 1/2

	Operands	Description	Operation	Flags	#Clocks	
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC \leftarrow PC + k + 1	None	1/2	
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC \leftarrow PC + k + 1	None	1/2	
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC \leftarrow PC + k + 1	None	1/2	
	BIT AN	D BIT-TEST INSTRUCTIONS		-	-	
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2	
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2	
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1	
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	1	
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1	
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1	
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=06$	Z,C,N,V	1	
SWAP	Rd	Swap Nibbles	Rd(30)←Rd(74),Rd(74)←Rd(30)	None	1	
BSET	S	Flag Set	SREG(s) ← 1	SREG(s)	1	
BCLR	S	Flag Clear	$SREG(s) \leftarrow 0$	SREG(s)	1	
BST	Rr, b	Bit Store from Register to T	$T \leftarrow Rr(b)$	Т	1	
BLD	Rd, b	Bit load from T to Register	$Rd(b) \leftarrow T$	None	1	
SEC		Set Carry	C ← 1	С	1	
CLC		Clear Carry	C ← 0	С	1	
SEN		Set Negative Flag	N ← 1	N	1	
CLN		Clear Negative Flag	N ← 0	N	1	
SEZ		Set Zero Flag	Z ← 1	Z	1	
CLZ		Clear Zero Flag	Z ~ 0	Z	1	
SEI		Global Interrupt Enable	← 1	1	1	
CLI		Global Interrupt Disable	l ← 0	1	1	
SES		Set Signed Test Flag	S ← 1	S	1	
CLS		Clear Signed Test Flag	<u>S</u> ← 0	S	1	
SEV		Set Twos Complement Overflow.	V ← 1	V	1	
CLV		Clear Twos Complement Overflow	V ← 0	V	1	
SET		Set T in SREG	<u> </u>	Т	1	
CLT		Clear T in SREG	T ← 0	Т	1	
SEH CLH		Set Half Carry Flag in SREG	H ← 1	Н	1	
CLH	DATA	Clear Half Carry Flag in SREG	H ← 0	п	I	
MOV		TRANSFER INSTRUCTIONS		Nana	4	
MOV	Rd, Rr	Move Between Registers	$Rd \leftarrow Rr$ $Rd+1:Rd \leftarrow Rr+1:Rr$	None	1	
MOVW	Rd, Rr	Copy Register Word		None	1	
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1 2	
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2	
LD LD	Rd, X+ Rd, - X	Load Indirect and Post-Inc. Load Indirect and Pre-Dec.	$Rd \leftarrow (X), X \leftarrow X + 1$ $X \leftarrow X - 1, Rd \leftarrow (X)$	None	2	
LD	Rd, Y	Load Indirect and Pre-Dec.	$\begin{array}{c} \land \leftarrow \land -1, \forall u \leftarrow (\land) \\ Rd \leftarrow (Y) \end{array}$	None None	2	
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2	
LD	Rd, 14	Load Indirect and Post-Inc.	$\begin{array}{c} Rd \leftarrow (f), \; f \leftarrow f + f \\ Y \leftarrow Y - 1, \; Rd \leftarrow (Y) \end{array}$	None	2	
LDD		Load Indirect with Displacement	$Rd \leftarrow (Y + q)$		2	
LDD	Rd,Y+q Rd, Z	Load Indirect With Displacement	$\frac{Rd \leftarrow (f + q)}{Rd \leftarrow (Z)}$	None None	2	
LD		Load Indirect	· /		2	
LD	Rd, Z+ Rd, -Z	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z+1$ $Z \leftarrow Z - 1, Rd \leftarrow (Z)$	None None	2	
LD	Rd, Z+q	Load Indirect and Pre-Dec.	$2 \leftarrow 2 - 1, Rd \leftarrow (2)$ Rd $\leftarrow (Z + q)$	None	2	
LDD	Rd, Z+q Rd, k	Load Direct from SRAM	$\frac{Rd \leftarrow (Z + q)}{Rd \leftarrow (k)}$	None	2	
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2	
ST	X, RI X+, Rr	Store Indirect Store Indirect	$(X) \leftarrow Ri$ $(X) \leftarrow Rr, X \leftarrow X + 1$	None	2	
ST	- X, Rr	Store Indirect and Post-Inc. Store Indirect and Pre-Dec.	$(X) \leftarrow Rr, X \leftarrow X + 1$ $X \leftarrow X - 1, (X) \leftarrow Rr$	None	2	
ST	- x, Rr Y, Rr	Store Indirect and Pre-Dec. Store Indirect		None	2	
	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr$ $(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2	
	+, Rr - Y, Rr	Store Indirect and Post-Inc. Store Indirect and Pre-Dec.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$ $Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2	
ST ST	~ 1, IXI		$(Y+q) \leftarrow Rr$	None	2	
ST	Via Pr	Store Indirect with Displacement				
ST STD	Y+q,Rr	Store Indirect with Displacement				
ST STD ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2	
ST STD ST ST	Z, Rr Z+, Rr	Store Indirect Store Indirect and Post-Inc.	$(Z) \leftarrow Rr$ $(Z) \leftarrow Rr, Z \leftarrow Z + 1$	None None	2 2	
ST STD ST ST ST	Z, Rr Z+, Rr -Z, Rr	Store Indirect Store Indirect and Post-Inc. Store Indirect and Pre-Dec.	$(Z) \leftarrow Rr$ $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ $Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None None None	2 2 2	
ST STD ST ST ST STD	Z, Rr Z+, Rr -Z, Rr Z+q,Rr	Store Indirect Store Indirect and Post-Inc. Store Indirect and Pre-Dec. Store Indirect with Displacement	$(Z) \leftarrow Rr$ $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ $(Z + q) \leftarrow Rr$	None None None None	2 2 2 2 2	
ST STD ST ST ST STD STS	Z, Rr Z+, Rr -Z, Rr	Store Indirect Store Indirect and Post-Inc. Store Indirect and Pre-Dec. Store Indirect with Displacement Store Direct to SRAM	$(Z) \leftarrow Rr$ $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ $(Z + q) \leftarrow Rr$ $(k) \leftarrow Rr$	None None None None None	2 2 2 2 2 2	
ST STD ST ST ST STD STS LPM	Z, Rr Z+, Rr -Z, Rr Z+q,Rr k, Rr	Store Indirect Store Indirect and Post-Inc. Store Indirect and Pre-Dec. Store Indirect with Displacement Store Direct to SRAM Load Program Memory	$(Z) \leftarrow Rr$ $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ $(Z + q) \leftarrow Rr$ $(k) \leftarrow Rr$ $R0 \leftarrow (Z)$	None None None None None None	2 2 2 2 2 2 2 3	
ST STD ST ST STD STD STS LPM LPM	Z, Rr Z+, Rr -Z, Rr Z+q,Rr k, Rr Rd, Z	Store Indirect Store Indirect and Post-Inc. Store Indirect and Pre-Dec. Store Indirect with Displacement Store Direct to SRAM Load Program Memory Load Program Memory	$(Z) \leftarrow Rr$ $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ $(Z + q) \leftarrow Rr$ $(k) \leftarrow Rr$ $R0 \leftarrow (Z)$ $Rd \leftarrow (Z)$	None None None None None None	2 2 2 2 2 3 3 3	
ST STD ST ST STD STS LPM LPM LPM	Z, Rr Z+, Rr -Z, Rr Z+q,Rr k, Rr	Store Indirect Store Indirect and Post-Inc. Store Indirect and Pre-Dec. Store Indirect with Displacement Store Direct to SRAM Load Program Memory Load Program Memory Load Program Memory Load Program Memory	$(Z) \leftarrow Rr$ $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ $(Z + q) \leftarrow Rr$ $(k) \leftarrow Rr$ $R0 \leftarrow (Z)$ $Rd \leftarrow (Z)$ $Rd \leftarrow (Z), Z \leftarrow Z + 1$	None None None None None None None	2 2 2 2 3 3 3 3 3	
ST STD ST ST ST STD STS LPM LPM	Z, Rr Z+, Rr -Z, Rr Z+q,Rr k, Rr Rd, Z	Store Indirect Store Indirect and Post-Inc. Store Indirect and Pre-Dec. Store Indirect with Displacement Store Direct to SRAM Load Program Memory Load Program Memory	$(Z) \leftarrow Rr$ $(Z) \leftarrow Rr, Z \leftarrow Z + 1$ $Z \leftarrow Z - 1, (Z) \leftarrow Rr$ $(Z + q) \leftarrow Rr$ $(k) \leftarrow Rr$ $R0 \leftarrow (Z)$ $Rd \leftarrow (Z)$	None None None None None None	2 2 2 2 2 3 3 3	





Mnemonics	Operands	Description	Operation	Flags	#Clocks
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	$Rd \leftarrow P$	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	$STACK \leftarrow Rr$	None	2
POP	Rd	Pop Register from Stack	$Rd \leftarrow STACK$	None	2
	MCU	CONTROL INSTRUCTIONS			
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

6. Ordering Information

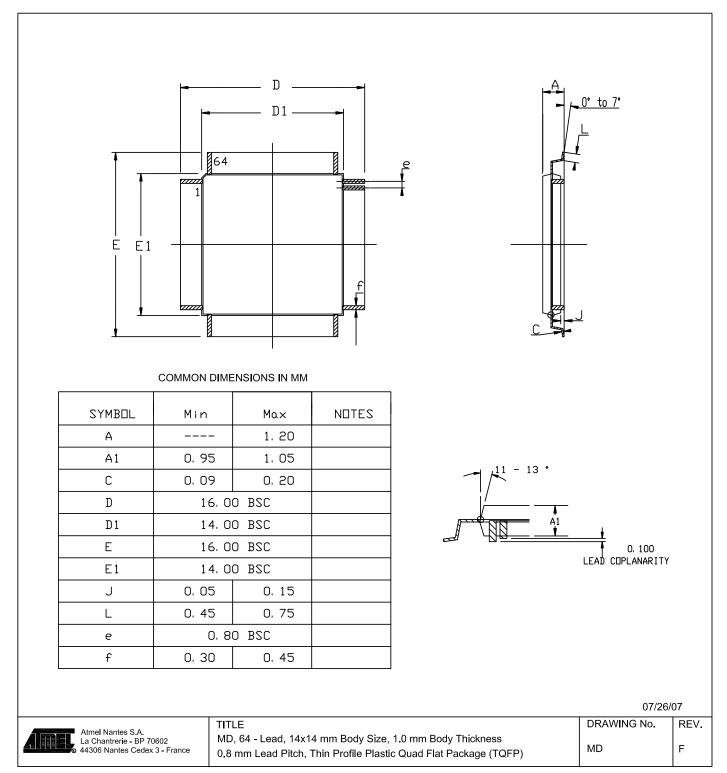
	Table 6-1.	Poss	ible Order Entrie	S		
Ordering Code	USB interface	Speed (MHz)	Power Supply (V)	Package	Operation Range	Product Marking
AT90USB1287-16AU	OTG	8-16	2.7 - 5.5	MD	Industrial (-40° to +85°C) Green	90USB1287-16AU
AT90USB1287-16MU	OTG	8-16	2.7 - 5.5	PS	Industrial (-40° to +85°C) Green	90USB1287-16MU
AT90USB1286-16MU	Device only	8-16	2.7 - 5.5	PS	Industrial (-40° to +85°C) Green	90USB1286-16MU
AT90USB647-16AU	OTG	8-16	2.7 - 5.5	MD	Industrial (-40° to +85°C) Green	90USB647-16AU
AT90USB647-16MU	OTG	8-16	2.7 - 5.5	PS	Industrial (-40° to +85°C) Green	90USB647-16MU
AT90USB646-16MU	Device only	8-16	2.7 - 5.5	PS	Industrial (-40° to +85°C) Green	90USB646-16MU

MD	64 - Lead, 14x14 mm Body Size, 1.0mm Body Thickness 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)
PS	64 - Lead, 9x9 mm Body Size, 0.50mm Pitch Quad Flat No Lead Package (QFN)





6.1 TQFP64



NOTES: STANDARD NOTES FOR PQFP/VQFP/TQFP/DQFP

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. - 1982.

2. "D1 AND E1" DIMENSIONS DO NOT INCLUDE MOLD PROTUSIONS MOLD PROTUSIONS SHALL NOT EXCEED 0.25 mm (0.010 INCH) . THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE BY AS MUCH AS 0.15 mm.

3. DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXISTS PLASTIC BODY AT BOTTOM OF PARTING LINE.

4. DATUM "A" AND "D" TO BE DETERMINED AT DATUM PLANE H.

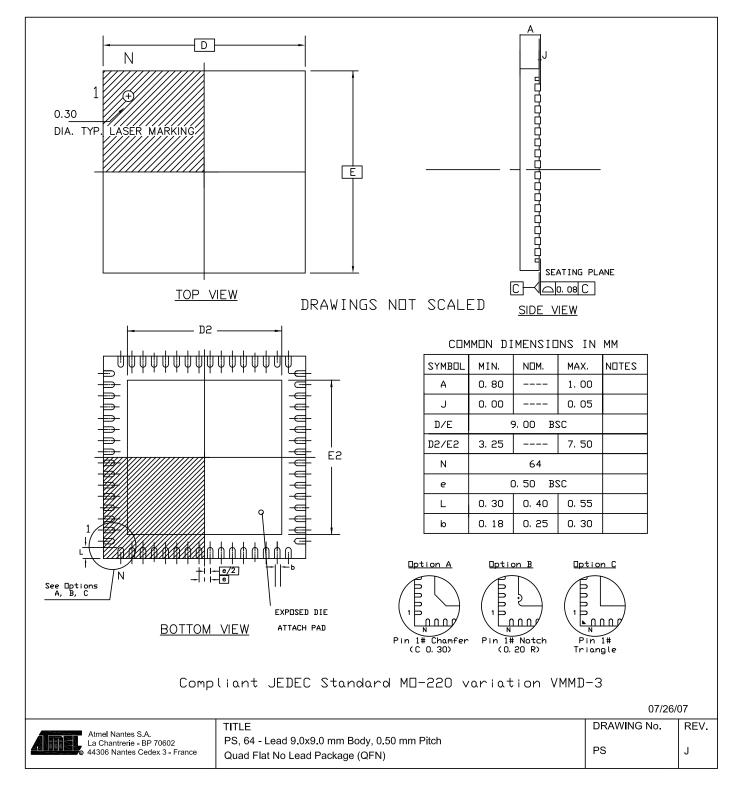
5. DIMENSION "f" DOES NOT INCLUDE DAMBAR PROTUSION ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 mm/.003" TOTAL EXCESS OF THE "f" DIMENSION AT MAXIMUM MATERIAL CONDITION.

DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.





6.2 QFN64



NOTES: QFN STANDARD NOTES

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. - 1994.

2. DIMENSION & APPLIES TO METALLIZED TERMINAL AND IS MEASURED

BETWEEN 0.15 AND 0.30 mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION & SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

3. MAX. PACKAGE WARPAGE IS 0.05mm.

4. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.

5. PIN #1 ID ON TOP WILL BE LASER MARKED.

6. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220.

7. A MAXIMUM 0.15mm PULL BACK (L1) MAY BE PRESENT.

L MINUS L1 TO BE EQUAL TO OR GREATER THAN 0.30 mm

8. THE TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER BE EITHER A MOLD OR MARKED FEATURE





7. Errata

8. AT90USB1287/6 Errata.

8.1 AT90USB1287/6 Errata History

Silicon Release	90USB1286-16MU	90USB1287-16AU	90USB1287-16MU		
First Release Date Code up to 0648		Date Code up to 0714 and lots 0735 6H2726*	Date Code up to 0701		
Second Release Date Code from 0709 to 0801 except lots 0801 7H5103*		from Date Code 0722 to 0806 except lots 0735 6H2726*	Date Code from 0714 to 0810 except lots 0748 7H5103*		
Third Release	Lots 0801 7H5103* and Date Code from 0814	Date Code from 0814	Lots 0748 7H5103* and Date Code from 0814		

Note '*' means a blank or any alphanumeric string

8.2 AT90USB1287/6 First Release

- Incorrect CPU behavior for VBUSTI and IDTI interrupts routines
- USB Eye Diagram violation in low-speed mode
- Transient perturbation in USB suspend mode generates over consumption
- VBUS Session valid threshold voltage
- USB signal rate
- VBUS residual level
- Spike on TWI pins when TWI is enabled
- High current consumption in sleep mode
- Async timer interrupt wake up from sleep generate multiple interrupts

9. Incorrect CPU behavior for VBUSTI and IDTI interrupts routines

The CPU core may incorrectly execute the interrupt vector related to the VBUSTI and IDTI interrupt flags.

Problem fix/workaround

Do not enable these interrupts, firmware must process these USB events by polling VBUSTI and IDTI flags.

8. USB Eye Diagram violation in low-speed mode

The low to high transition of D- violates the USB eye diagram specification when transmitting with low-speed signaling.

Problem fix/workaround

None.

7. Transient perturbation in USB suspend mode generates overconsumption

In device mode and when the USB is suspended, transient perturbation received on the USB lines generates a wake up state. However the idle state following the perturbation does

²² ATmega32U6/AT90USB64/128

not set the SUSPI bit anymore. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300µA extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

6. VBUS Session valid threshold voltage

The VSession valid threshold voltage is internally connected to VBus_Valid (4.4V approx.). That causes the device to attach to the bus only when Vbus is greater than VBusValid instead of V_Session Valid. Thus if VBUS is lower than 4.4V, the device is detached.

Problem fix/workaround

According to the USB power drop budget, this may require connecting the device toa root hub or a self-powered hub.

5. UBS signal rate

The average USB signal rate may sometime be measured out of the USB specifications $(12MHz \pm 30kHz)$ with short frames. When measured on a long period, the average signal rate value complies with the specifications. This bit rate deviation does not generates communication or functional errors.

Problem fix/workaround

None.

4. VBUS residual level

In USB device and host mode, once a 5V level has been detected to the VBUS pad, a residual level (about 3V) can be measured on the VBUS pin.

Problem fix/workaround

None.

3. Spike on TWI pins when TWI is enabled

100 ns negative spike occurs on SDA and SCL pins when TWI is enabled.

Problem Fix/workaround

No known workaround, enable ATmega32U6/AT90USB64/128 TWI first versus the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem Fix/workaround

Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

1. Asynchronous timer interrupt wake up from sleep generates multiple interrupts





If the CPU core is in sleep and wakes-up from an asynchronous timer interrupt and then go back in sleep again it may wake up multiple times.

Problem Fix/workaround

A software workaround is to wait with performing the sleep instruction until TCNT2>OCR2+1.

8.3 AT90USB1287/6 Second Release

- Incorrect CPU behavior for VBUSTI and IDTI interrupts routines
- USB Eye Diagram violation in low-speed mode
- Transient perturbation in USB suspend mode generates over consumption
- VBUS Session valid threshold voltage
- Spike on TWI pins when TWI is enabled
- High current consumption in sleep mode
- Async timer interrupt wake up from sleep generate multiple interrupts

7. Incorrect CPU behavior for VBUSTI and IDTI interrupts routines

The CPU core may incorrectly execute the interrupt vector related to the VBUSTI and IDTI interrupt flags.

Problem fix/workaround

Do not enable these interrupts, firmware must process these USB events by polling VBUSTI and IDTI flags.

6. USB Eye Diagram violation in low-speed mode

The low to high transition of D- violates the USB eye diagram specification when transmitting with low-speed signaling.

Problem fix/workaround

None.

5. Transient perturbation in USB suspend mode generates overconsumption

In device mode and when the USB is suspended, transient perturbation received on the USB lines generates a wake up state. However the idle state following the perturbation does not set the SUSPI bit anymore. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300µA extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

4. VBUS Session valid threshold voltage

The VSession valid threshold voltage is internally connected to VBus_Valid (4.4V approx.). That causes the device to attach to the bus only when Vbus is greater than VBusValid instead of V_Session Valid. Thus if VBUS is lower than 4.4V, the device is detached.

Problem fix/workaround

According to the USB power drop budget, this may require connecting the device toa root hub or a self-powered hub.

3. Spike on TWI pins when TWI is enabled

100 ns negative spike occurs on SDA and SCL pins when TWI is enabled.





Problem Fix/workaround

No known workaround, enable ATmega32U6/AT90USB64/128 TWI first versus the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem Fix/workaround

Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

1. Asynchronous timer interrupt wake up from sleep generates multiple interrupts

If the CPU core is in sleep and wakes-up from an asynchronous timer interrupt and then go back in sleep again it may wake up multiple times.

Problem Fix/workaround

A software workaround is to wait with performing the sleep instruction until TCNT2>OCR2+1.

8.4 AT90USB1287/6 Third Release

- Incorrect CPU behavior for VBUSTI and IDTI interrupts routines
- Transient perturbation in USB suspend mode generates over consumption
- Spike on TWI pins when TWI is enabled
- High current consumption in sleep mode
- Async timer interrupt wake up from sleep generate multiple interrupts

5. Incorrect CPU behavior for VBUSTI and IDTI interrupts routines

The CPU core may incorrectly execute the interrupt vector related to the VBUSTI and IDTI interrupt flags.

Problem fix/workaround

Do not enable these interrupts, firmware must process these USB events by polling VBUSTI and IDTI flags.

4. Transient perturbation in USB suspend mode generates overconsumption

In device mode and when the USB is suspended, transient perturbation received on the USB lines generates a wake up state. However the idle state following the perturbation does not set the SUSPI bit. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300μ A extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

3. Spike on TWI pins when TWI is enabled

100 ns negative spike occurs on SDA and SCL pins when TWI is enabled.

Problem Fix/workaround

No known workaround, enable ATmega32U6/AT90USB64/128 TWI first, before the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem Fix/workaround

Before entering sleep, interrupts not used to wake up the part from sleep mode should be disabled.

Asynchronous timer interrupt wake up from sleep generates multiple interrupts
 If the CPU core is in sleep mode and wakes-up from an asynchronous timer interrupt and
 then goes back into sleep mode, it may wake up multiple times.

Problem Fix/workaround





A software workaround is to wait beforeperforming the sleep instruction: until TCNT2>OCR2+1.

9. AT90USB647/6 Errata.

- Incorrect interrupt routine exection for VBUSTI, IDTI interrupts flags
- USB Eye Diagram violation in low-speed mode
- Transient perturbation in USB suspend mode generates over consumption
- Spike on TWI pins when TWI is enabled
- High current consumption in sleep mode
- Async timer interrupt wake up from sleep generate multiple interrupts

6. Incorrect CPU behavior for VBUSTI and IDTI interrupts routines

The CPU core may incorrectly execute the interrupt vector related to the VBUSTI and IDTI interrupt flags.

Problem fix/workaround

Do not enable these interrupts, firmware must process these USB events by polling VBUSTI and IDTI flags.

5. USB Eye Diagram violation in low-speed mode

The low to high transition of D- violates the USB eye diagram specification when transmitting with low-speed signaling.

Problem fix/workaround

None.

4. Transient perturbation in USB suspend mode generates overconsumption

In device mode and when the USB is suspended, transient perturbation received on the USB lines generates a wake up state. However the idle state following the perturbation does not set the SUSPI bit anymore. The internal USB engine remains in suspend mode but the USB differential receiver is still enabled and generates a typical 300µA extra-power consumption. Detection of the suspend state after the transient perturbation should be performed by software (instead of reading the SUSPI bit).

Problem fix/workaround

USB waiver allows bus powered devices to consume up to 2.5mA in suspend state.

3. Spike on TWI pins when TWI is enabled

100 ns negative spike occurs on SDA and SCL pins when TWI is enabled.

Problem Fix/workaround

No known workaround, enable ATmega32U6/AT90USB64/128 TWI first versus the others nodes of the TWI network.

2. High current consumption in sleep mode

If a pending interrupt cannot wake the part up from the selected mode, the current consumption will increase during sleep when executing the SLEEP instruction directly after a SEI instruction.

Problem Fix/workaround

Before entering sleep, interrupts not used to wake up the part from the sleep mode should be disabled.

1. Asynchronous timer interrupt wake up from sleep generates multiple interrupts

If the CPU core is in sleep and wakes-up from an asynchronous timer interrupt and then go back in sleep mode again it may wake up several times.

Problem Fix/workaround

A software workaround is to wait with performing the sleep instruction until TCNT2>OCR2+1.

10. ATmega32U6 Errata.

- Spike on TWI pins when TWI is enabled
- · Async timer interrupt wake up from sleep generate multiple interrupts

2. Spike on TWI pins when TWI is enabled

100 ns negative spike occurs on SDA and SCL pins when TWI is enabled.

Problem Fix/workaround

No known workaround, enable ATmega32U6/AT90USB64/128 TWI first versus the others nodes of the TWI network.

1. Asynchronous timer interrupt wake up from sleep generates multiple interrupts

If the CPU core is in sleep and wakes-up from an asynchronous timer interrupt and then go back in sleep mode again it may wake up several times.

Problem Fix/workaround

A software workaround is to wait with performing the sleep instruction until TCNT2>OCR2+1.





11. Datasheet Revision History for ATmega32U6/AT90USB64/128

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

11.1 Changes from 7593A to 7593B

- 1. Changed default configuration for fuse bytes and security byte.
- 2. Suppression of timer 4,5 registers which does not exist.
- 3. Updated typical application schematics in USB section

11.2 Changes from 7593B to 7593C

1. Update to package drawings, MQFP64 and TQFP64.

11.3 Changes from 7593C to 7593D

 For further product compatibility, changed USB PLL possible prescaler configurations. Only 8MHz and 16MHz crystal frequencies allows USB operation (See Table 6-11 on page 49).

11.4 Changes from 7593D to 7593E

- 1. Updated PLL Prescaler table: configuration words are different between AT90USB64x and AT90USB128x to enable the PLL with a 16 MHz source.
- 2. Cleaned up some bits from USB registers, and updated information about OTG timers, remote wake-up, reset and connection timings.
- 3. Updated clock distribution tree diagram (USB prescaler source and configuration register).
- 4. Cleaned up register summary.
- 5. Suppressed PCINT23:8 that do not exist from External Interrupts.
- 6. Updated Electrical Characteristics.
- 7. Added Typical Characteristics.
- 8. Update Errata section.

11.5 Changes from 7593E to 7593F

- 1. Removed 'Preliminary' from document status.
- 2. Clarification in Stand by mode regarding USB.

11.6 Changes from 7593F to 7593G

1. Updated Errata section.

11.7 Changes from 7593G to 7593H

- 1. Added Signature information for 64K devices.
- 2. Fixed figure for typical bus powered application
- 3. Added min/max values for BOD levels
- 4. Added ATmega32U6 product
- 5. Update Errata section
- 6. Modified descriptions for HWUPE and WAKEUPE interrupts enable (these interrupts should be enabled only to wake up the CPU core from power down mode).

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7. Added description to access unique serial number located in Signature Row see "Reading the Signature Row from Software" on page 360.

11.8 Changes from 7593H to 7593I

1. Updated Table 8-2 in "Brown-out Detection" on page 60. Unused BOD levels removed.

