GENERAL DESCRIPTION

The SP510E is a highly integrated physical layer solution that is configurable to support multiple serial standards. It incorporates eight drivers and eight receivers (8TX/8RX), configurable for either differential (V.11 or V.35) or single ended (V.28 and V.10) signaling.

SP510E enables a Serial Communications Controller to implement a variety of serial port types including V.24, V.25, V.36, EIA-530, EIA-530-A, X.21, RS-232. The device architecture is designed to support the data and clock signals used in HDLC or SDLC serial ports as either DTE or DCE.

Operating configuration is programmable in system using the mode-select pins. The V.11 and V.35 modes include internal bus termination that may be switched in or out using the TERM_OFF pin.

The SP510E is ideal for space constrained applications. It requires only a single 5V supply for full operation. The V_L pin determines the receiver output voltage (V_{OH}, down to 1.65V), for interfacing with lower voltage CPUs and FPGAs. For single supply operation at 5V the V_L pin will be connected to V_{CC}.

Fully compliant V.28 and V.10 driver output voltages are generated using the onboard charge pump. Special power sequencing is not required during system startup. Charge pump outputs are internally regulated to minimize power consumption. The SP510E requires only four 1µF capacitors for complete functionality. The device may be put into a low power shutdown mode when not in active use.

All receivers have fail-safe protection to put outputs into an output-high state when inputs are open, shorted, or terminated but idle.

FEATURES

- Up to 52Mbps Differential Transmission Rates
- ±15kV HBM ESD Tolerance for Analog I/O Pins
- Integrated Termination Resistors for V.11/V.35
- Eight Drivers and Eight Receivers (8TX/8RX)
- Adjustable Logic Level Pin V_L (Down to 1.65V)
- Software Selectable Protocols with 3-Bit Word:
  - RS-232 (V.28)
  - EIA-530 (V.10 & V.11)
  - EIA-530A (V.10 & V.11)
  - X.21 (V.11)
  - RS-449/V.36
- Internal Line or Digital Loopback Testing
- Adheres to NET1/NET2 and TBR2 Requirements
- Easy Flow-Through Pinout
- Single +5V Supply Voltage
- Individual Driver/Receiver Enable/Disable Controls
- Operates in DTE or DCE Mode
- Pin Compatible Upgrade for SP509, SP508

TYPICAL APPLICATIONS

- Data Communication Networks
- Telecommunication Equipment
- Secured Data Communication
- CSU and DSU
- Data Routers
- Network Switches
- WAN Access Equipment
- VoIP-PBX Gateways

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE	DEVICE STATUS
SP510EEF-L	100-pin LQFP	-40°C to +85°C	Active
SP510ECF-L	100-pin LQFP	0°C to +70°C	Active

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Supply Voltage V_{CC}	+7.0V
Logic-Interface Voltage (V_L)	$V_L \leq V_{CC}$
Receiver DC Input Voltage	±15.5V
Input Voltage at TTL Input Pins	-0.3V to (V_{CC} + 0.5V)
Driver Output Voltage (from Ground)	-7.5V to +12.5V
Short Circuit Duration, TxOUT to GND	Continuous
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation at T_{AMB} = +70°C 100-Pin LQFP (derate 19mW/°C above +70°C) θ_{JA} = 52.7°C/W, θ_{JC} = 6.5°C/W	1520mW

ESD PROTECTION

TX Output & RX Input Pins	±15	kV	Human Body Model
All Other Pins	±2	kV	Human Body Model

TABLE 1: DC ELECTRICAL CHARACTERISTICS

DC ELECTRICAL CHARACTERISTICS Vcc = +4.75V to +5.25V, C1-C4 = 1µF. T_{AMB} = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_{AMB} = +25°C						
PARAMETERS	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
V_{CC} Supply Voltage	V_{CC}		4.75		5.25	V
Logic Interface Voltage	V_L	$V_L \leq V_{CC}$	1.65		5.25	V
I_{CC} Supply Current	I_{CC}				300	mA
I_{CC} Shutdown	I_{CCSD}			200		µA
DRIVER INPUT AND LOGIC INPUT PINS						
Logic Input High	V_{IH}		1.6			V
Logic Input Low	V_{IL}				0.4	V
RECEIVER OUTPUTS						
Receiver Logic Output Low	V_{OL}	I_{OUT} = -3.2 mA			0.4	V
Receiver Logic Output High	V_{OH}	I_{OUT} = 1 mA	V_L-0.3		V_L+0.3	V
Receiver Output Short-Circuit Current	I_{OSS}	0V < V_O < V_{CC}		±20	±60	mA
Receiver Output Leakage Current	I_{OZ}	Receivers disabled 0.4V < V_O < 5.25V		±0.05	±1	µA
V.28 / RS-232 DRIVERS						
Output Voltage Swing	V_T	Output load = 3kΩ to GND Figure 3	±5	±6	±15	V
	V_{OC}	Open Circuit Output Figure 2			±15	V
Short Circuit Current	I_{SC}	V_{OUT} = 0V, Figure 5			±100	mA
Power-Off Impedance		Figure 6	300	10M		Ω
V.28 / RS-232 RECEIVERS						
Input Voltage Range			-15		15	V
Input Threshold Low			0.8	1.2		V
Input Threshold High				1.7	3	V
Input Hysteresis				500		mV
Input Resistance		Figure 8	3	5	7	kΩ
Open Circuit Bias	V_{OC}	Figure 9			±2	V

DC ELECTRICAL CHARACTERISTICS

Vcc = +4.75V to +5.25V, C1-C4 = 1µF. T_{AMB} = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_{AMB} = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V.10 / RS-423 DRIVERS						
Open Circuit Voltage	V_{OC}	Figure 10	±4		±6	V
Test Terminated Voltage	V_T	Figure 11	$0.9V_{OC}$			V
Short Circuit Current	I_{SC}	Figure 12			±150	mA
Power-Off Current		Figure 13			±100	µA
V.10 / RS-423 RECEIVERS						
Input Current	I_{IA}	Figure 15 and Figure 16	-3.25		+3.25	mA
Input Impedance			4	15		kΩ
Sensitivity					±0.2	V
V.11 / RS-422 DRIVERS						
Open Circuit Voltage	V_{OCA},V_{OCB}	Figure 17			±6	V
Test Terminated Voltage	V_T	Figure 18	±2			V
Balance	ΔV_T	Figure 18			±0.4	V
Driver DC Offset	V_{OS}	Figure 18			3	V
Offset Balance	ΔV_{OS}	Figure 18			±0.4	V
Short Circuit Output Current	I_{SA}, I_{SB}	Figure 19			±150	mA
Power-Off Current		Figure 20			±100	µA
V.11 / RS-422 RECEIVERS						
Receiver Input Range	V_{CM}		-7		+7	V
Input Current	I_{IA}, I_{IB}	Figure 21 and Figure 23			±3.25	mV
Input Current with Termination	I_{IA}, I_{IB}	Figure 24 and Figure 25			±60.75	mA
Receiver Input Impedance	R_{IN}	-10V ≤ V_{CM} ≤ +10V	4	15		kΩ
Receiver Sensitivity	V_{TH}				±0.2	V
Receiver Input Hysteresis	ΔV_{TH}	V_{CM} = 0 V		15		mV

DC ELECTRICAL CHARACTERISTICS

Vcc = +4.75V to +5.25V, C1-C4 = 1µF. T_{AMB} = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_{AMB} = +25°C

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V.35 DRIVERS (ALL VALUES MEASURED WITH TERM_OFF = '0')						
Test Terminated Voltage	V_T	Figure 26	±0.44		±0.66	V
Offset	V_{OS}	Figure 26			±0.6	V
Output Overshoot		Figure 26, V_{ST} = Steady State Voltage	-0.2V_{ST}		+0.2V_{ST}	V
Source Impedance		Figure 29 $Z_S = V_2 / V_1 \times 50\Omega$	50		150	Ω
Short Circuit Impedance		Figure 28	135		165	Ω
V.35 RECEIVERS (ALL VALUES MEASURED WITH TERM_OFF = '0')						
Sensitivity				±100	±200	mV
Source Impedance		Figure 30 $Z_S = V_2 / V_1 \times 50\Omega$	90		110	Ω
Short-Circuit Impedance		Figure 31	135		165	Ω
TRANSCEIVER LEAKAGE CURRENT						
Driver Output Tri-state Current		Drivers disabled, Figure 32		500		µA
Receiver Output Tri-state Current		Tx and Rx Disabled, $0.4V \le V_O \le 2.4V$		1	10	µA

TABLE 2: AC TIMING CHARACTERISTICS

TIMING CHARACTERISTICS

V_{CC} = +4.75 to 5.25V, C1-C4 = 1µF; T_{AMB} = T_{MIN} to T_{MAX}, unless noted. Typical values are at T_{AMB} = +25°C.

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V.28 / RS-232 DRIVER						
Maximum Transmission Rate		Figure 7	250			kbps
Driver Propagation Delay	t_{DPHL}, t_{DPLH}		0.5	1	5	µs
Driver Transition Time		+3V to -3V, Figure 7	0.2		1.5	µs
Instantaneous Slew Rate		+3V to -3V, Figure 4	4		30	V/µs
Driver Skew		$\lvert t_{DPHL} - t_{DPLH} \rvert$ at zero crossing		100	800	ns
Driver Channel to Channel Skew				20		ns
Driver Output Enable Time Tri-state to Output Low	t_{DZL}	C_L = 100 pF, S1 closed Figure 34 and Figure 40			2	µs
Driver Output Enable Time Tri-state to Output High	t_{DZH}	C_L = 100 pF, S2 closed Figure 34 and Figure 40			2	µs
Driver Output Disable Time Output Low to Tri-state	t_{DLZ}	C_L = 15 pF, S1 closed Figure 34 and Figure 40			2	µs
Driver Output Disable Time Output High to Tri-state	t_{DHZ}	C_L = 15 pF, S2 closed Figure 34 and Figure 40			2	µs
V.28 / RS-232 RECEIVER						
Receiver Propagation Delay	t_{PHL}, t_{PLH}	R_IN to R_OUT, C_L = 15 pF	50	100	500	ns
Receiver Skew		$\lvert t_{PHL} - t_{PLH} \rvert$ at 1.5V		50		ns
Receiver Channel to Channel Skew				20		ns
Receiver Output Rise / Fall Time	t_R, t_F	C_L = 15 pF		15		ns
Receiver Output Enable Time Tri-state to Output Low	t_{ZL}	C_L = 100 pF, S1 closed Figure 35 and Figure 40			2	µs
Receiver Output Enable Time Tri-state to Output High	t_{ZH}	C_L = 100 pF, S2 closed Figure 35 and Figure 40			2	µs
Receiver Output Disable Time Output Low to Tri-state	t_{LZ}	C_L = 15 pF, S1 closed Figure 35 and Figure 40			2	µs
Receiver Output Disable Time Output High to Tri-state	t_{HZ}	C_L = 15 pF, S2 closed Figure 35 and Figure 40			2	µs
Charge Pump Rise Time		Shutdown to operational			2	ms

TIMING CHARACTERISTICS

V_{CC} = +4.75 to 5.25V, C1-C4 = 1µF; T_{AMB} = T_{MIN} to T_{MAX}, unless noted. Typical values are at T_{AMB} = +25°C.

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V.10 / RS-423 DRIVER						
Maximum Transmission Rate			250			kbps
Driver Propagation Delay	t_{DPHL}, t_{DPLH}		30	150	500	ns
Driver Rise / Fall Time	t_{DR}, t_{DF}	10% to 90%, Figure 14			500	ns
Driver Skew		$\lvert t_{DPHL} - t_{DPLH} \rvert$ at zero crossing			100	ns
Driver Channel to Channel Skew				5		ns
Driver Output Enable Time Tri-state to Output Low	t_{DZL}	C_L = 100 pF, S1 closed Figure 34 and Figure 40			2	µs
Driver Output Enable Time Tri-state to Output High	t_{DZH}	C_L = 100 pF, S2 closed Figure 34 and Figure 40			2	µs
Driver Output Disable Time Output Low to Tri-state	t_{DLZ}	C_L = 15 pF, S1 closed Figure 34 and Figure 40			2	µs
Driver Output Disable Time Output High to Tri-state	t_{DHZ}	C_L = 15 pF, S2 closed Figure 34 and Figure 40			2	µs
V.10 / RS-423 RECEIVER						
Receiver Propagation Delay	t_{PHL}, t_{PLH}			100	500	ns
Receiver Output Rise / Fall Time	t_R, t_F	C_L = 15 pF		15		ns
Receiver Skew		$\lvert t_{PHL} - t_{PLH} \rvert$ at 1.5V		5		ns
Receiver Channel to Channel Skew				5		ns
Receiver Output Enable Time Tri-state to Output Low	t_{ZL}	C_L = 100 pF, S1 closed Figure 35 and Figure 40			2	µs
Receiver Output Enable Time Tri-state to Output High	t_{ZH}	C_L = 100 pF, S2 closed Figure 35 and Figure 40			2	µs
Receiver Output Disable Time Output Low to Tri-state	t_{LZ}	C_L = 15 pF, S1 closed Figure 35 and Figure 40			2	µs
Receiver Output Disable Time Output High to Tri-state	t_{HZ}	C_L = 15 pF, S2 closed Figure 35 and Figure 40			2	µs

TIMING CHARACTERISTICS

V_{CC} = +4.75 to 5.25V, C1-C4 = 1µF; T_{AMB} = T_{MIN} to T_{MAX}, unless noted. Typical values are at T_{AMB} = +25°C.

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH SPEED V.11 / RS-422 (DRIVERS 1, 2 & 3)						
Maximum Bit Rate			52			Mbps
Driver Rise and Fall Time	t_{DR}, t_{DF}	10-90% Figure 22 and Figure 36			6	ns
Driver Propagation Delay Time	t_{DPHL}, t_{DPLH}	C_L = 50 pF Figure 33 and Figure 36		20	50	ns
Driver Skew		$\lvert t_{DPHL} - t_{DPLH} \rvert$ C_L = 50 pF Figure 33 and Figure 36			3.8	ns
Driver Channel to Channel Skew				2		ns
Driver Output Enable Time Tri-state to Output Low	t_{DZL}	C_L = 100 pF, S1 closed Figure 34 and Figure 37			100	ns
Driver Output Enable Time Tri-state to Output High	t_{DZH}	C_L = 100 pF, S2 closed Figure 34 and Figure 37			100	ns
Driver Output Disable Time Output Low to Tri-state	t_{DLZ}	C_L = 15 pF, S1 closed Figure 34 and Figure 37			100	ns
Driver Output Disable Time Output High to Tri-state	t_{DHZ}	C_L = 15 pF, S2 closed Figure 34 and Figure 37			100	ns
HIGH SPEED V.11 / RS-422 (RECEIVERS 1, 2 & 3)						
Receiver Output Rise / Fall Time	t_R, t_F	C_L = 50 pF			6	ns
Receiver Propagation Delay	t_{PHL}, t_{PLH}	C_L = 50 pF Figure 33 and Figure 38		20	50	ns
Receiver Skew		$\lvert t_{PHL} - t_{PLH} \rvert$ C_L = 50 pF Figure 33 and Figure 38			3.8	ns
Receiver Channel to Channel Skew				2		ns
Receiver Output Enable Time Tri-state to Output Low	t_{ZL}	C_L = 100 pF, S1 closed Figure 35 and Figure 39			100	ns
Receiver Output Enable Time Tri-state to Output High	t_{ZH}	C_L = 100 pF, S2 closed Figure 35 and Figure 39			100	ns
Receiver Output Disable Time Output Low to Tri-state	t_{LZ}	C_L = 15 pF, S1 closed Figure 35 and Figure 39			100	ns
Receiver Output Disable Time Output High to Tri-state	t_{HZ}	C_L = 15 pF, S2 closed Figure 35 and Figure 39			100	ns

TIMING CHARACTERISTICS

V_{CC} = +4.75 to 5.25V, C1-C4 = 1µF; T_{AMB} = T_{MIN} to T_{MAX}, unless noted. Typical values are at T_{AMB} = +25°C.

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V.11 / RS-422 HANDSHAKE SIGNALS (DRIVERS 4, 5 & 6)						
Maximum Bit Rate		Figure 33	10			Mbps
Driver Rise and Fall Time	t_{DR}, t_{DF}	Figure 22 and Figure 36		2	10	ns
Driver Propagation Delay Time	t_{DPHL}, t_{DPLH}	C_L = 50 pF Figure 33 and Figure 36		20	50	ns
Driver Skew		$\|t_{DPHL} - t_{DPLH}\|$, C_L = 50 pF Figure 33 and Figure 36			10	ns
Driver Channel to Channel Skew				2		ns
Driver Output Enable Time Tri-state to Output Low	t_{DZL}	C_L = 100 pF, S1 closed Figure 34 and Figure 37			100	ns
Driver Output Enable Time Tri-state to Output High	t_{DZH}	C_L = 100 pF, S2 closed Figure 34 and Figure 37			100	ns
Driver Output Disable Time Output Low to Tri-state	t_{DLZ}	C_L = 15 pF, S1 closed Figure 34 and Figure 37			100	ns
Driver Output Disable Time Output High to Tri-state	t_{DHZ}	C_L = 15 pF, S2 closed Figure 34 and Figure 37			100	ns
V.11 / RS-422 HANDSHAKE SIGNALS (RECEIVERS 4, 5 & 6)						
Receiver Output Rise / Fall Time	t_R, t_F	C_L = 50 pF			20	ns
Receiver Propagation Delay	t_{PHL}, t_{PLH}	C_L = 50 pF Figure 33 and Figure 38		20	50	ns
Receiver Skew		$\|t_{PHL} - t_{PLH}\|$ C_L = 50 pF Figure 33 and Figure 38			10	ns
Receiver Channel to Channel Skew				2		ns
Receiver Output Enable Time Tri-state to Output Low	t_{ZL}	C_L = 100 pF, S1 closed Figure 35 and Figure 39			100	ns
Receiver Output Enable Time Tri-state to Output High	t_{ZH}	C_L = 100 pF, S2 closed Figure 35 and Figure 39			100	ns
Receiver Output Disable Time Output Low to Tri-state	t_{LZ}	C_L = 15 pF, S1 closed Figure 35 and Figure 39			100	ns
Receiver Output Disable Time Output High to Tri-state	t_{HZ}	C_L = 15 pF, S2 closed Figure 35 and Figure 39			100	ns

TIMING CHARACTERISTICS

V_{CC} = +4.75 to 5.25V, C1-C4 = 1µF; T_{AMB} = T_{MIN} to T_{MAX}, unless noted. Typical values are at T_{AMB} = +25°C.

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V.35 (DRIVERS 1, 2 & 3)						
Maximum Bit Rate		f_{MAX} = 20 MHz, Figure 33	40			Mbps
Driver Rise and Fall Time	t_{DR}, t_{DF}	Figure 29			10	ns
Driver Propagation Delay Time	t_{DPHL}, t_{DPLH}	C_L = 50 pF Figure 33 and Figure 36		25	50	ns
Driver Skew		$\lvert t_{DPHL} - t_{DPLH} \rvert$ C_L = 50 pF Figure 33 and Figure 36		2	5	ns
Driver Channel to Channel Skew				2		ns
Driver Output Enable Time Tri-state to Output Low	t_{DZL}	C_L = 100 pF, S1 closed Figure 34 and Figure 37			200	ns
Driver Output Enable Time Tri-state to Output High	t_{DZH}	C_L = 100 pF, S2 closed Figure 34 and Figure 37			200	ns
Driver Output Disable Time Output Low to Tri-state	t_{DLZ}	C_L = 15 pF, S1 closed Figure 34 and Figure 37			200	ns
Driver Output Disable Time Output High to Tri-state	t_{DHZ}	C_L = 15 pF, S2 closed Figure 34 and Figure 37			200	ns
V.35 (RECEIVERS 1, 2 & 3)						
Receiver Propagation Delay	t_{PHL}, t_{PLH}	C_L = 50 pF Figure 33 and Figure 38		30	50	ns
Receiver Skew		$\lvert t_{PHL} - t_{PLH} \rvert$ C_L = 50 pF Figure 33 and Figure 38			5	ns
Receiver Channel to Channel Skew				2		ns
Receiver Output Enable Time Tri-state to Output Low	t_{ZL}	C_L = 100 pF, S1 closed Figure 35 and Figure 39			200	ns
Receiver Output Enable Time Tri-state to Output High	t_{ZH}	C_L = 100 pF, S2 closed Figure 35 and Figure 39			200	ns
Receiver Output Disable Time Output Low to Tri-state	t_{LZ}	C_L = 15 pF, S1 closed Figure 35 and Figure 39			200	ns
Receiver Output Disable Time Output High to Tri-state	t_{HZ}	C_L = 15 pF, S2 closed Figure 35 and Figure 39			200	ns

FIGURE 1. PIN OUT DIAGRAM

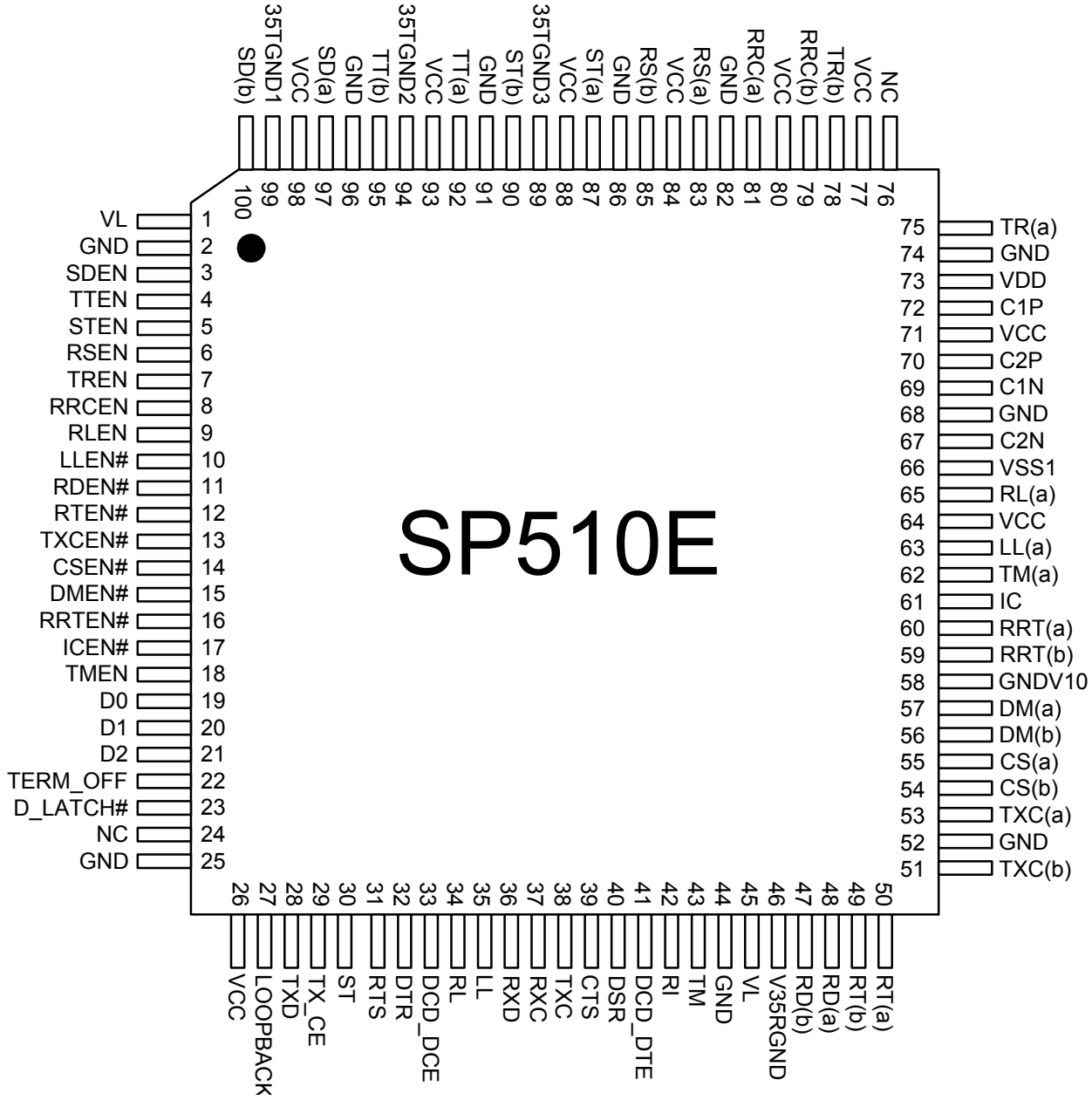


TABLE 3: PIN DESCRIPTIONS BY FUNCTION

PIN NAME	PIN NUMBER	I/O		DESCRIPTION
DIFFERENTIAL DRIVERS				
TxD	28	I	TTL	TxD Driver Input
SD(b) / SD(a)	100, 97	O	TTL	Differential Transmit data non-inverting (b) and inverting (a) outputs
V35TGND1	99	I		SD Termination Reference
SDEN	3	I	TTL	TxD Driver Enable
TxCE	29	I	TTL	TxCE Driver Input
TT(b) / TT(a)	95, 92	O	TTL	Differential TxCE non-inverting (b) and inverting (a) outputs
V35TGND2	94	I		TT Termination Reference
TTEN	4	I	TTL	TxCE Driver Enable
ST	30	I	TTL	ST Driver Input
ST(b) / ST(a)	90, 87	O	TTL	Differential ST non-inverting (b) and inverting (a) outputs
V35TGND3	89	I		ST Termination Reference
STEN	5	I	TTL	ST Driver Enable
RTS	31	I	TTL	RTS Driver Input
RS(b) / RS(a)	85, 83	O	TTL	Differential RTS non-inverting (b) and inverting (a) outputs
RSEN	6	I	TTL	RTS Driver Enable
DTR	32	I	TTL	DTR Driver Input
TR(b) / TR(a)	78, 75	O	TTL	Differential DTR non-inverting (b) and inverting (a) outputs
TREN	7	I	TTL	DTR Driver Enable
DCD_DCE	33	I	TTL	DCD_DCE Driver Input
RRC(b) / RRC(a)	79, 81	O	TTL	Differential DCD non-inverting (b) and inverting (a) outputs
RRCEN	8	I	TTL	DCD Driver Enable
SINGLE ENDED DRIVERS				
RL	34	I	TTL	RL Driver Input
RL(a)	65	O	TTL	RL Driver Output
RLEN	9	I	TTL	RL Driver Enable
LL	35	I	TTL	LL Driver Input
LL(a)	63	O	TTL	LL Driver Output
LLEN#	10	I	TTL	LL Driver Enable, active low

PIN NAME	PIN NUMBER	I/O		DESCRIPTION
DIFFERENTIAL RECEIVERS				
RxD	36	O	TTL	RxD Receiver Output
RD(b) / RD(a)	47, 48	I	TTL	Differential RXD non-inverting (b) and inverting (a) inputs
RDEN#	11	I	TTL	RxD Receiver Enable, active low
RxC	37	O	TTL	RxC Receiver Output
RT(b) / RT(a)	49, 50	I	TTL	Differential RXC non-inverting (b) and inverting (a) inputs
RTEN#	12	I	TTL	RxC Receiver Enable, active low
TxC	38	O	TTL	TxC Receiver Output
TxC(b) / TxC(a)	51, 53	I	TTL	Differential TxC non-inverting (b) and inverting (a) inputs
TxCEN#	13	I	TTL	TxC Receiver Enable, active low
CTS	39	O	TTL	CTS Receiver Output
CS(b) / CS(a)	54, 55	I	TTL	Differential CTS non-inverting (b) and inverting (a) inputs
CSEN#	14	I	TTL	CTS Receiver Enable, active low
DSR	40	O	TTL	DSR Receiver Output
DM(b) / DM(a)	56, 57	I	TTL	Differential DSR non-inverting (b) and inverting (a) inputs
DMEN#	15	I	TTL	DSR Receiver Enable, active low
DCD_DTE	41	O	TTL	DCD_DTE Receiver Output
RRT(b) / RRT(a)	59, 60	I	TTL	Differential DCD_DTE non-inverting (b) and inverting (a) inputs
RRTEN#	16	I	TTL	DCD_DTE Receiver Enable, active low
SINGLE ENDED RECEIVERS				
IC	61	I	TTL	RI Receiver Input
RI	42	O	TTL	RI Receiver Output
ICEN#	17	I	TTL	RI Receiver Enable, active low
TM(a)	62	I	TTL	TM Receiver Input
TM	43	O	TTL	TM Receiver Output
TMEN	18	I	TTL	TM Receiver Enable

PIN NAME	PIN NUMBER	I/O		DESCRIPTION
PROTOCOL & MODE SELECTION PINS				
D2, D1, D0	21, 20, 19	I	TTL	Mode Select - Refer to Table 5 and Table 6
CHARGE PUMP PINS				
C1P, C1N	72, 69	I		Charge Pump Capacitor 1 +/- inputs. Connect a 1 µF capacitor between C1P and C1N pins.
C2P, C2N	70, 67	I		Charge Pump Capacitor 2 +/- inputs. Connect a 1 µF capacitor between C2P and C2N pins.
VSS1	66	I		$-2xV_{CC}$ Charge Pump
VDD	73	I		$2xV_{CC}$ Charge Pump
GENERAL CONTROL PINS				
LOOPBACK#	27	I	TTL	Loopback mode enable, active low
D_LATCH#	23	I		Decoder Latch, active low
TERM_OFF	22	I		Termination disable
RESERVED PINS				
NC	24, 76			No Connect
POWER AND GROUND PINS				
VCC	26, 64, 71, 77, 80, 84, 88, 98	I		5V supply
VL	1, 45	I		Logic I/O Power Supply Input
GND	2, 25, 44, 52, 68, 74, 82, 86, 91, 96	I		Ground
GNDV10	58	I		V.10 Receiver Ground Reference
V35RGND	46	O		Receiver Termination Reference

NOTE: **Pin type: I = Input, O = Output, I/O = Input/output.**

TABLE 4: PIN DESCRIPTIONS BY PIN NUMBER

PIN DESCRIPTIONS BY PIN NUMBER					
1	VL	Logic I/O Power Supply Input	32	DTR	DTR Driver TTL Input
2	GND	Ground	33	DCD_DCE	DCD_DCE Driver TTL Input
3	SDEN	TxD Driver Enable Input	34	RL	RL Driver TTL Input
4	TTEN	TxCE Driver Enable Input	35	LL	LL Driver TTL Input
5	STEN	ST Driver Enable Input	36	RxD	RxD Receiver TTL Output
6	RSEN	RTS Driver Enable Input	37	RxC	RxC Receiver TTL Output
7	TREN	DTR Driver Enable Input	38	TxC	TxC Receiver TTL Output
8	RRCEN	DCD Driver Enable Input	39	CTS	CTS Receiver TTL Output
9	RLEN	RL Driver Enable Input	40	DSR	DSR Receiver TTL Output
10	LLEN#	LL Driver Enable Input	41	DCD_DTE	DCD_DTE Receiver TTL Output
11	RDEN#	RxD Receiver Enable Input	42	RI	RI Receiver TTL Output
12	RTEN#	RxC Receiver Enable Input	43	TM	TM Receiver TTL Output
13	TxCEN#	TxC Receiver Enable Input	44	GND	Ground
14	CSEN#	CTS Receiver Enable Input	45	VL	Logic I/O Power Supply Input
15	DMEN#	DSR Receiver Enable Input	46	V35RGND	Receiver Termination Reference
16	RRTEN#	DCD_DTE Receiver Enable Input	47	RD(b)	RXD Non-Inverting Input
17	ICEN#	RI Receiver Enable Input	48	RD(a)	RXD Inverting Input
18	TMEN	TM Receiver Enable Input	49	RT(b)	RxC Non-Inverting Input
19	D0	Mode Select Input - Bit 0	50	RT(a)	RxC Inverting Input
20	D1	Mode Select Input - Bit 1	51	TxC(b)	TxC Non-Inverting Input
21	D2	Mode Select Input - Bit 2	52	GND	Ground
22	TERM_OFF	Termination Disable Input	53	TxC(a)	TxC Inverting Input
23	D_LATCH#	Decoder Latch Input	54	CS(b)	CTS Non-Inverting Input
24	N/C	No Connect	55	CS(a)	CTS Inverting Input
25	GND	Ground	56	DM(b)	DSR Non-Inverting Input
26	VCC	5V Power Supply Input	57	DM(a)	DSR Inverting Input
27	LOOP-BACK#	Loopback Mode Enable Input	58	GNDV10	V.10 Rx Ground Reference
28	TxD	TxD Driver TTL Input	59	RRT(b)	DCD_DTE Non-Inverting Input
29	TxCE	TxCE Driver TTL Input	60	RRT(a)	DCD_DTE Inverting Input
30	ST	ST Driver TTL Input	61	IC	RI Receiver Input
31	RTS	RTS Driver TTL Input	62	TM(a)	TM Receiver Input

PIN DESCRIPTIONS BY PIN NUMBER					
63	LL(a)	LL Driver Output	82	GND	Ground
64	VCC	5V Power Supply Input	83	RS(a)	RTS Inverting Output
65	RL(a)	RL Driver Output	84	VCC	5V Power Supply Input
66	VSS1	-2 x V_{CC} Charge Pump	85	RS(b)	RTS Non-Inverting Output
67	C2N	Charge Pump Capacitor	86	GND	Ground
68	GND	Ground	87	ST(a)	ST Inverting Output
69	C1N	Charge Pump Capacitor	88	VCC	5V Power Supply Input
70	C2P	Charge Pump Capacitor	89	V35TGND3	ST Termination Reference
71	VCC	5V Power Supply Input	90	ST(b)	ST Non-Inverting Output
72	C1P	Charge Pump Capacitor	91	GND	Ground
73	VDD	2 x V_{CC} Charge Pump	92	TT(a)	TxCE Inverting Output
74	GND	Ground	93	VCC	5V Power Supply Input
75	TR(a)	DTR Inverting Output	94	V35TGND2	TT Termination Reference
76	NC	No Connect	95	TT(b)	TxCE Non-Inverting Output
77	VCC	5V Power Supply Input	96	GND	Ground
78	TR(b)	DTR Non-Inverting Output	97	SD(a)	TxD Inverting Output
79	RRC(b)	DCD Non-Inverting Output	98	VCC	5V Power Supply Input
80	VCC	5V Power Supply Input	99	V35TGND1	SD Termination Reference
81	RRC(a)	DCD Inverting Output	100	SD(b)	TxD Non-Inverting Output

TABLE 5: DRIVER MODE SELECTION

DRIVER OUTPUT PIN	V.35 MODE	EIA-530 MODE	RS-232 MODE (V.28)	EIA-530A MODE	RS-449 MODE (V.36)	X.21 MODE (V.11)	SHUT-DOWN	SUGGESTED SIGNAL
MODE (D2, D1, D0)	**001**	**010**	**011**	**100**	**101**	**110**	**111**	
T_1OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxD(a)
T_1OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxD(b)
T_2OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxCE(a)
T_2OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxCE(b)
T_3OUT(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxC_DCE(a)
T_3OUT(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxC_DCE(b)
T_4OUT(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	RTS(a)
T_4OUT(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	RTS(b)
T_5OUT(a)	V.28	V.11	V.28	V.10	V.11	V.11	High-Z	DTR(a)
T_5OUT(b)	High-Z	V.11	High-Z	High-Z	V.11	V.11	High-Z	DTR(b)
T_6OUT(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	DCD_DCE(a)
T_6OUT(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	DCD_DCE(b)
T_7OUT(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	RL
T_8OUT(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	LL

TABLE 6: RECEIVER MODE SELECTION

RECEIVER INPUT PIN	V.35 MODE	EIA-530 MODE	RS-232 MODE (V.28)	EIA-530A MODE	RS-449 MODE (V.36)	X.21 MODE (V.11)	SHUT-DOWN	SUGGESTED SIGNAL
MODE (D2, D1, D0)	**001**	**010**	**011**	**100**	**101**	**110**	**111**	
R_1IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	RxD(a)
R_1IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	RxD(b)
R_2IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	RxCE(a)
R_2IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	RxCE(b)
R_3IN(a)	V.35	V.11	V.28	V.11	V.11	V.11	High-Z	TxC_DTE(a)
R_3IN(b)	V.35	V.11	High-Z	V.11	V.11	V.11	High-Z	TxC_DTE(b)
R_4IN(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	CTS(a)
R_4IN(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	CTS(b)
R_5IN(a)	V.28	V.11	V.28	V.10	V.11	V.11	High-Z	DSR(a)
R_5IN(b)	High-Z	V.11	High-Z	High-Z	V.11	V.11	High-Z	DSR(b)
R_6IN(a)	V.28	V.11	V.28	V.11	V.11	V.11	High-Z	DCD_DTE(a)
R_6IN(b)	High-Z	V.11	High-Z	V.11	V.11	V.11	High-Z	DCD_DTE(b)
R_7IN(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	RI
R_8IN(a)	V.28	V.10	V.28	V.10	V.10	High-Z	High-Z	TM

TABLE 7: V.11 & V.35 DRIVERS

INPUTS		OUTPUTS	
TX_EN#	TX_IN	TX(A)	TX(B)
1	1	0	1
1	0	1	0

TABLE 8: V.28 DRIVERS

INPUTS		OUTPUTS	
TX_EN#	TX_IN	TX(A)	TX(B)
1	1	< -5V	> 30 kΩ
1	0	> +5V	> 30 kΩ

TABLE 9: V.10 DRIVERS

INPUTS		OUTPUTS	
TX_EN#	TX_IN	TX(A)	TX(B)
1	1	< -4V	> 30 kΩ
1	0	> +4V	> 30 kΩ

TABLE 10: V.11 & V.35 RECEIVERS

INPUTS	OUTPUTS
RX(A) - RX(B)	RO
≥ 200 mV	1
≤ –200 mV	0
Open / shorted	1

TABLE 11: V.28 RECEIVERS

INPUTS	OUTPUTS
RX(A) - RX(B)	RO
≥ +3V	0
≤ –3V	1
Open / ground	1

TABLE 12: V.10 RECEIVERS

INPUTS	OUTPUTS
RX(A) - RX(B)	RO
≥ +0.3V	0
≤ –0.3V	1
Open / ground	1

FIGURE 2. V.28 DRIVER OUTPUT OPEN CIRCUIT VOLTAGE

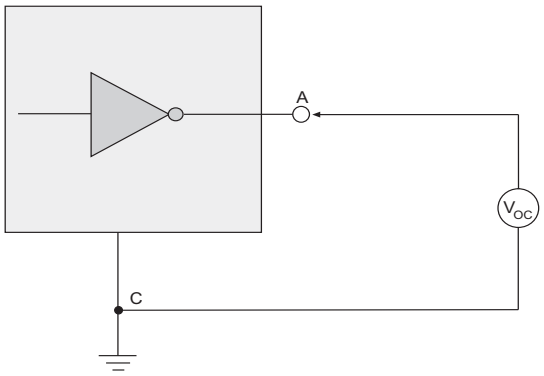


FIGURE 3. V.28 DRIVER OUTPUT LOADED VOLTAGE

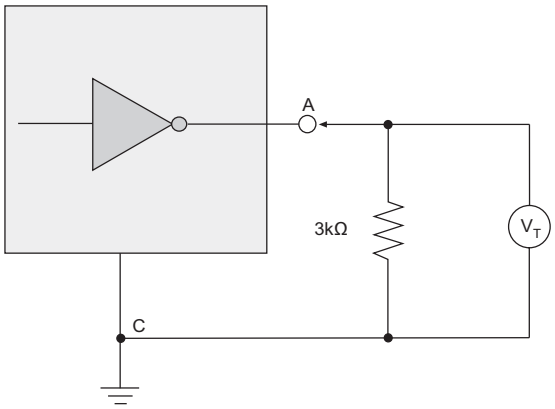


FIGURE 4. V.28 DRIVER OUTPUT SLEW RATE

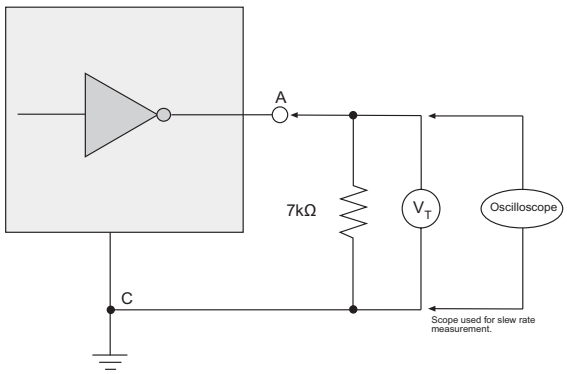


FIGURE 5. V.28 DRIVER OUTPUT SHORT CIRCUIT CURRENT

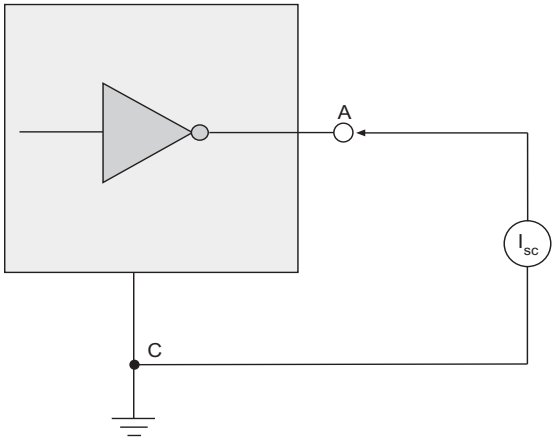


FIGURE 6. V.28 DRIVER OUTPUT POWER-OFF IMPEDANCE

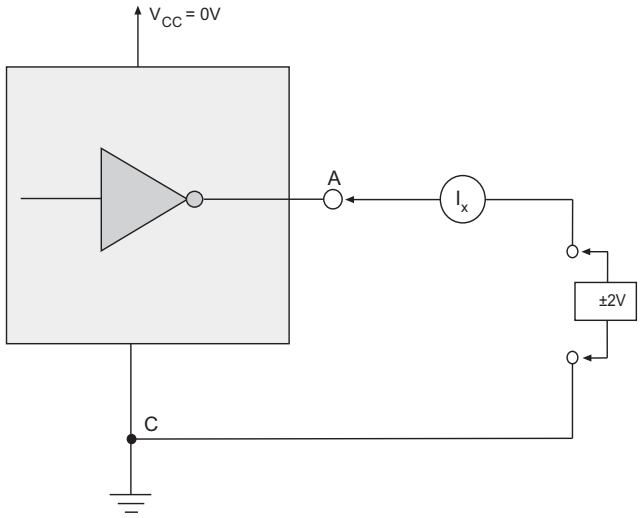


FIGURE 7. V.28 DRIVER OUTPUT RISE/FALL TIME

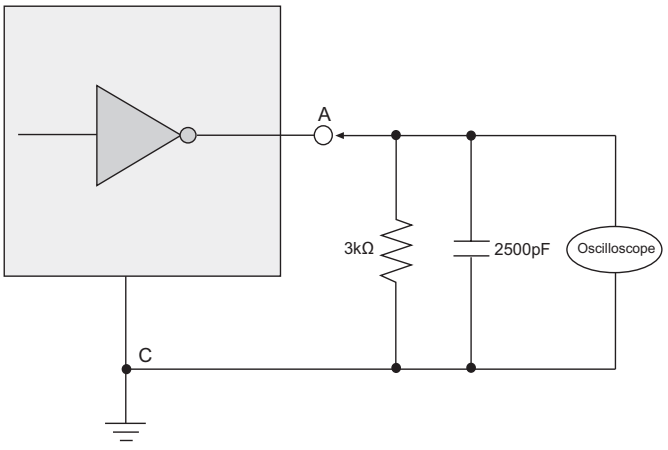


FIGURE 8. V.28 RECEIVER INPUT IMPEDANCE

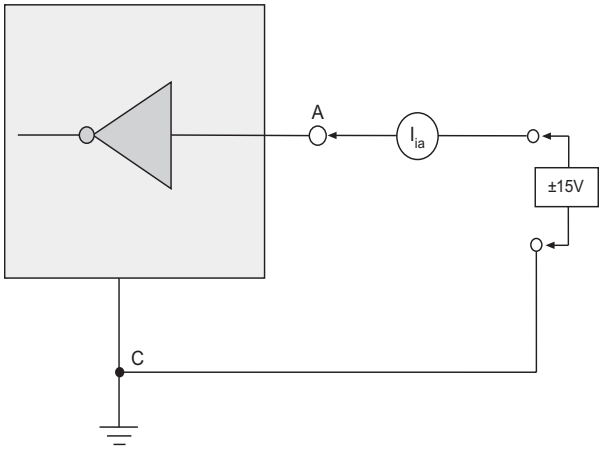


FIGURE 9. V.28 RECEIVER INPUT OPEN-CIRCUIT BIAS

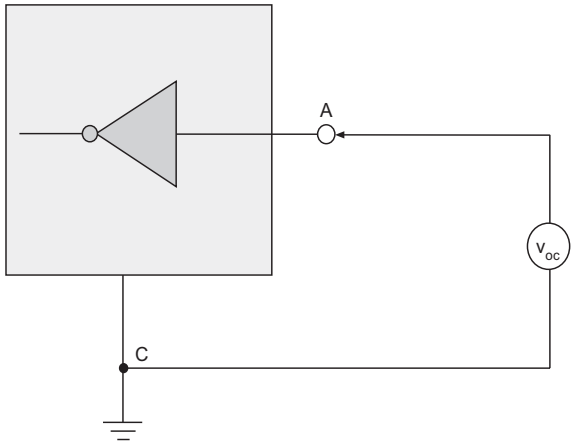


FIGURE 10. V.10 DRIVER OUTPUT OPEN-CIRCUIT VOLTAGE

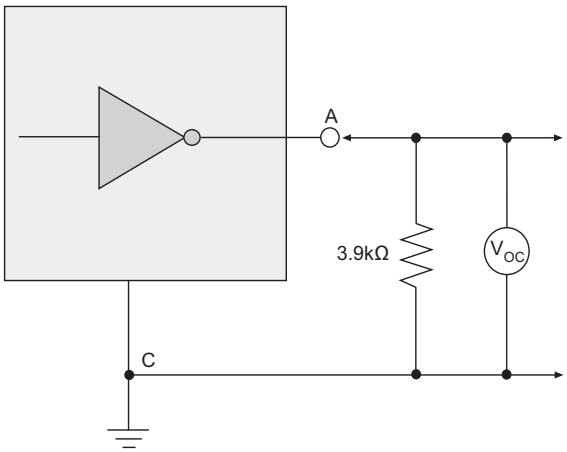


FIGURE 11. V.10 DRIVER OUTPUT TEST TERMINATED VOLTAGE

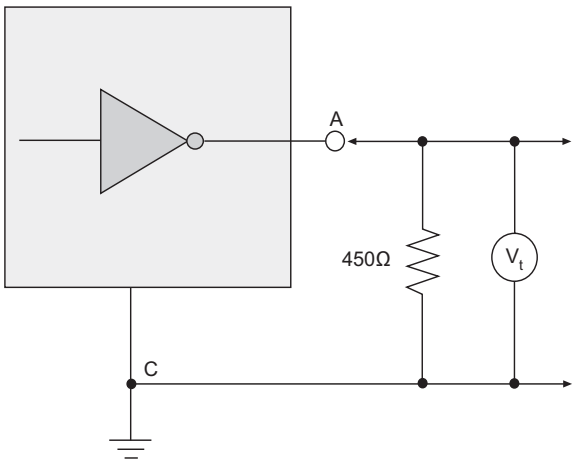


FIGURE 12. V.10 DRIVER OUTPUT SHORT-CIRCUIT CURRENT

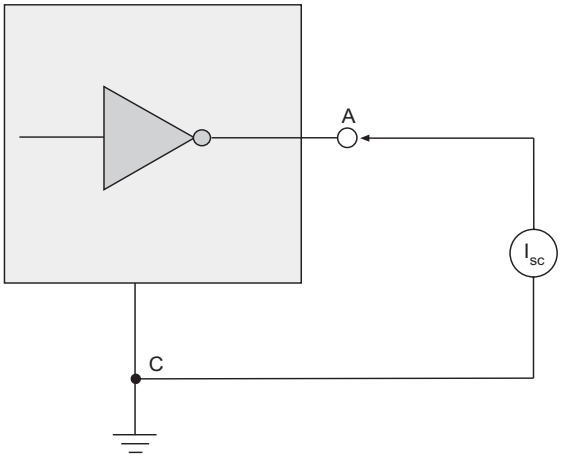


FIGURE 13. V.10 DRIVER OUTPUT POWER-OFF IMPEDANCE

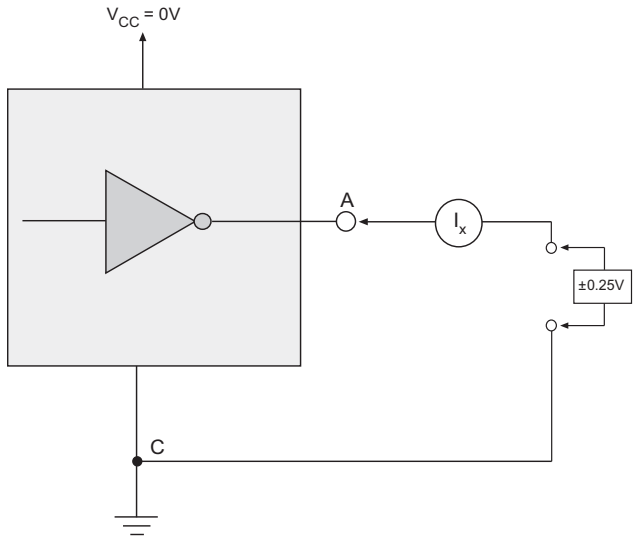


FIGURE 14. V.10 DRIVER OUTPUT TRANSITION TIME

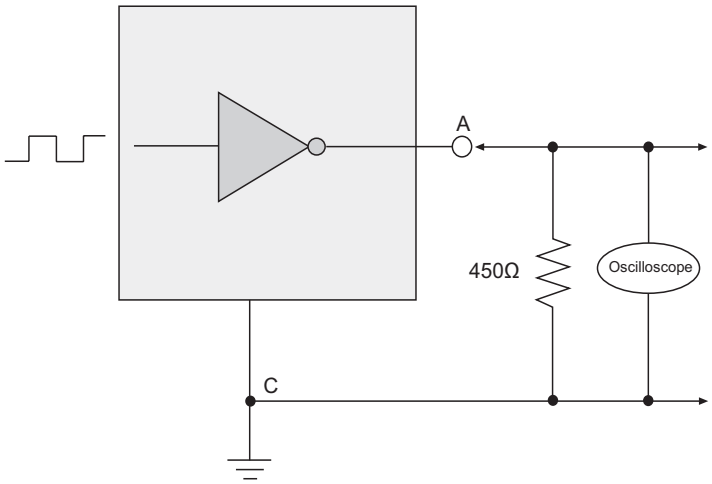


FIGURE 15. V.10 RECEIVER INPUT CURRENT

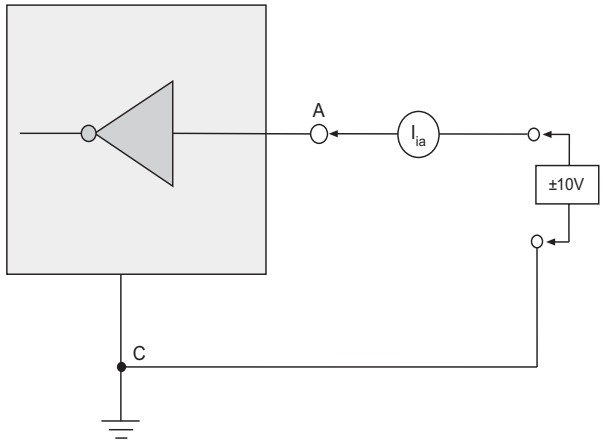


FIGURE 16. V.10 RECEIVER INPUT IV GRAPH

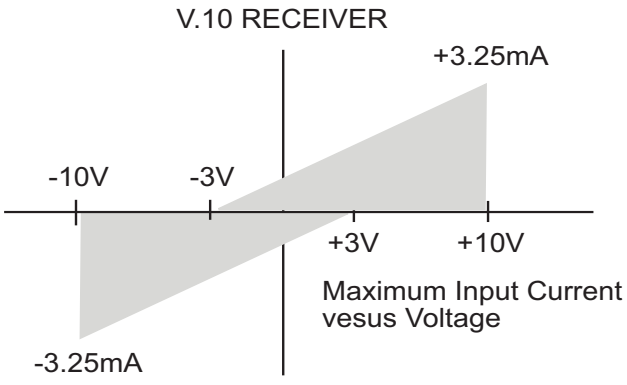


FIGURE 17. V.11 DRIVER OUTPUT TEST TERMINATED VOLTGE

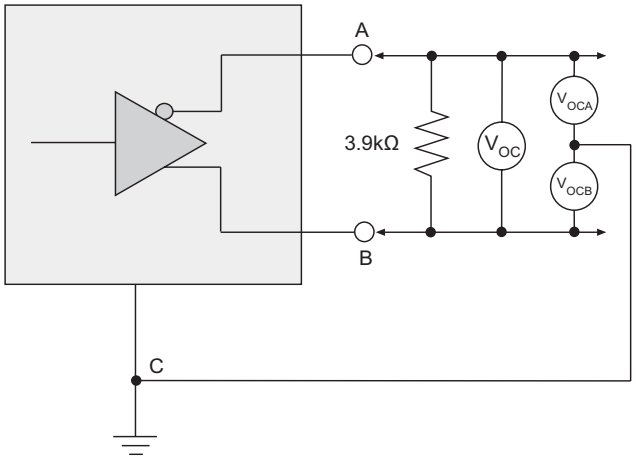


FIGURE 18. V.11 DRIVER OUTPUT TEST TERMINATED VOLTAGE

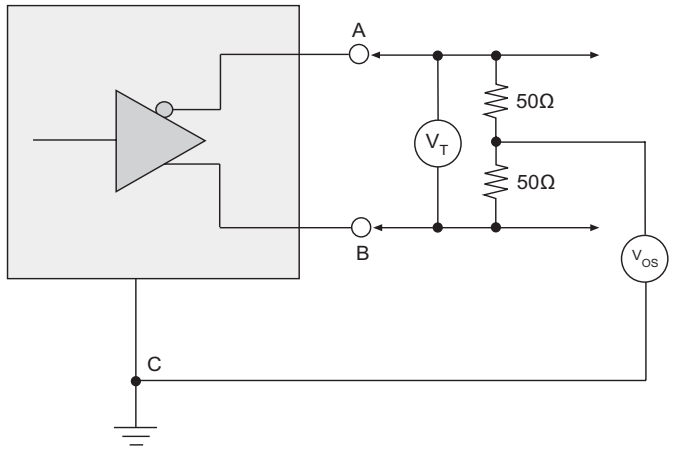


FIGURE 19. V.11 DRIVER OUTPUT SHORT-CIRCUIT CURRENT

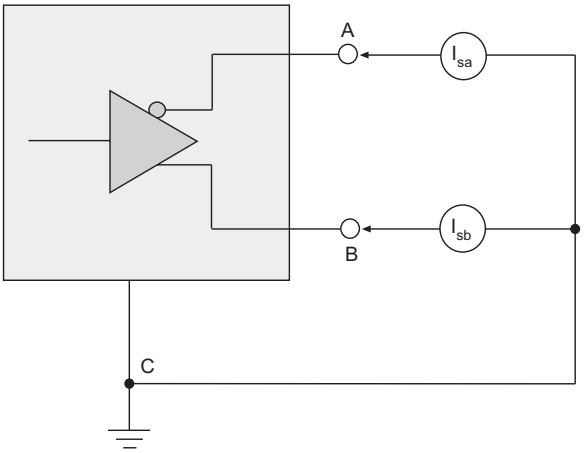


FIGURE 20. V.11 DRIVER OUTPUT POWER-OFF CURRENT

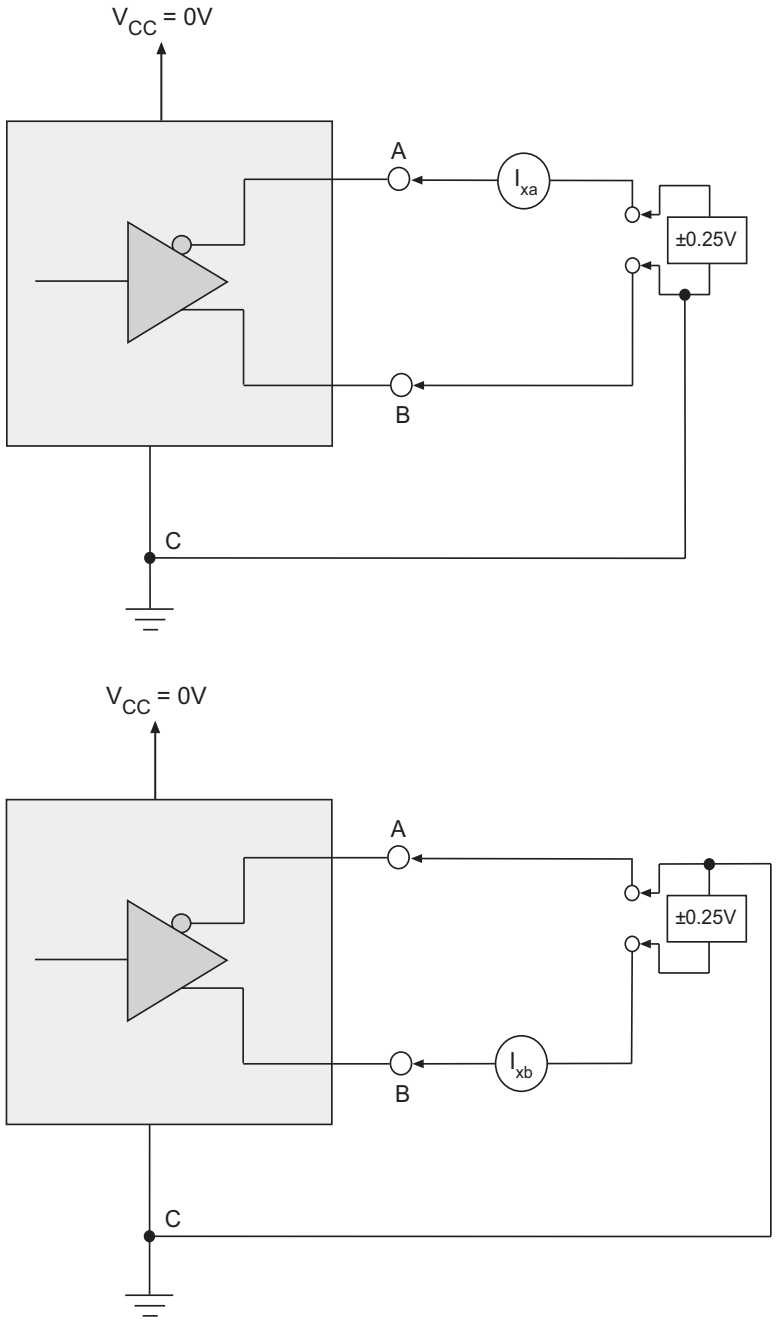


FIGURE 21. V.11 RECEIVER INPUT CURRENT

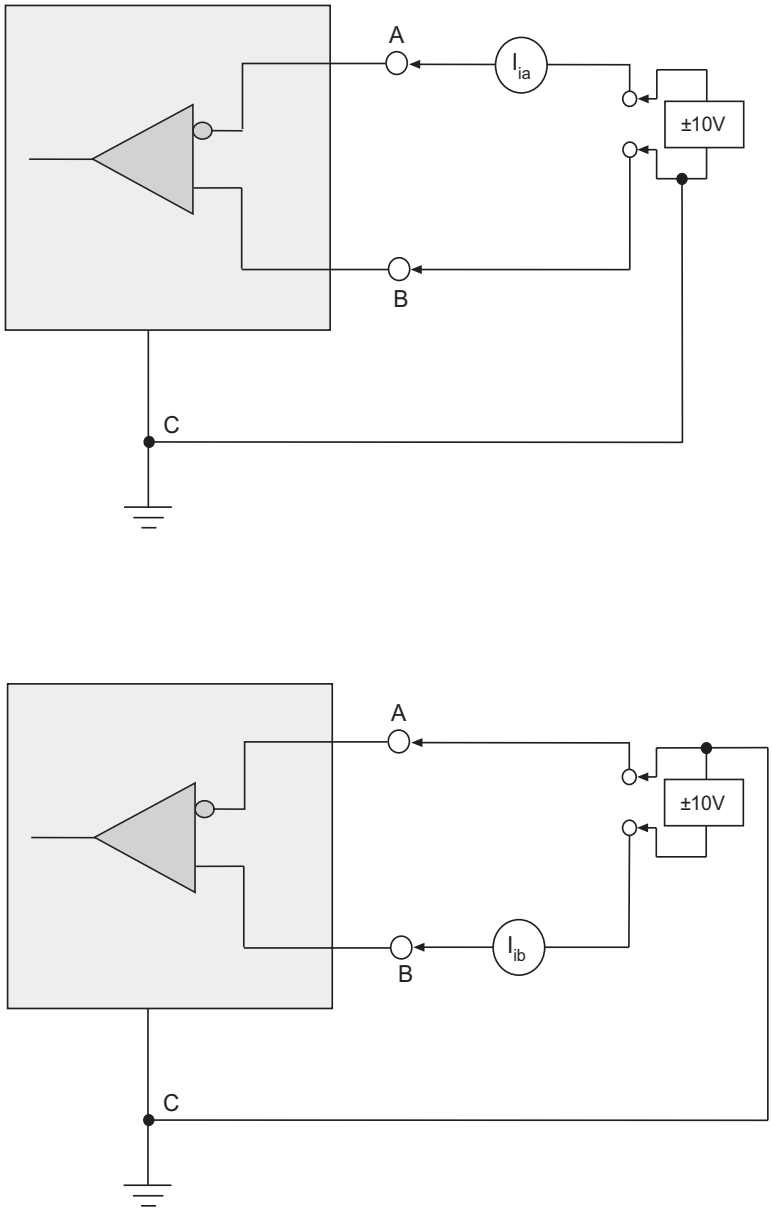


FIGURE 22. V.11 DRIVER OUTPUT RISE/FALL TIME

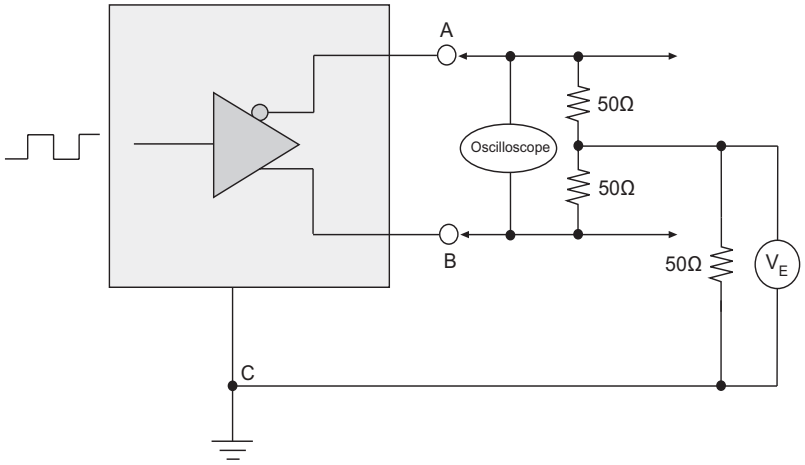


FIGURE 23. V.11 RECEIVER INPUT IV GRAPH

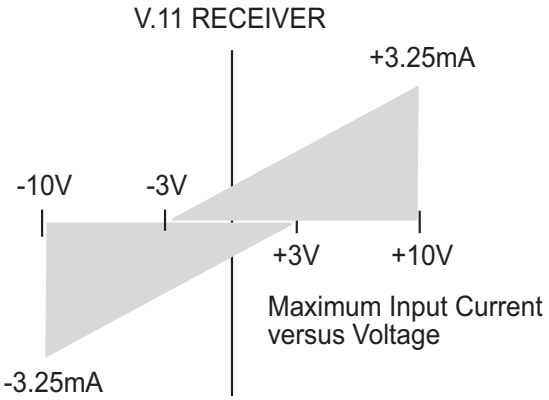
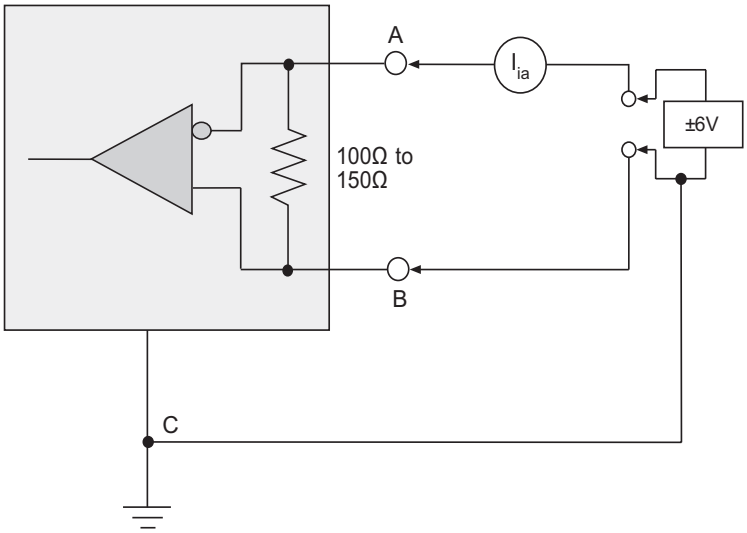


FIGURE 24. V.11 RECEIVER INPUT CURRENT WITH TERMINATION



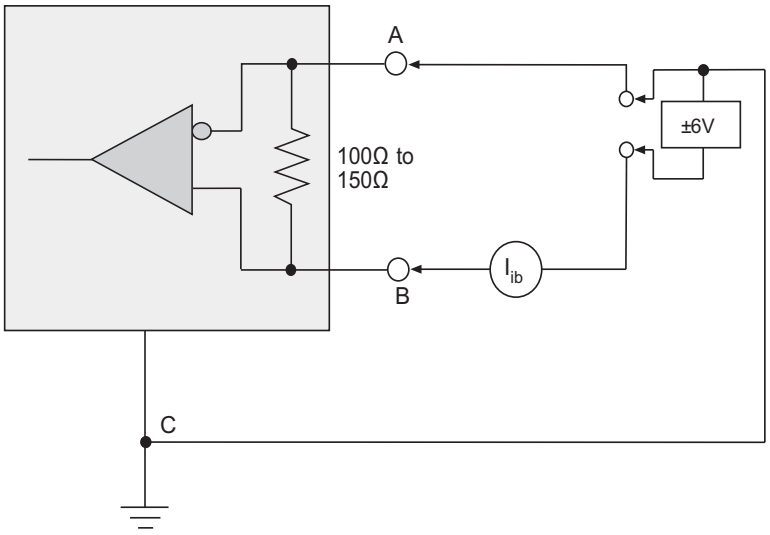


FIGURE 25. V.11 RECEIVER INPUT IV GRAPH WITH TERMINATION

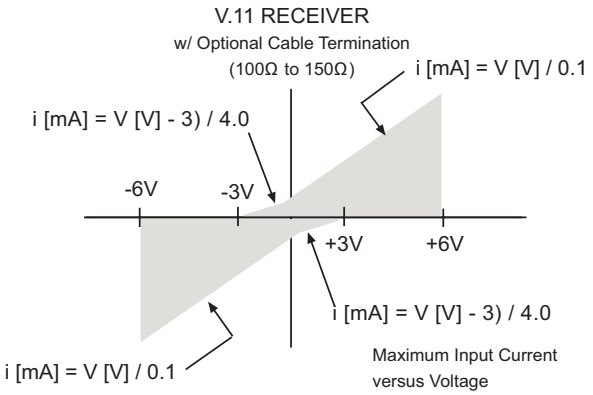


FIGURE 26. V.35 DRIVER OUTPUT TEST TERMINATED VOLTAGE

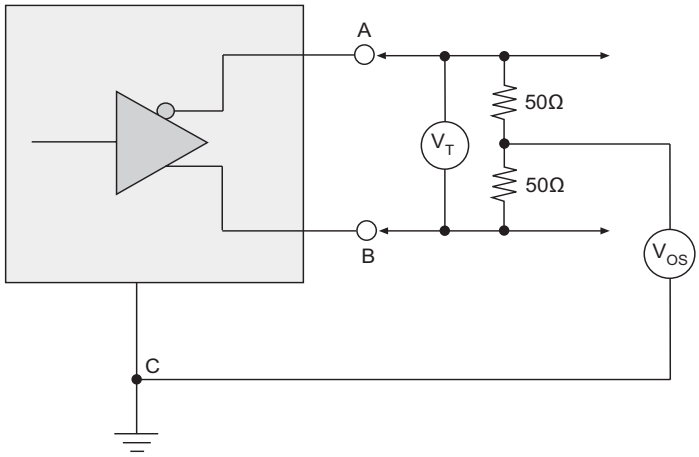


FIGURE 27. V.35 DRIVER OUTPUT SOURCE IMPEDANCE

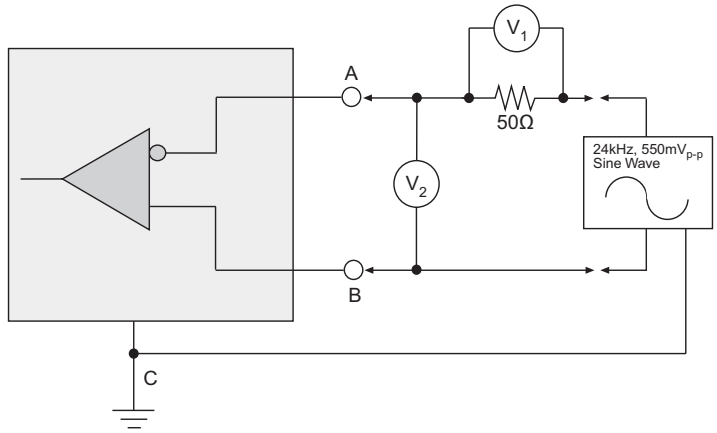


FIGURE 28. V.35 DRIVER OUTPUT SHORT-CIRCUIT IMPEDANCE

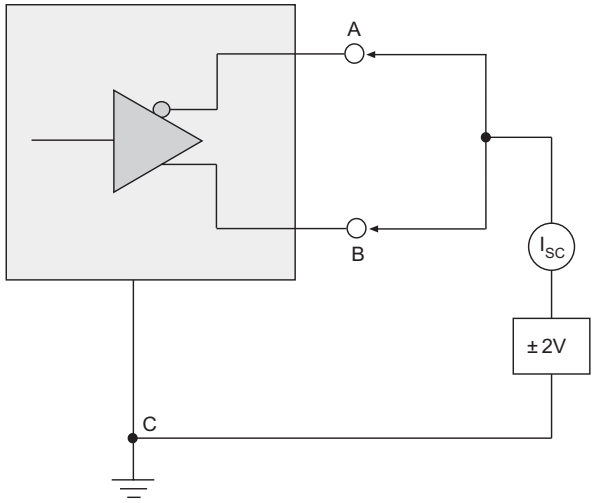


FIGURE 29. V.35 DRIVER OUTPUT RISE/FALL TIME

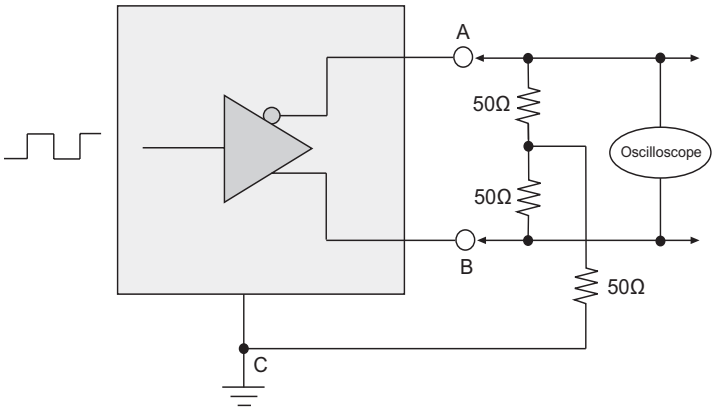


FIGURE 30. V.35 RECEIVER INPUT SOURCE IMPEDANCE

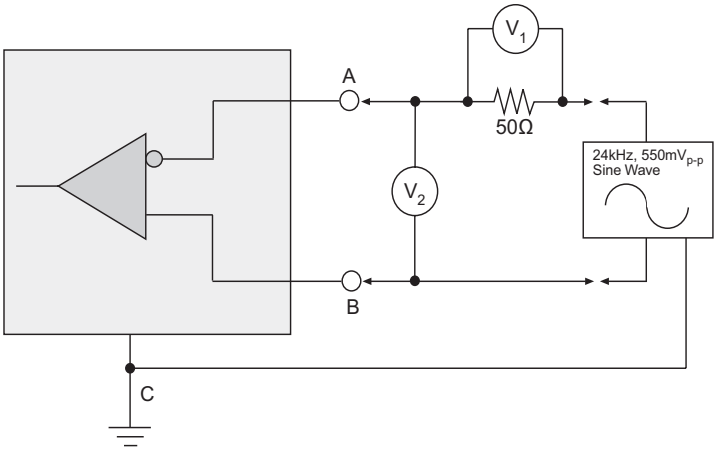


FIGURE 31. V.35 RECEIVER INPUT SHORT-CIRCUIT IMPEDANCE

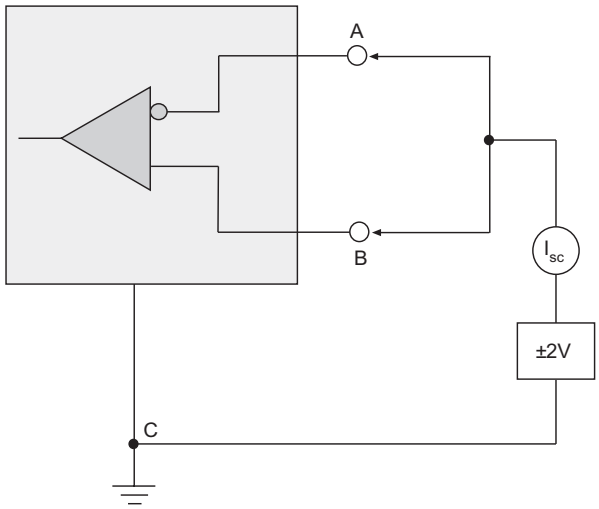


FIGURE 32. DRIVER OUTPUT CURRENT LEAKAGE TEST

Any one of the three conditions for disabling the driver.

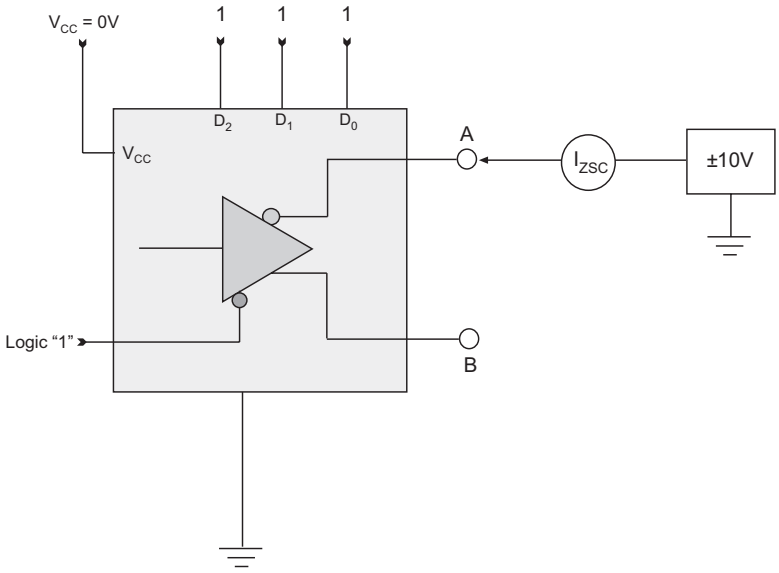


FIGURE 33. DRIVER / RECEIVER TIMING TEST CIRCUIT

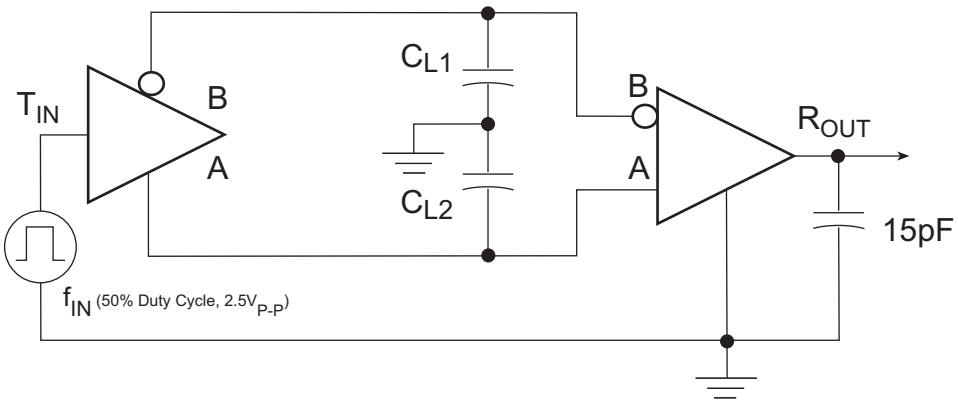


FIGURE 34. DRIVER TIMING TEST LOAD CIRCUIT

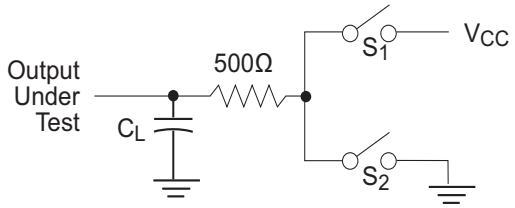


FIGURE 35. RECEIVER TIMING TEST LOAD CIRCUIT

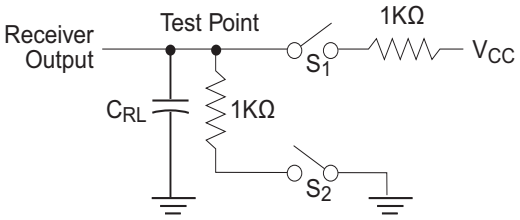
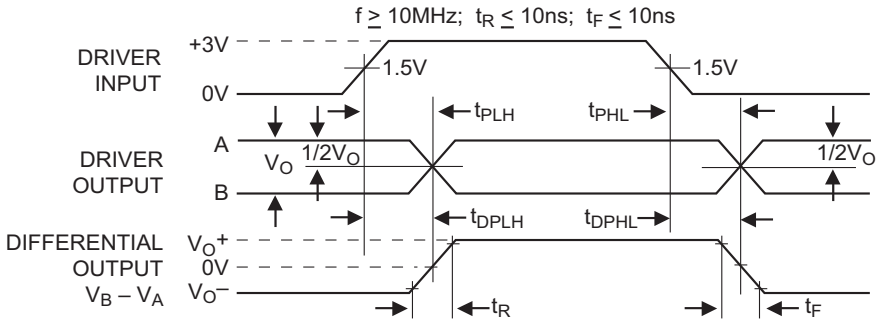


FIGURE 36. DRIVER PROPAGATON DELAYS



$t_{SKEW} = | t_{DPLH} - t_{DPHL} |$

FIGURE 37. DRIVER ENABLE AND DISABLE TIMES

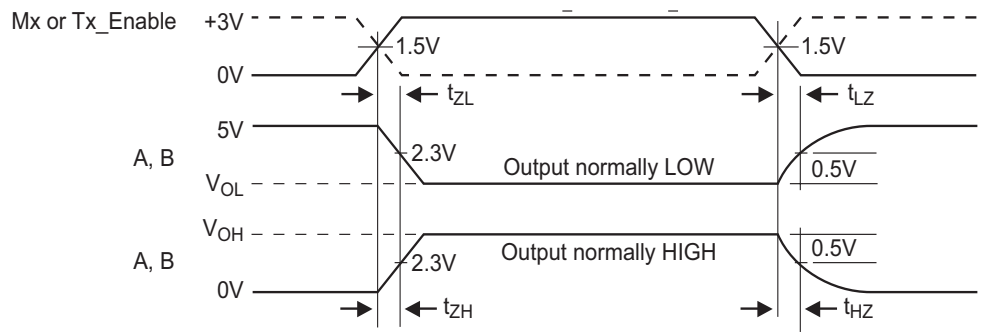


FIGURE 38. RECEIVER PROPAGATION DELAYS

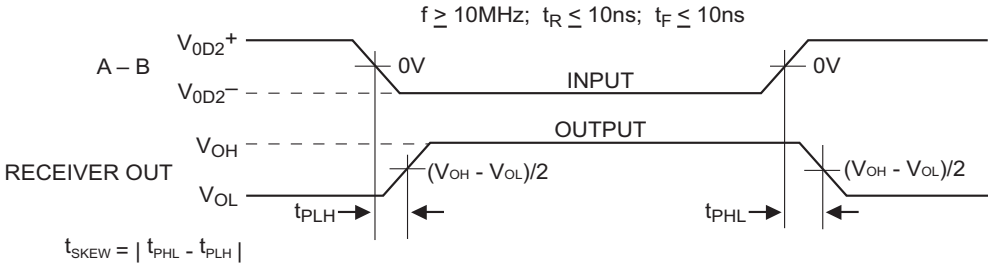


FIGURE 39. RECEIVER ENABLE AND DISABLE TIMES

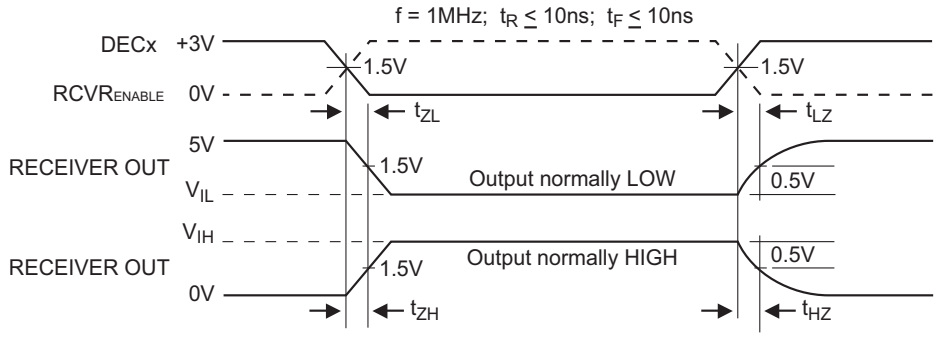


FIGURE 40. V.28 (RS-232) AND V.10 (RS-423) DRIVER ENABLE AND DISABLE TIMES

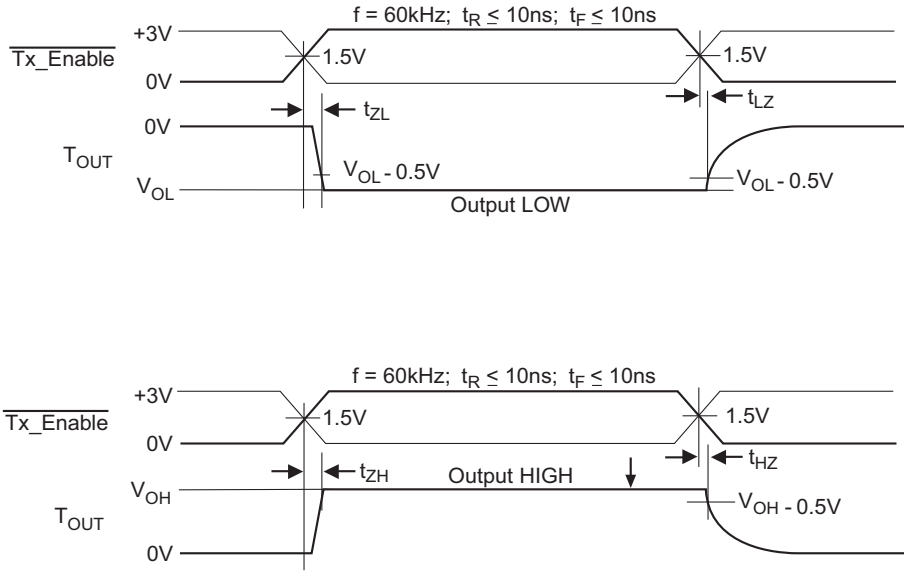


FIGURE 41. TYPICAL V.28 DRIVER OUTPUT WAVEFORM

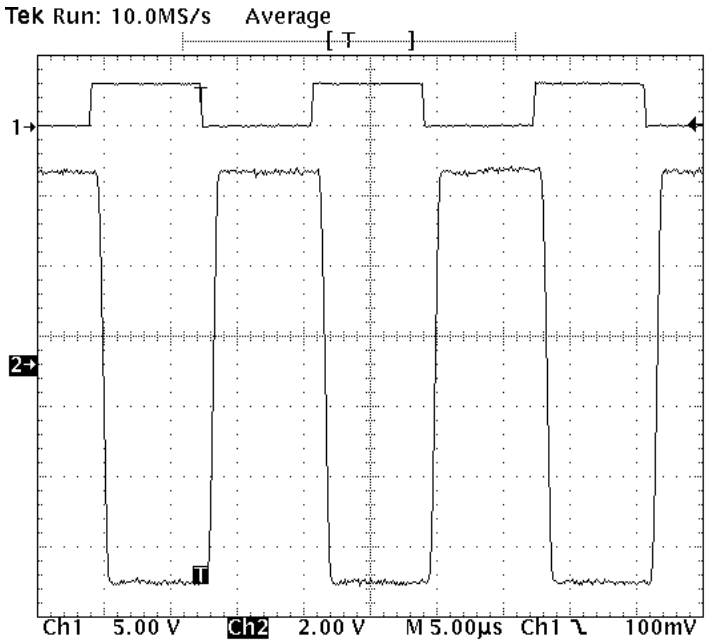


FIGURE 42. TYPICAL V.10 DRIVER OUTPUT WAVEFORM

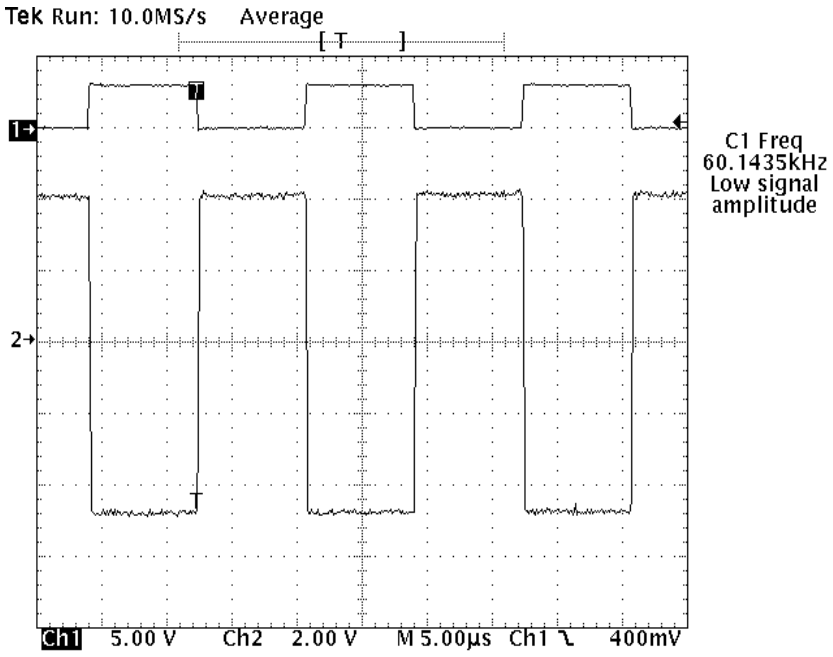


FIGURE 43. TYPICAL V.11 DRIVER OUTPUT WAVEFORM

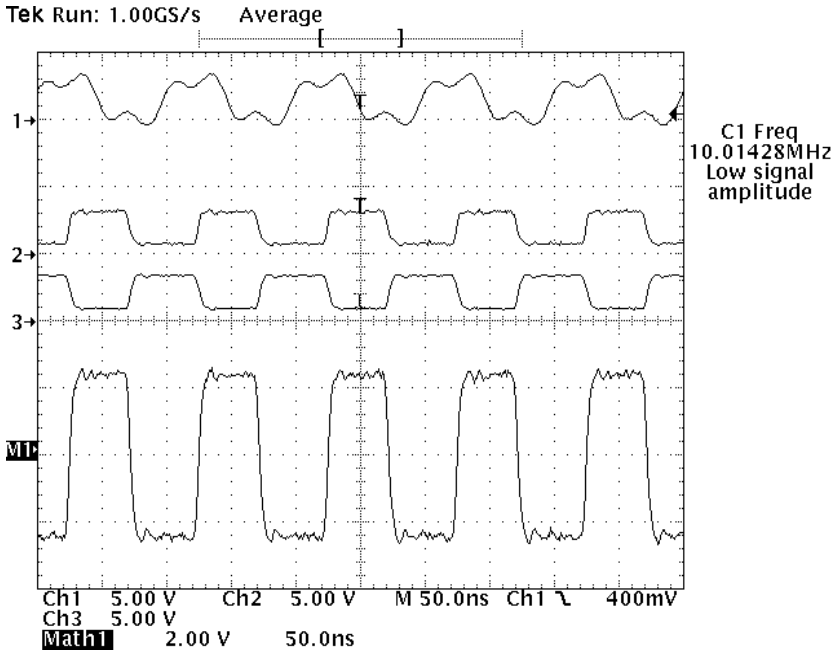


FIGURE 44. TYPICAL V.35 DRIVER OUTPUT WAVEFORM

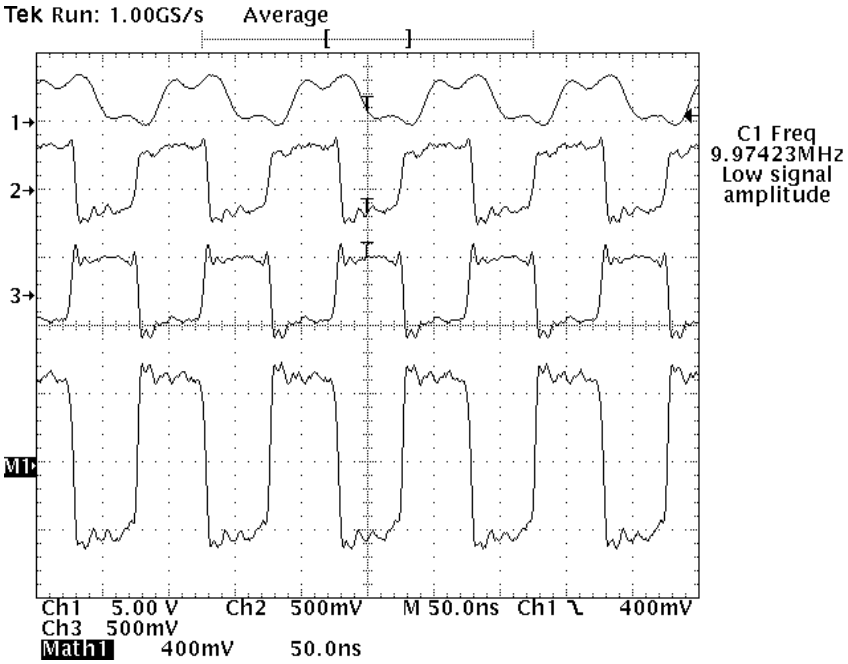


FIGURE 45. FUNCTIONAL DIAGRAM

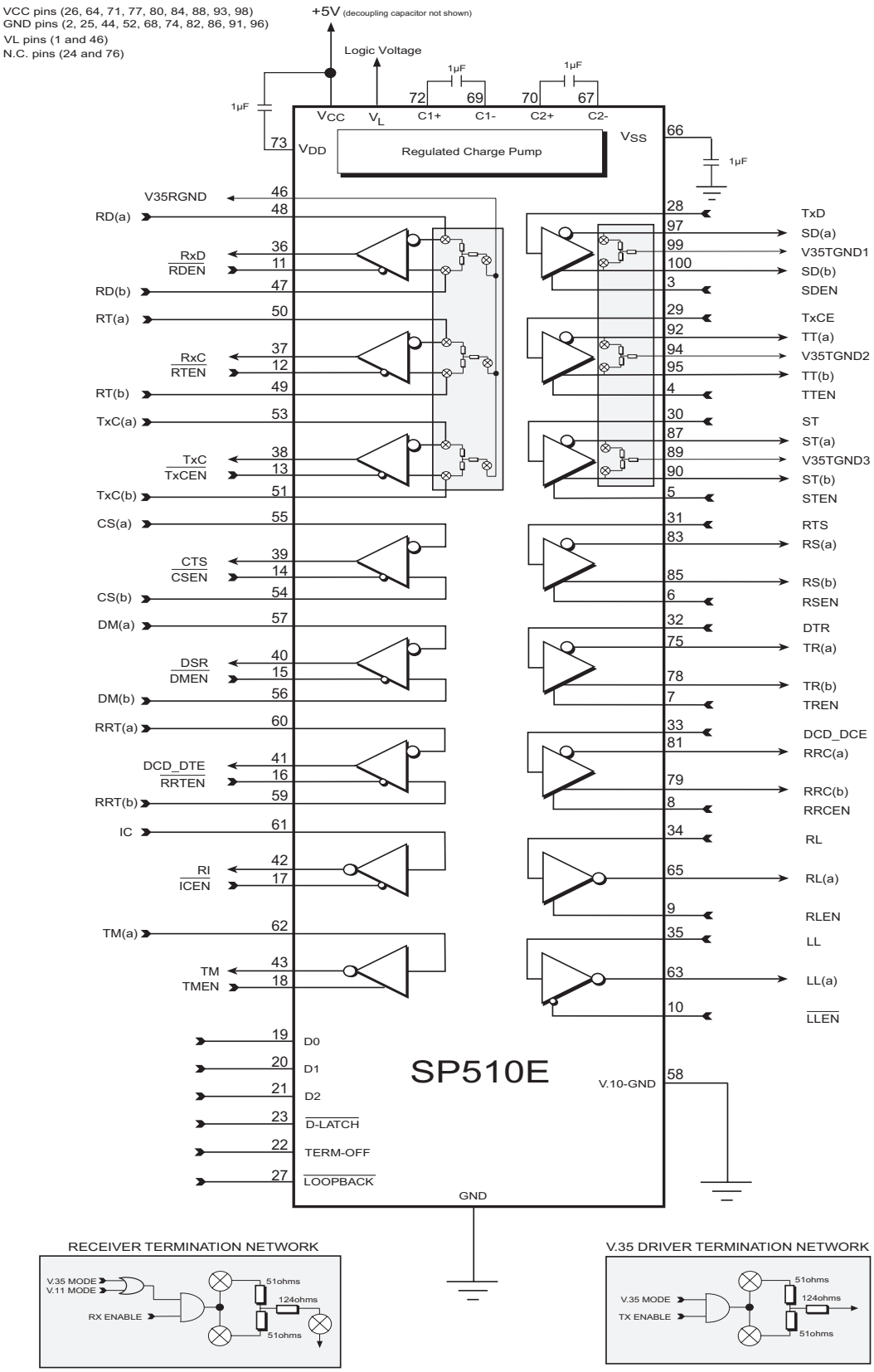


FIGURE 46. SP510E LOOPBACK PATH

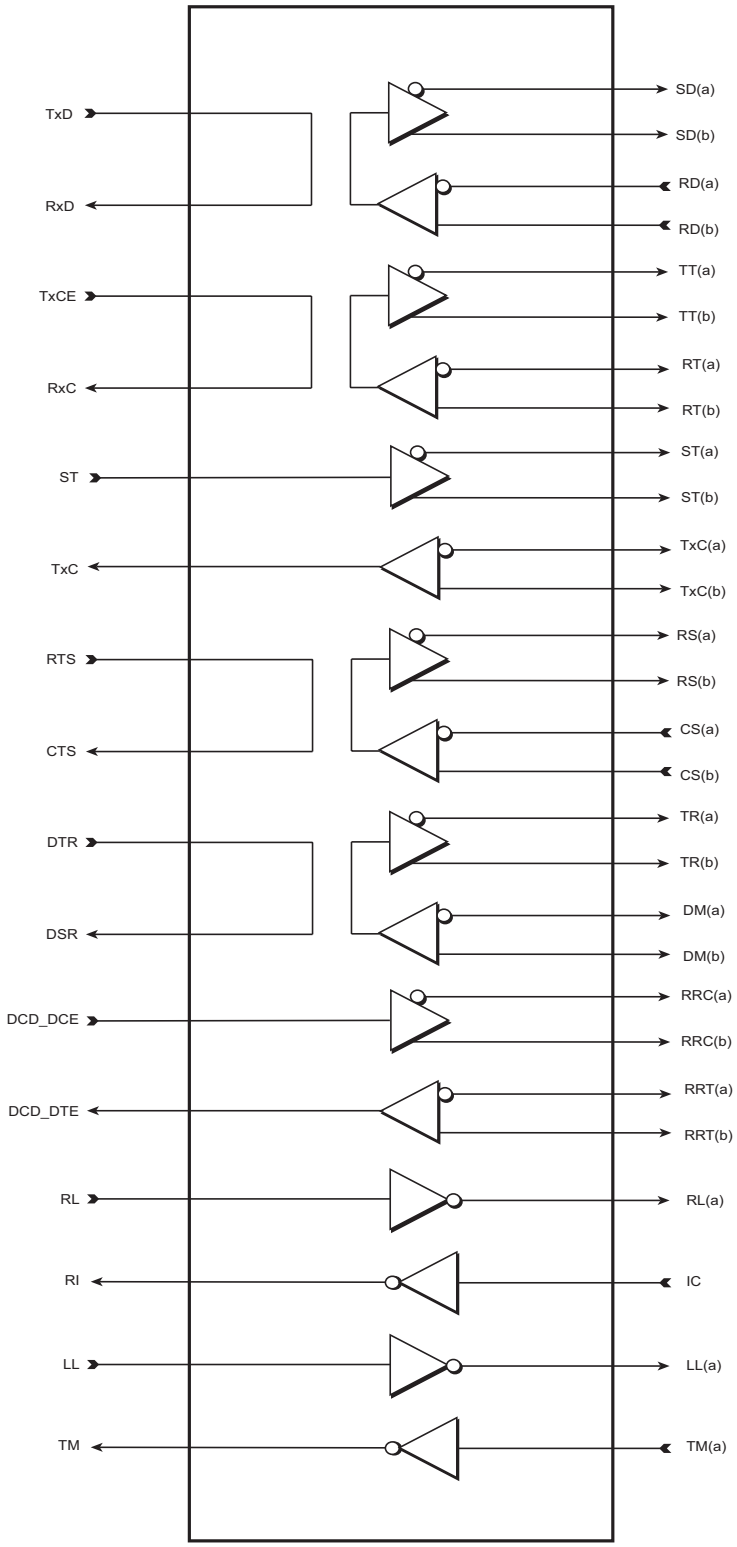
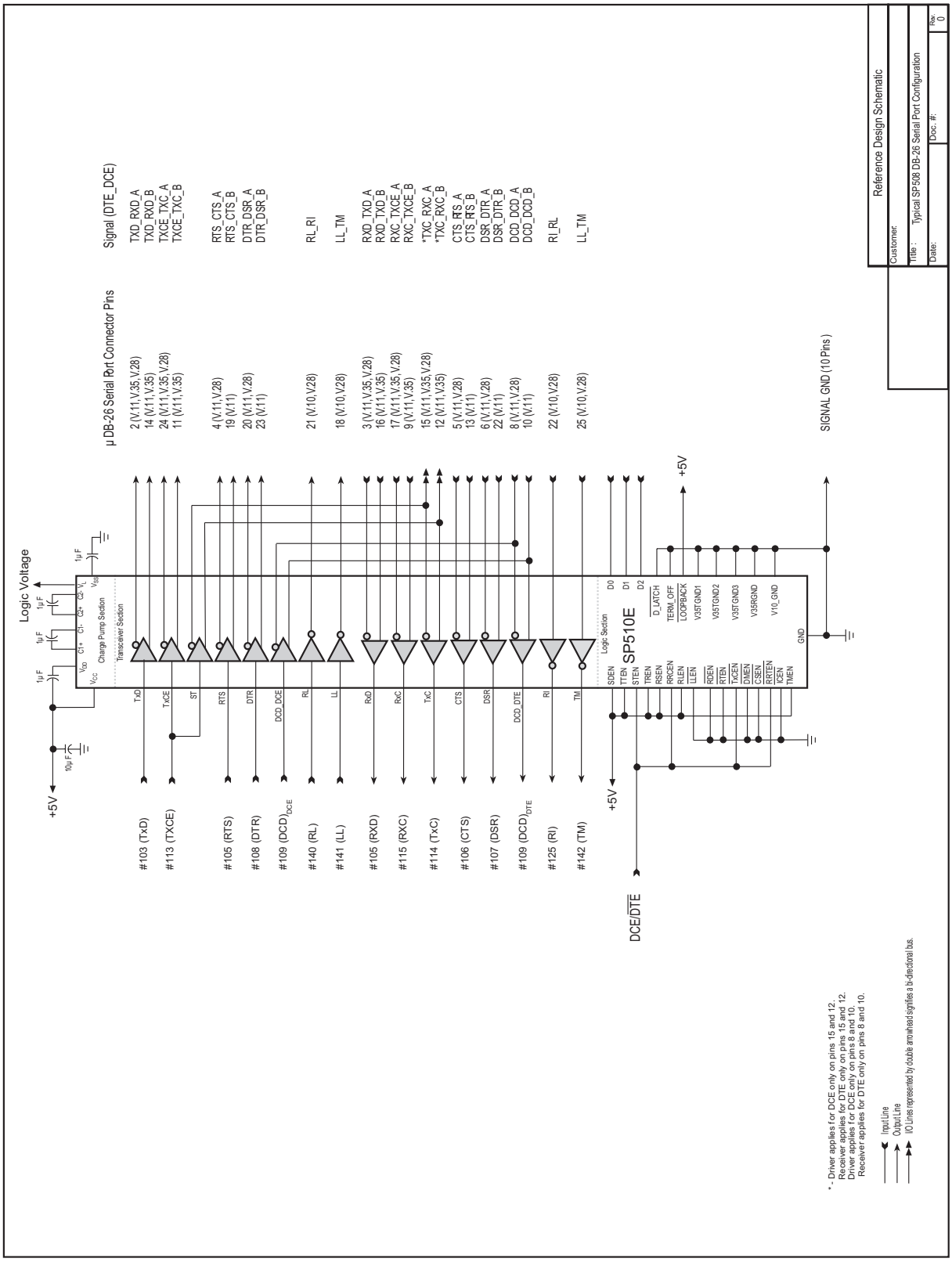


FIGURE 48. TYPICAL CONFIGURATION TO SERIAL PORT CONNECTOR WITH DCE/DTE PROGRAMMABILITY

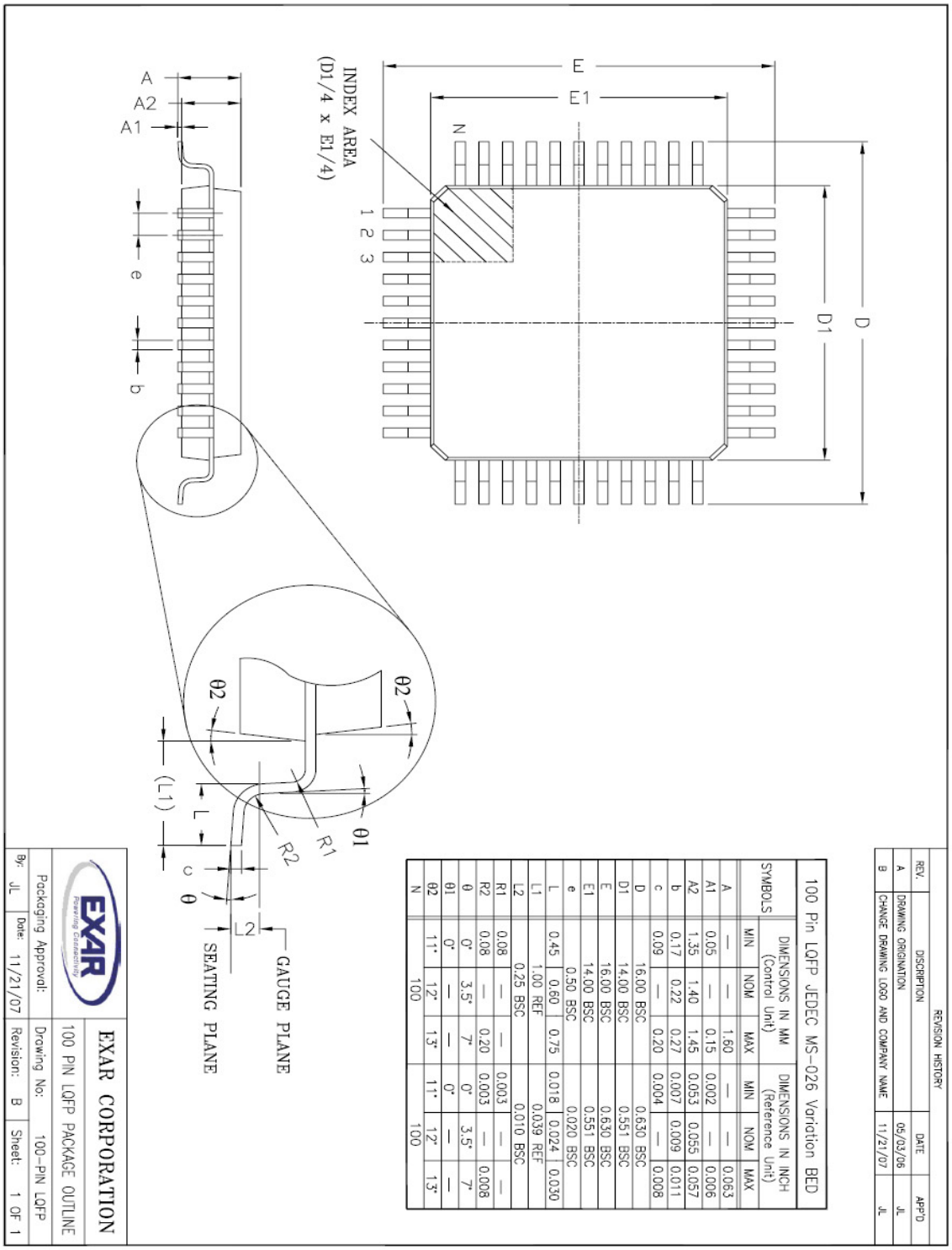


Thermal Considerations

High speed devices like the SP510E dissipate heat during normal operation. Actual power dissipation is a function of the switching frequency and loading. For maximum system performance and reliability designers should ensure sufficient air flow. Other commonly used methods for managing heat include heat sinks for higher powered devices, forced air flow (fans) and lower density board stuffing.

PCB Design

The use of multi layer printed circuit boards is recommended to provide both a better ground plane and a thermal path for heat dissipation. If possible, the ground plane should face the bottom of the package to form the thermal conduction plane. Two-sided printed circuit boards may be used where board dimensions and package count are small, but multi-layer boards allow for improved signal routing as well as improved signal integrity. A multi-layer board allows microstrip line techniques for high speed signal interconnections when the high speed signal lines on the inner layers.



REVISION HISTORY

REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	05/03/06	JL
B	CHANGE DRAWING LOGO AND COMPANY NAME	11/21/07	JL

100 Pin LQFP JEDEC MS-026 Variation BED

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.09	—	0.20	0.004	—	0.008
D	16.00 BSC			0.630 BSC		
D1	14.00 BSC			0.551 BSC		
E	16.00 BSC			0.630 BSC		
E1	14.00 BSC			0.551 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
L2	0.25 BSC			0.010 BSC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
N	100			100		

EXAR CORPORATION

100 PIN LQFP PACKAGE OUTLINE

Packaging Approval:	Drawing No: 100-PIN LQFP
By: JL Date: 11/21/07	Revision: B Sheet: 1 OF 1

REVISION HISTORY

DATE	REVISION	DESCRIPTION
July 2012	1.0.0	Production Release

NOTICE

Datasheet July 2012.

Send your UART technical inquiry with technical details to hotline: SerialTechSupport@exar.com.