



# XRD87L75

## Low-Voltage CMOS 8-Bit High-Speed Analog-to-Digital Converter

April 2==2 1

### FEATURES

- 8-Bit Resolution
- Up to 10MHz Sampling Rate
- Internal S/H Function
- Single Supply: 3.3V
- $V_{IN}$  DC Range: 0V to  $V_{DD}$
- $V_{REF}$  DC Range: 1V to  $V_{DD}$
- Low Power: 25mW typ. (excluding reference)
- Latch-Up Free

- ESD Protection: 2000V Minimum
- Small 20-Pin SOIC/SSOP Packages

### APPLICATIONS

- Digital Color Copiers
- Cellular Telephones
- CCD-Based Systems
- Hardware Scanners
- Video Capture Boards

### GENERAL DESCRIPTION

The XRD87L75 is an 8-bit Analog-to-Digital Converter in a small 20-pin SOIC/SSOP package. Designed using an advanced 3.3V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

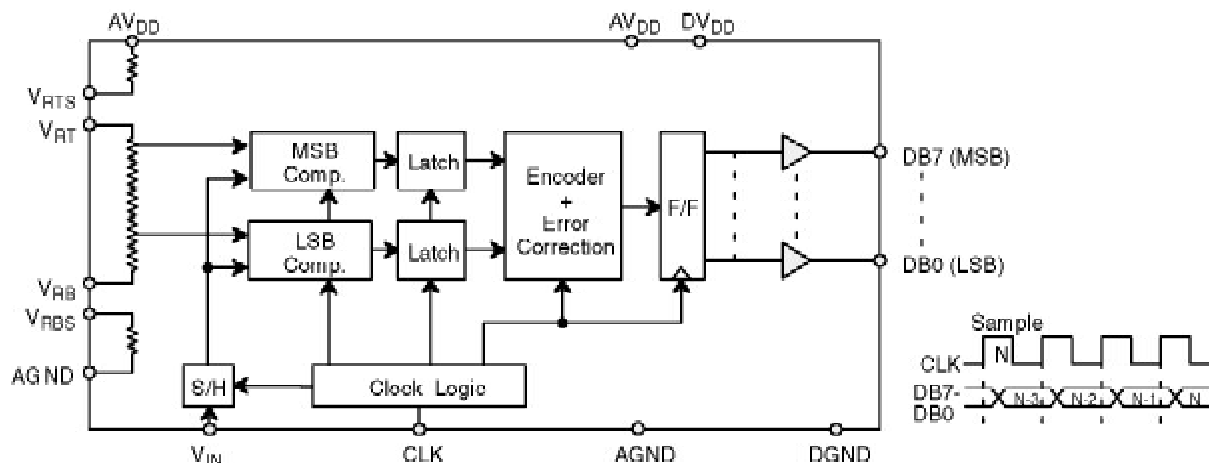
This device uses a two-step flash architecture to maintain low power consumption at high conversion rates. The input circuitry of the XRD87L75 includes an on-chip S/H function and allows the user to digitize analog input signals between AGND and  $AV_{DD}$ . Careful design and chip layout have achieved a low analog input capacitance. This reduces “kickback” and eases the requirements of the buffer/amplifier used to drive the XRD87L75.

The designer can choose the internally generated reference voltages by connecting  $V_{RB}$  to  $V_{RBS}$  and  $V_{RT}$  to  $V_{RTS}$ , or provide external reference voltages to the  $V_{RB}$  and  $V_{RT}$  pins. The internal reference generates 0.4V at  $V_{RB}$  and 1.72V at  $V_{RT}$ . Providing external reference voltages allows easy interface to any input signal range between GND and  $V_{DD}$ . This also allows the system to adjust these voltages to cancel zero scale and full scale errors, or to change the input range as needed.

The device operates from a single +3.3V supply. Power consumption is 25mW at  $F_s = 6$ MHz.

Specified for operation over the commercial / industrial (-40 to +85°C) temperature range, the XRD87L75 is available in Surface Mount (SOIC), Shrink Small Outline (SSOP) and Plastic Dual-In-line (PDIP) Packages.

### SIMPLIFIED BLOCK AND TIMING DIAGRAM



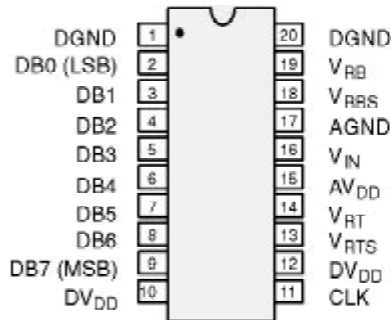
Rev. 1.00

## ORDERING INFORMATION

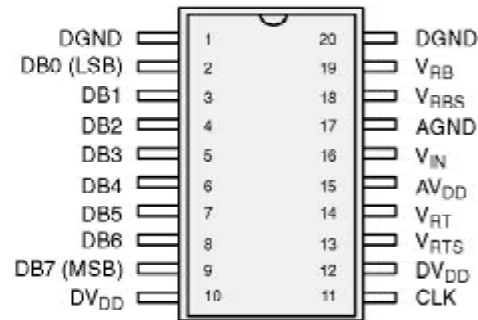
Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
SOIC	-40 to +85°C	XRD87L75AID	+/-0.5	+/-1.5
PDIP	-40 to +85°C	XRD87L75AIP	+/-0.5	+/-1.5
SSOP	-40 to +85°C	XRD87L75AIU	+/-0.5	+/-1.5

## PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20-Pin PDIP (300 MIL) - P20



20-Pin SOIC (Jedec, 300 MIL) - D20  
20-Pin SSOP (5.3mm) - U20

## PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION	PIN NO.	NAME	DESCRIPTION
1	DGND	Digital Ground	11	CLK	Sample Clock
2	DB0	Data Output Bit 0 (LSB)	12	DV <sub>DD</sub>	Digital Power Supply
3	DB1	Data Output Bit 1	13	V <sub>RTS</sub>	Generates 1.72V if tied to V <sub>RT</sub>
4	DB2	Data Output Bit 2	14	V <sub>RT</sub>	Top Reference
5	DB3	Data Output Bit 3	15	AV <sub>DD</sub>	Analog Power Supply
6	DB4	Data Output Bit 4	16	V <sub>IN</sub>	Analog Input
7	DB5	Data Output Bit 5	17	AGND	Analog Ground
8	DB6	Data Output Bit 6	18	V <sub>RBS</sub>	Generates 0.4V if tied to V <sub>RB</sub>
9	DB7	Data Output Bit 7 (MSB)	19	V <sub>RB</sub>	Bottom Reference
10	DV <sub>DD</sub>	Digital Power Supply	20	DGND	Digital Ground

## ELECTRICAL CHARACTERISTICS TABLE

UNLESS OTHERWISE SPECIFIED:  $AV_{DD} = DV_{DD} = 3.3V$ ,  $FS = 6MHz$  (50% DUTY CYCLE),  
 $V_{RT} = 2.5V$ ,  $V_{RB} = 0.5V$ ,  $T_A = 25^\circ C$

Parameter	Symbol	25°C			Units	Test Conditions/Comments
		Min	Typ	Max		
<b>KEY FEATURES</b>						
Resolution		8			Bits	
Sampling Rate	FS	0.1	6	10	MHz	
<b>ACCURACY</b>						
Differential Non-Linearity	DNL		+/-0.3	+/-0.5	LSB	Best Fit Line (Max INL – Min INL)/2
Integral Non-Linearity	INL		+/-0.75	+/-1.5	LSB	
Zero Scale Error	EZS		+3		LSB	
Full Scale Error	EFS		-2		LSB	
<b>REFERENCE VOLTAGES</b>						
Positive Ref. Voltage	$V_{RT}$		2.5	$AV_{DD}$	V	$V_{REF} = V_{RT} - V_{RB}$
Negative Ref. Voltage	$V_{RB}$	AGND	0.5		V	
Differential Ref. Voltage <sup>3</sup>	$V_{REF}$	1.0		$AV_{DD}$	V	
Ladder Resistance	$R_L$	245	350	550	$\Omega$	
Ladder Temp. Coefficient	$R_{TCO}$		2000		ppm/°C	
Self Bias 1						
Short $V_{RB}$ and $V_{RBS}$	$V_{RB}$		0.4		V	
Short $V_{RT}$ and $V_{RTS}$	$V_{RT} - V_{RB}$		1.72		V	
Self Bias 2						
$V_{RB} = AGND$ , Short $V_{RT}$ and $V_{RTS}$	$V_{RT}$		1.5		V	
<b>ANALOG INPUT</b>						
Input Bandwidth (-1 dB) <sup>2,4</sup>	BW		50		MHz	
Input Voltage Range	$V_{IN}$	$V_{RB}$		$V_{RT}$	V	
Input Capacitance <sup>5</sup>	$C_{IN}$		16		pF	
Aperture Delay <sup>2</sup>	$t_{AP}$		4		ns	
<b>DIGITAL INPUTS</b>						
Logical "1" Voltage	$V_{IH}$	2.5			V	$V_{IN} = DGND$ to $DV_{DD}$
Logical "0" Voltage	$V_{IL}$			0.5	V	
DC Leakage Current <sup>6</sup>	$I_{IN}$				$\mu A$	
CLK			5		$\mu A$	
Input Capacitance			5		pF	
Clock Timing ( See Figure 1.) <sup>7</sup>						
Clock Period	1/FS	100	166		ns	
High Pulse Width	$t_{PWH}$	50	83		ns	
Low Pulse Width	$t_{PWL}$	50	83		ns	
<b>DIGITAL OUTPUTS</b>						
Logical "1" Voltage	$V_{OH}$	2.5			V	$C_{OUT} = 15 pF$ $I_{LOAD} = 1 mA$
Logical "0" Voltage	$V_{OL}$			0.5	V	
Data Valid Delay <sup>8</sup>	$t_{DL}$		12		ns	

## ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

UNLESS OTHERWISE SPECIFIED:  $AV_{DD} = DV_{DD} = 3.3V$ ,  $FS = 6MHz$  (50% DUTY CYCLE),  
 $V_{RT} = 2.5V$ ,  $V_{RB} = 0.5V$ ,  $T_A = 25^\circ C$

Parameter	Symbol	25°C			Units	Test Conditions/Comments
		Min	Typ	Max		
<b>ACPARAMETERS</b>						
Differential Gain Error	$d_G$		2		%	FS = 4 x NTSC
Differential Phase Error	$d_{PH}$		1		Degree	FS = 4 x NTSC
<b>POWERSUPPLIES</b>						
Operating Voltage ( $AV_{DD}$ , $DV_{DD}$ ) <sup>9</sup>	$V_{DD}$	3	3.3	3.6	V	
Current (AGND + DGND)	$I_{DD}$		8	12	mA	Does not include ref. current

### NOTES

- The difference between the measured and the ideal code width ( $V_{REF}/256$ ) is the DNL error (Figure 3). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (Figure 4). Accuracy is a function of the sampling rate (FS).
- Guaranteed, not tested.
- Specified values guarantee functionality. Refer to other parameters for accuracy.
- 1dB bandwidth is a measure of performance of the A/D input stage (S/H + amplifier). Refer to other parameters for accuracy within the specified bandwidth.
- See  $V_{IN}$  input equivalent circuit (Figure 5). Switched capacitor analog input requires driver with low output resistance.
- All inputs have diodes to  $DV_{DD}$  and DGND. Input DC currents will not exceed specified limits for any input voltage between DGND and  $DV_{DD}$ .
- $t_R$ ,  $t_F$  should be limited to >5ns for best results.
- Depends on the RC load connected to the output pin.
- AGND & DGND pins are connected through the silicon substrate. Connect together at the package and to the analog ground plane.

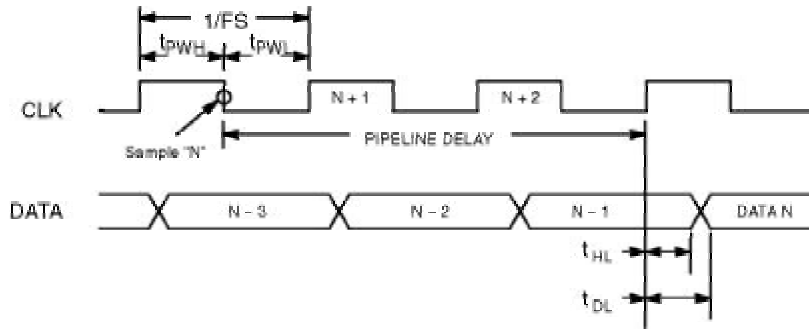
Specifications are subject to change without notice

## ABSOLUTE MAXIMUM RATINGS ( $T_A = +25^\circ C$ unless otherwise noted)<sup>1, 2, 3</sup>

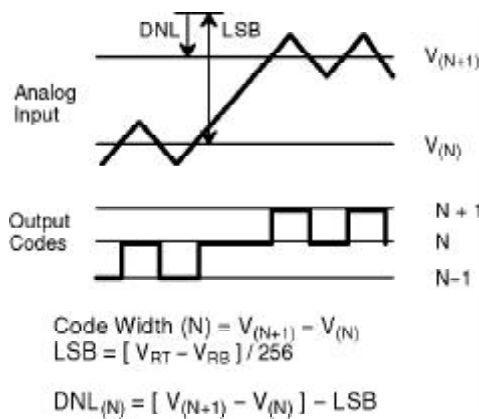
$V_{DD}$ to GND .....	5.5V	Storage Temperature .....	-65 to +150°C
$V_{RT}$ & $V_{RB}$ .....	$V_{DD} +0.5$ to GND -0.5V	Lead Temperature (Soldering 10 seconds) ...	+300°C
$V_{IN}$ .....	$V_{DD} +0.5$ to GND -0.5V	Package Power Dissipation Rating @ 75°C	
All Inputs .....	$V_{DD} +0.5$ to GND -0.5V	PDIP, SOIC, SSOP .....	650mW
All Outputs .....	$V_{DD} +0.5$ to GND -0.5V	Derates above 75°C .....	9mW/°C

### NOTES:

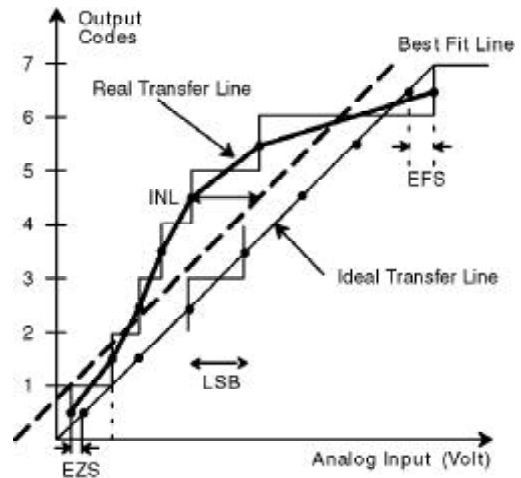
- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100ms.
- $V_{DD}$  refers to  $AV_{DD}$  and  $DV_{DD}$ . GND refers to AGND and DGND.



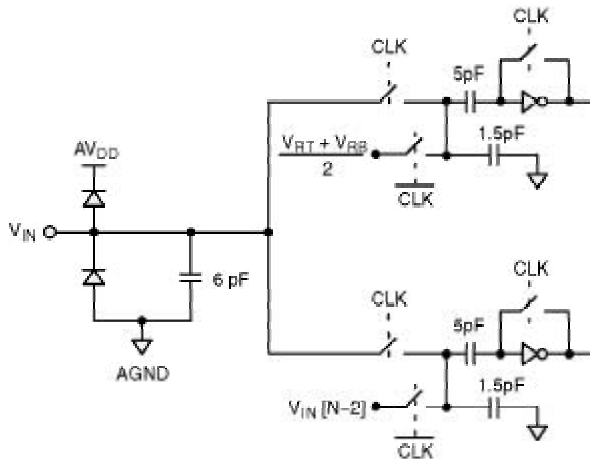
**Figure 1. XRD87L75 Timing Diagram**



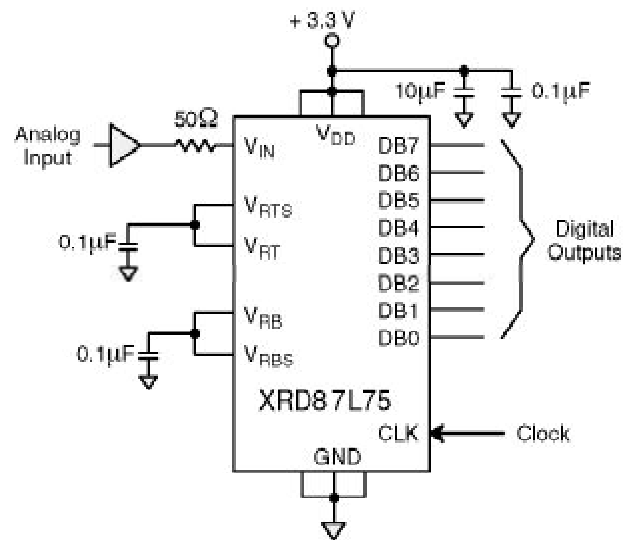
**Figure 2. DNL Measurement**



**Figure 3. INL Error Calculation**



**Figure 4. Equivalent Input Circuit**



**Figure 5. Typical Circuit Connections**

## APPLICATION NOTES

Signals should not exceed  $AV_{DD} + 0.5V$  or go below  $AGND - 0.5V$  or  $DV_{DD} + 0.5V$  or  $DGND - 0.5V$ . All pins have internal protection diodes that will protect them from short transients ( $< 100\mu s$ ) outside the supply range.

$AGND$  and  $DGND$  pins are connected internally through the P-substrate. DC voltage differences between these pins will cause undesirable internal substrate currents.

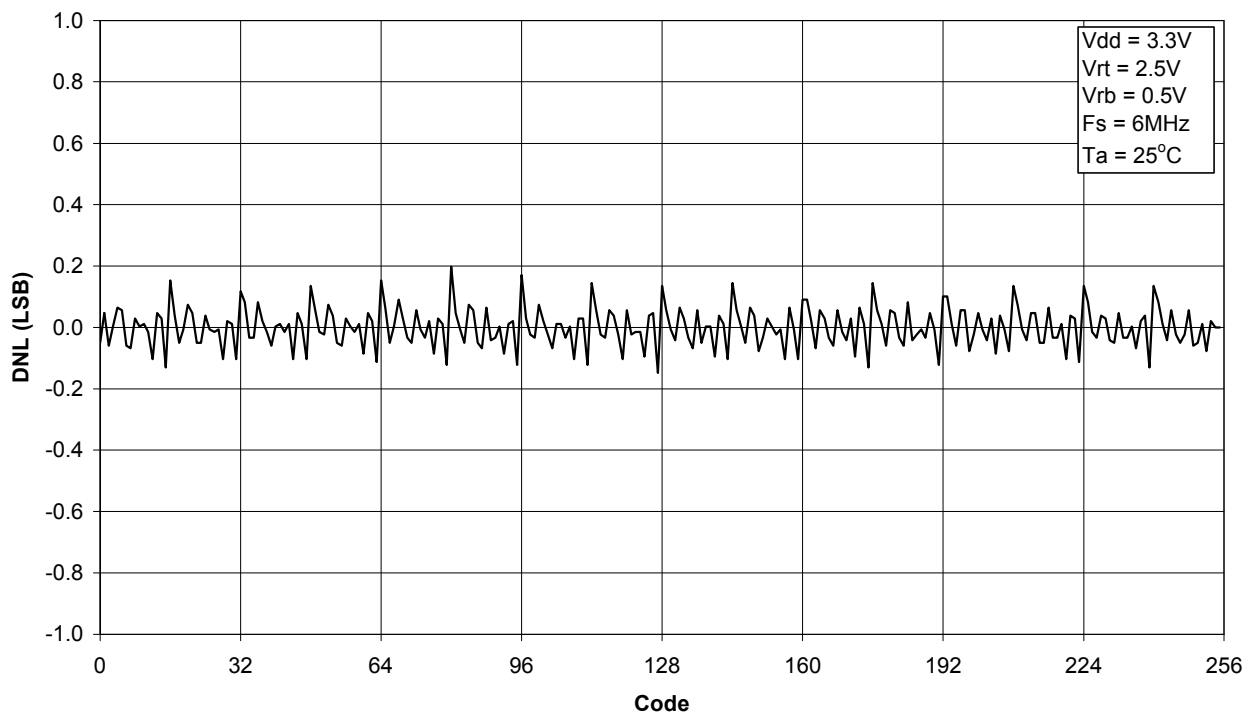
The power supply ( $AV_{DD}$ ) and reference voltage ( $V_{RT}$  &  $V_{RB}$ ) pins should be decoupled with  $0.1\mu F$  and  $10\mu F$  capacitors to  $AGND$ , placed as close to the chip as possible.

The digital outputs should not drive long wires or buses. The capacitive coupling and reflections will contribute noise to the conversion.

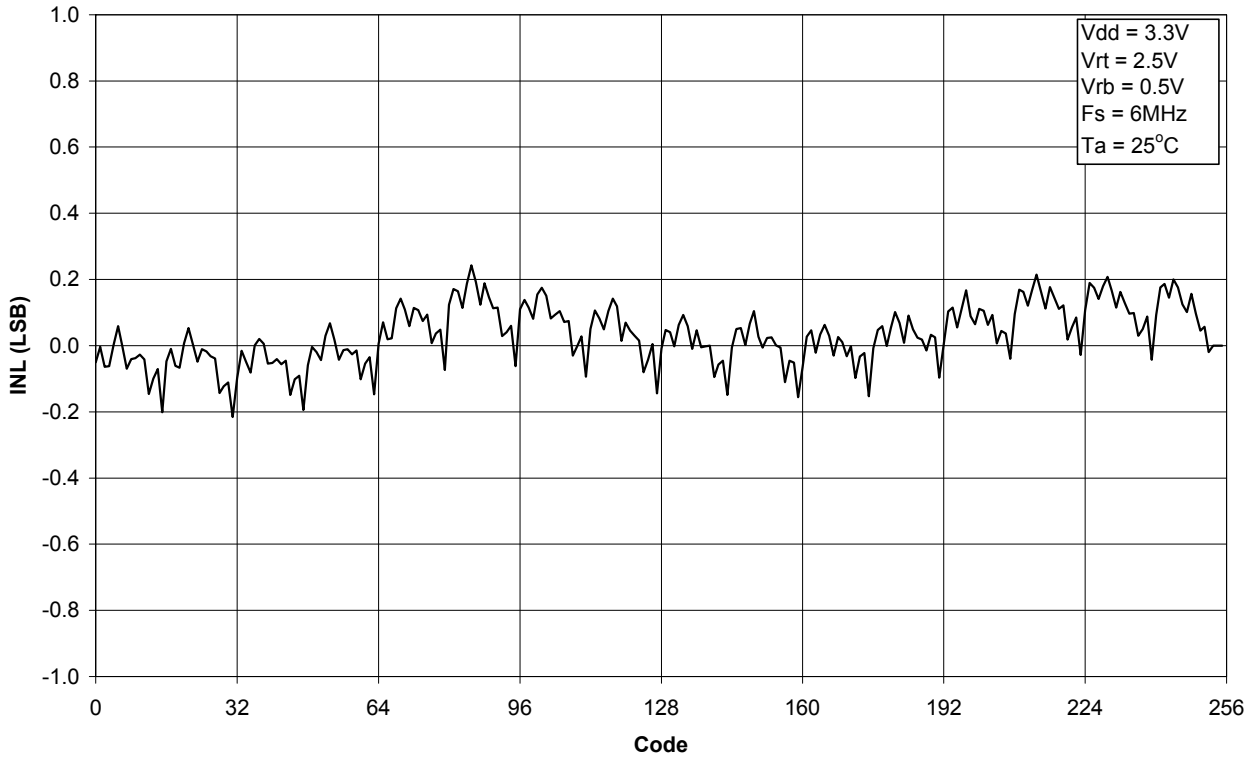
To avoid timing errors, use the rising edge of the sample clock (CLK) to latch data from the XRD87L75 to other parts of the system.

The reference can be biased internally by shorting  $V_{RT}$  to  $V_{RTS}$  and  $V_{RB}$  to  $V_{RBS}$ . This will generate  $0.4V$  at  $V_{RB}$  and  $1.72V$  at  $V_{RT}$  (see *Figure 5*).

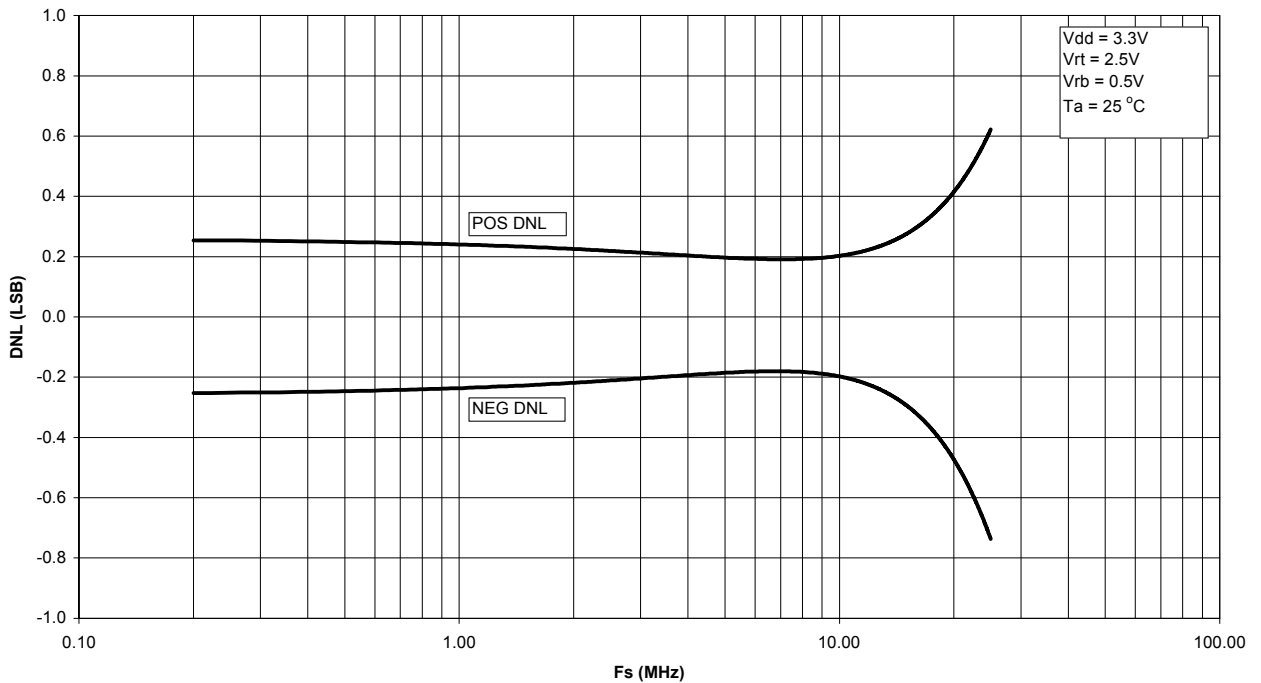
If the internal reference pins  $V_{RTS}$  and/or  $V_{RBS}$  are not used they should be left unconnected.



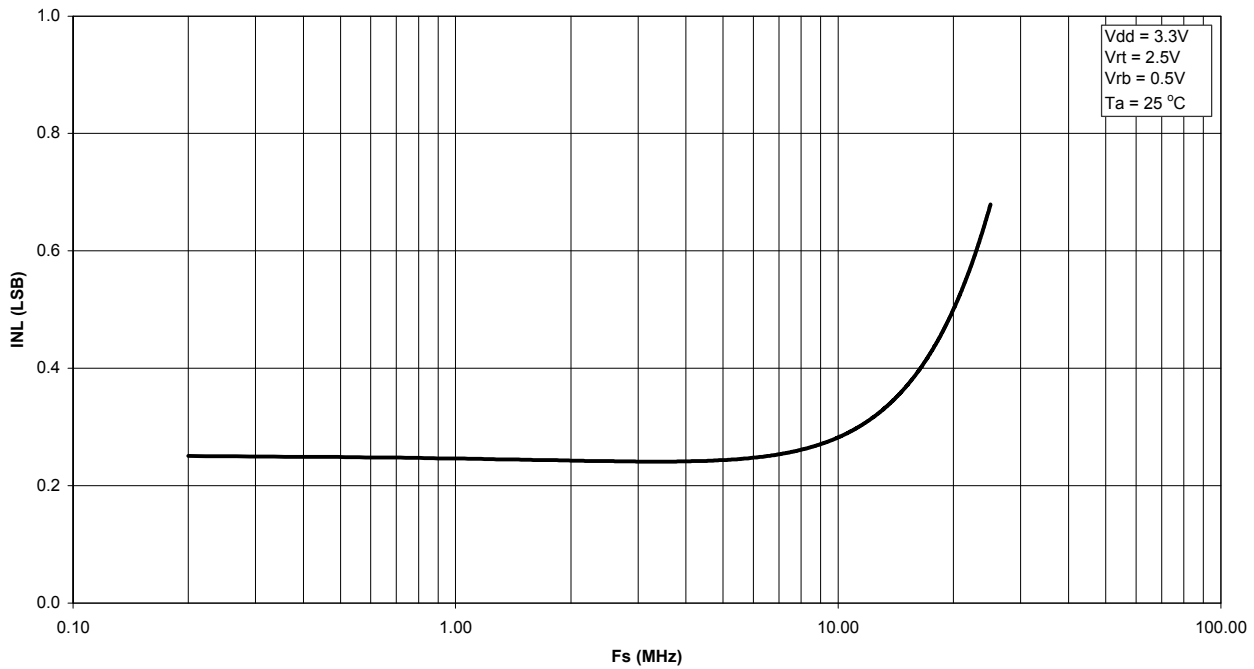
Graph 1. DNL vs. Code



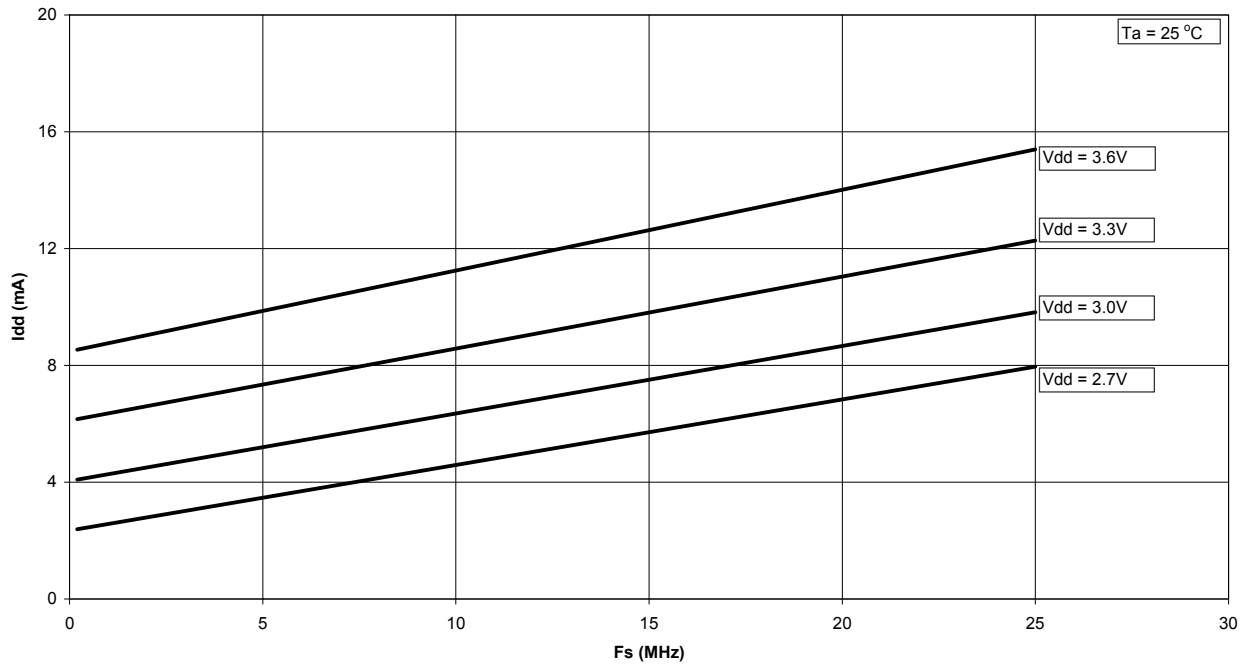
Graph 2. INL vs. Code



Graph 3. DNL vs. Sampling Frequency

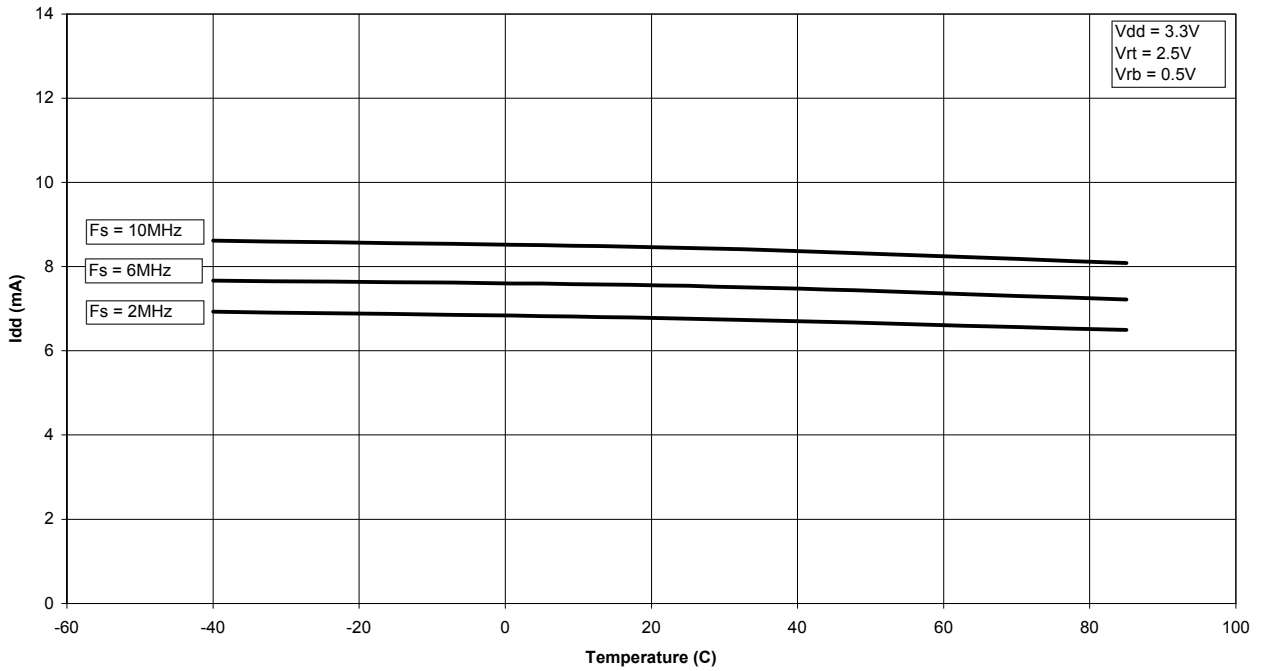


Graph 4. Best Fit INL vs. Sampling Frequency

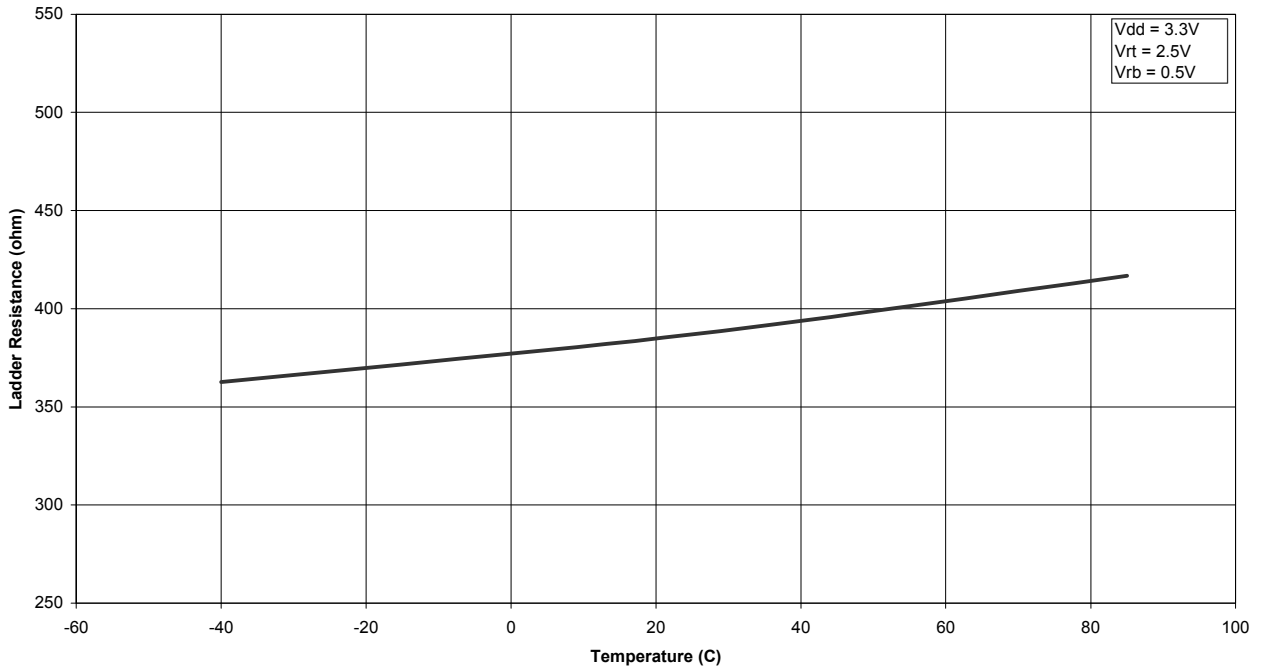


Graph 5. IDD vs. Sampling Frequency

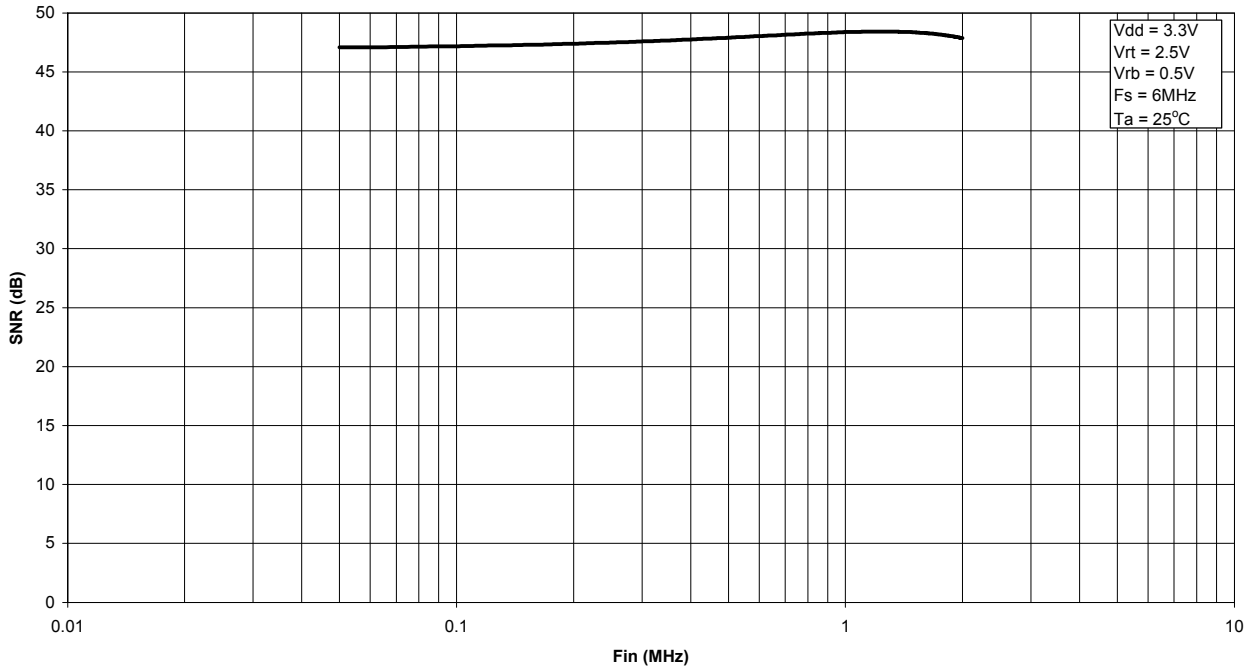




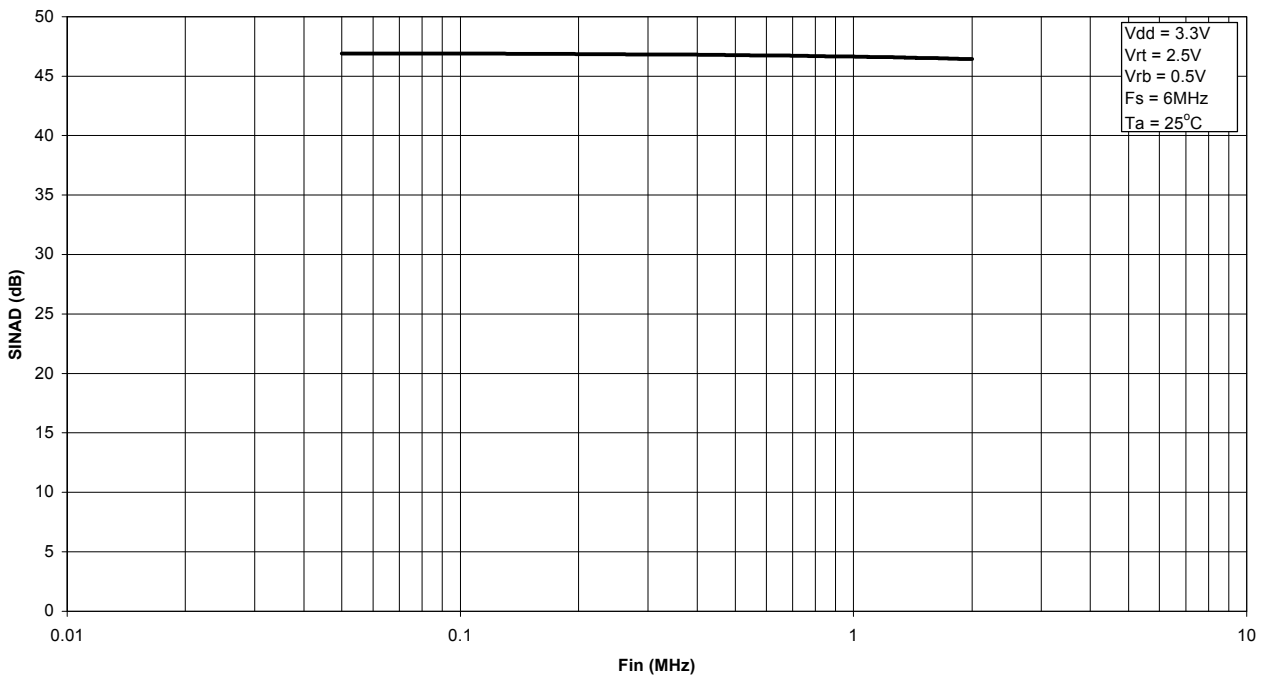
Graph 6. Supply Current vs. Temperature



Graph 7. Ladder Resistance vs. Temperature

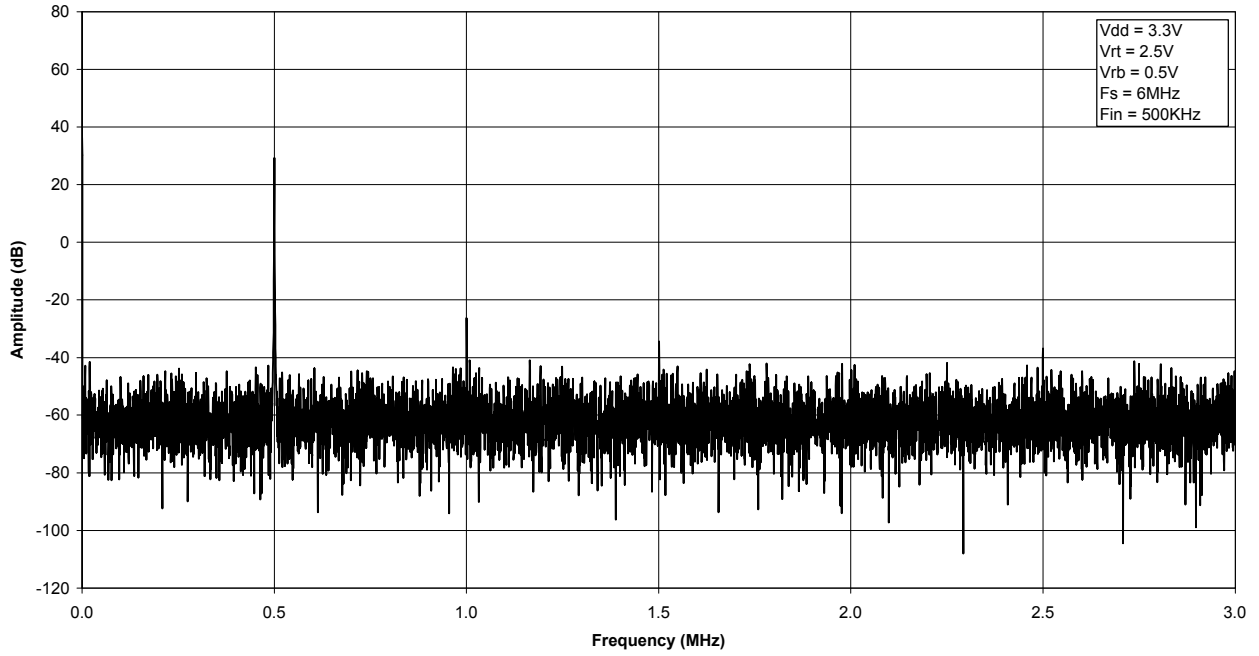


Graph 8. SNR vs. Input Frequency



Graph 9. SINAD vs. Input Frequency

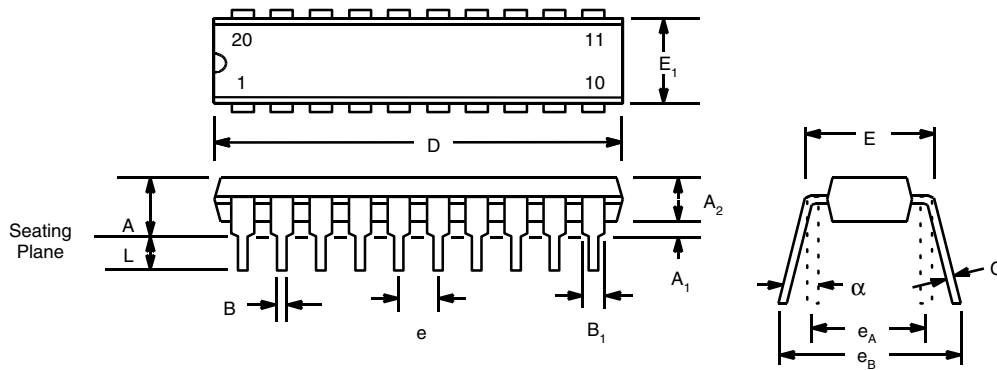
Graph 10. FFT Plot



Graph 10. FFT Plot

## 20 LEAD PLASTIC DUAL-IN-LINE (300 MIL PDIP)

REV. 1.00

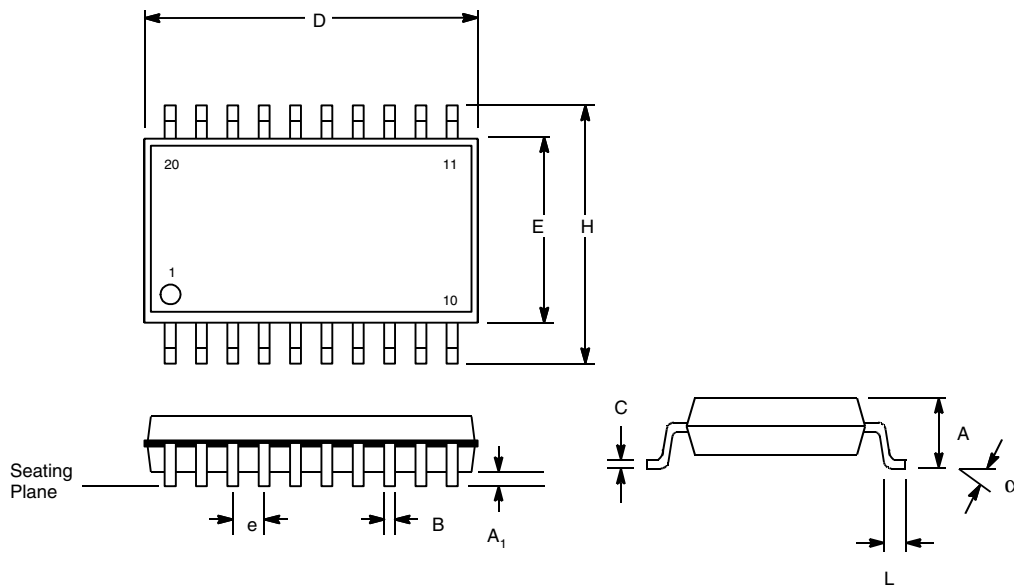


Note: The control dimension is the inch column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.145	0.210	3.68	5.33
A1	0.015	0.070	0.38	1.78
A2	0.115	0.195	2.92	4.95
B	0.014	0.024	0.36	0.56
B1	0.030	0.070	0.76	1.78
C	0.008	0.014	0.20	0.38
D	0.925	1.060	23.50	26.92
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eA	0.300 BSC		7.62 BSC	
eB	0.310	0.430	7.87	10.92
L	0.115	0.160	2.92	4.06
a	0°	15°	0°	15°

**20 LEAD SMALL OUTLINE  
(300 MIL JEDEC SOIC)**

REV. 1.00

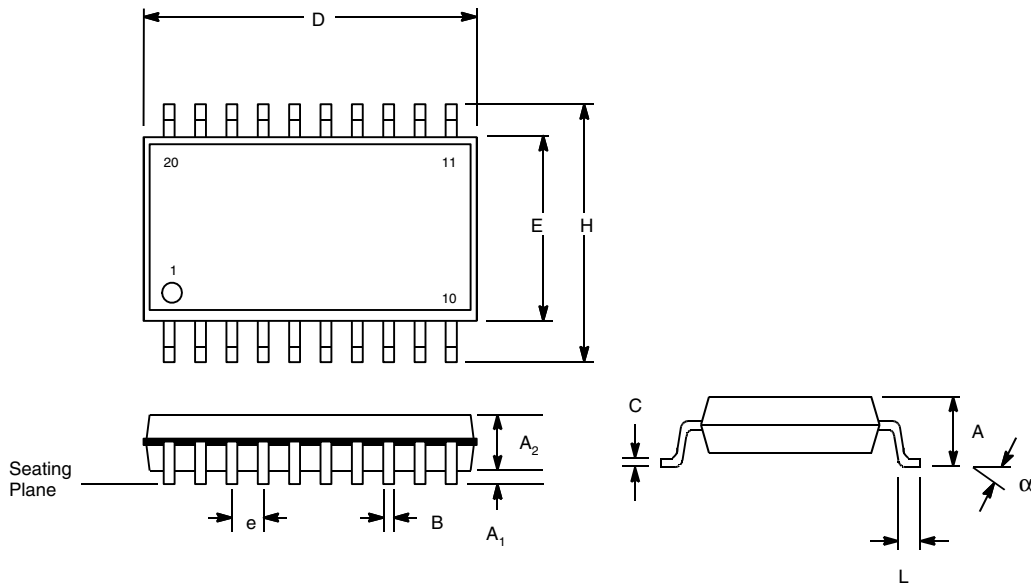


NOTE: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.013	0.020	0.33	0.51
C	0.009	0.013	0.23	0.32
D	0.496	0.512	12.60	13.00
E	0.291	0.299	7.40	7.60
e	0.050 BSC		1.27 BSC	
H	0.394	0.419	10.00	10.65
L	0.016	0.050	0.40	1.27
a	0°	8°	0°	8°

## 20 LEAD SHRINK SMALL OUTLINE PACKAGE (5.3 mm SSOP)

REV. 2.00



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.067	0.079	1.70	2.00
A1	0.002	0.006	0.05	0.15
A2	0.065	0.073	1.65	1.85
B	0.009	0.015	0.22	0.38
C	0.004	0.010	0.09	0.25
D	0.272	0.296	6.90	7.50
E	0.197	0.221	5.00	5.60
e	0.0256 BSC		0.65 BSC	
H	0.292	0.323	7.40	8.20
L	0.022	0.037	0.55	0.95
a	0°	8°	0°	8°

**NOTICE**

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 2002 EXAR Corporation  
Datasheet April 2002

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.