

April 2013

# FDPF035N06B\_F152

# N-Channel PowerTrench<sup>®</sup> MOSFET 60 V, 88 A, 3.5 m $\Omega$

#### **Features**

- $R_{DS(on)}$  = 2.91 m $\Omega$  ( Typ.) @  $V_{GS}$  = 10 V,  $I_D$  = 88 A
- Low FOM R<sub>DS(on)</sub>\*Q<sub>G</sub>
- Low Reverse Recovery Charge, Q<sub>rr</sub>
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- · Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

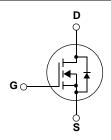
# **Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor®'s advanced PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

# **Applications**

- Synchronous Rectification for ATX / Server / Telecom PSU
- · Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Renewable System





# MOSFET Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted\*

Symbol		Parameter	Parameter		
V <sub>DSS</sub>	Drain to Source Voltage			60	V
V <sub>GSS</sub>	Gate to Source Voltage			±20	V
	Drain Current	- Continuous (T <sub>C</sub> = 25°C, Silicon Limited)		88	^
ID	Drain Current	- Continuous (T <sub>C</sub> = 100°C, Silic	on Limited)	62	A
I <sub>DM</sub>	Drain Current	- Pulsed	- Pulsed (Note 1)		Α
E <sub>AS</sub>	Single Pulsed Avalanche Er	ergy	(Note 2)	600	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	6.0	V/ns
D	Davis Diagination	$(T_C = 25^{\circ}C)$		46.3	W
$P_{D}$	Power Dissipation	- Derate above 25°C		0.31	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Tem	perature Range		-55 to +175	°C
T <sub>L</sub>	Maximum Lead Temperature 1/8" from Case for 5 Second			300	°C

#### **Thermal Characteristics**

Symbol	Parameter	FDPF035N06B_F152	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	3.24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	62.5	*C/VV

# **Package Marking and Ordering Information**

Device Marking	Device	Package	Packaging Type	Quantity
FDPF035N06B	FDPF035N06B_F152	TO-220F	Tube	50

# **Electrical Characteristics** $T_C = 25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	eteristics					
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	60	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250μA, Referenced to 25°C	-	0.03	-	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 48V, V_{GS} = 0V$	-	-	1	μΑ
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	-	-	±100	nA

#### On Characteristics

1	$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu A$	2	-	4	V
	R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10V, I_D = 88A$	•	2.91	3.5	mΩ
9	g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10V, I_{D} = 88A$	•	176	-	S

## **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	.,	-	6035	8030	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 30V, V_{GS} = 0V$ f = 1MHz	-	1685	2240	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 - 1101112	-	55	-	pF
C <sub>oss(er)</sub>	Energy Related Output Capacitance	$V_{DS} = 30V, V_{GS} = 0V$	-	2619	-	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10V		-	76	99	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DS} = 30V, I_{D} = 100A$	-	29	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge	V <sub>GS</sub> = 10V	-	12	-	nC
V <sub>plateau</sub>	Gate Plateau Volatge	(Note 4	-	5.2	-	V
Q <sub>sync</sub>	Total Gate Charge Sync.	$V_{DS} = 0V$ , $I_D = 50A$ (Note 5)	-	67.3	-	nC
Q <sub>oss</sub>	Output Charge	$V_{DS} = 30V, V_{GS} = 0V$	-	92.4	-	nC

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time		-	32	74	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 30V, I_{D} = 100A$	-	33	76	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 10V, R_{GEN} = 4.7\Omega$	-	56	122	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	-	23	56	ns
ESR	Equivalent Series Resistance (G-S)	f = 1MHz	-	2.0	-	Ω

#### **Drain-Source Diode Characteristics**

Is	Maximum Continuous Drain to Source Diode Forward Current			-	88	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	352	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0V, I_{SD} = 88A$	-	-	1.25	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 100A	-	71	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F/dt = 100A/\mu s$	-	78	-	nC

#### Notes

- 1. Repetitive Rating: Pulse width limited by maximum junction temperature
- 2. L = 3mH,  $I_{AS}$  = 20A, Starting  $T_J$  = 25°C
- 3.  $I_{SD} \leq$  100A, di/dt  $\leq$  200A/ $\mu$ s,  $V_{DD} \leq$  BV $_{DSS}$ , Starting  $T_J$  = 25°C
- 4. Essentially Independent of Operating Temperature Typical Characteristics
- 5. See the test circuit in page 8

# **Typical Performance Characteristics**

Figure 1. On-Region Characteristics

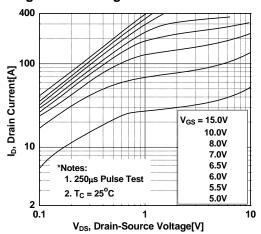


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

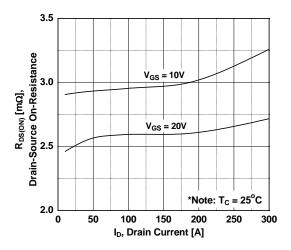


Figure 5. Capacitance Characteristics

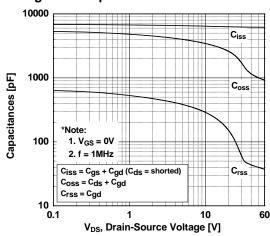


Figure 2. Transfer Characteristics

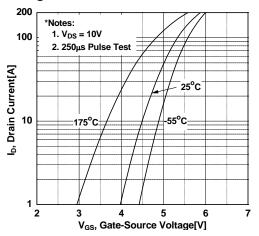


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

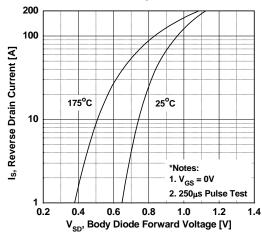
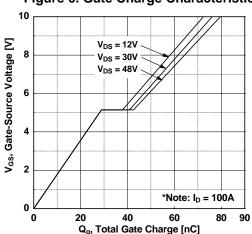


Figure 6. Gate Charge Characteristics



## Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

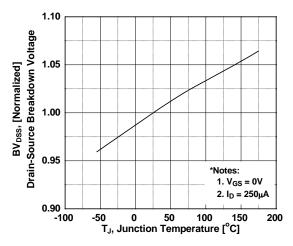


Figure 9. Maximum Safe Operating Area vs. Case Temperature

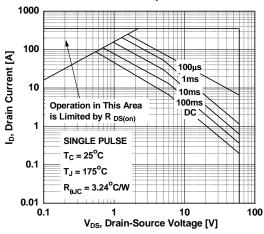


Figure 11. Eoss vs. Drain to Source Voltage

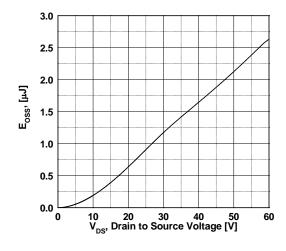


Figure 8. On-Resistance Variation vs. Temperature

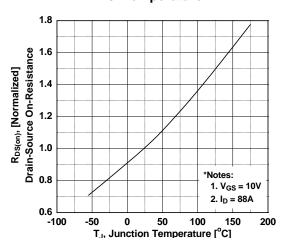


Figure 10. Maximum Drain Current

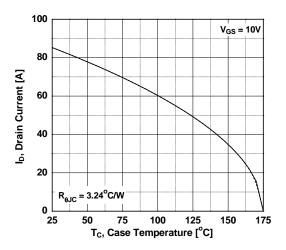
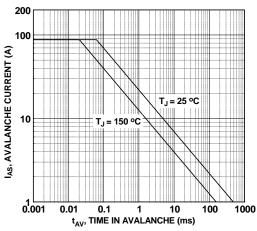
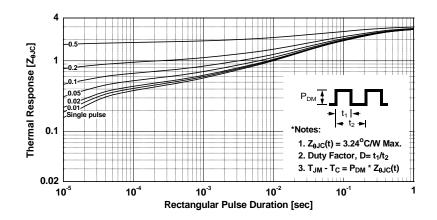


Figure 12. Unclamped Inductive Switching Capability

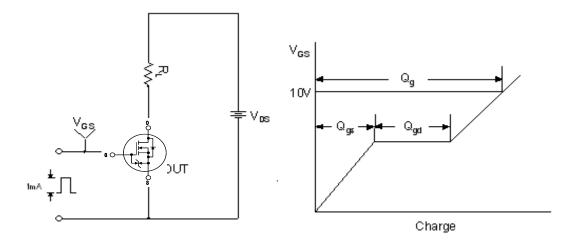


# **Typical Performance Characteristics** (Continued)

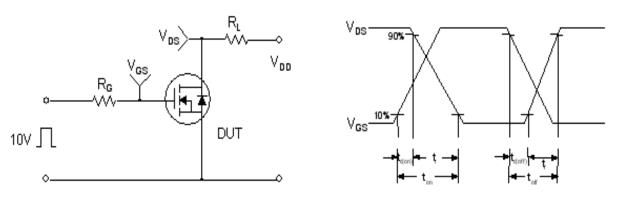




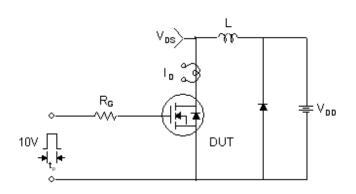
#### **Gate Charge Test Circuit & Waveform**

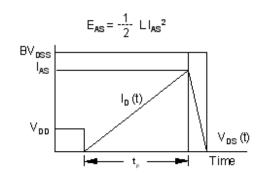


#### **Resistive Switching Test Circuit & Waveforms**

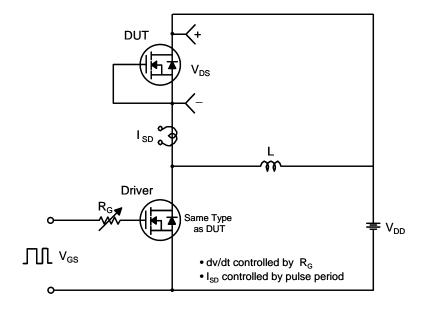


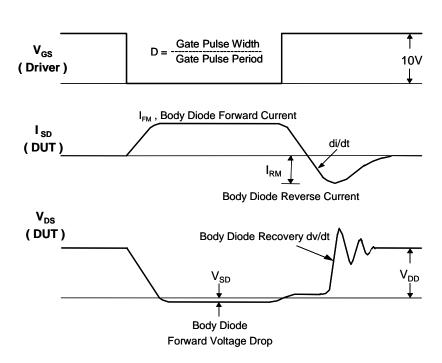
**Unclamped Inductive Switching Test Circuit & Waveforms** 



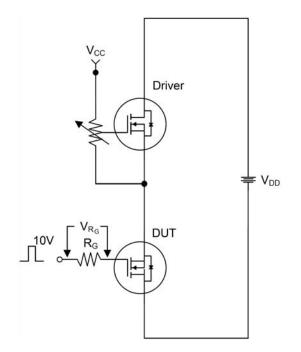


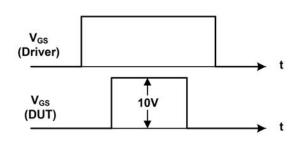
#### Peak Diode Recovery dv/dt Test Circuit & Waveforms





#### Total Gate Charge Qsync. Test Circuit & Waveforms

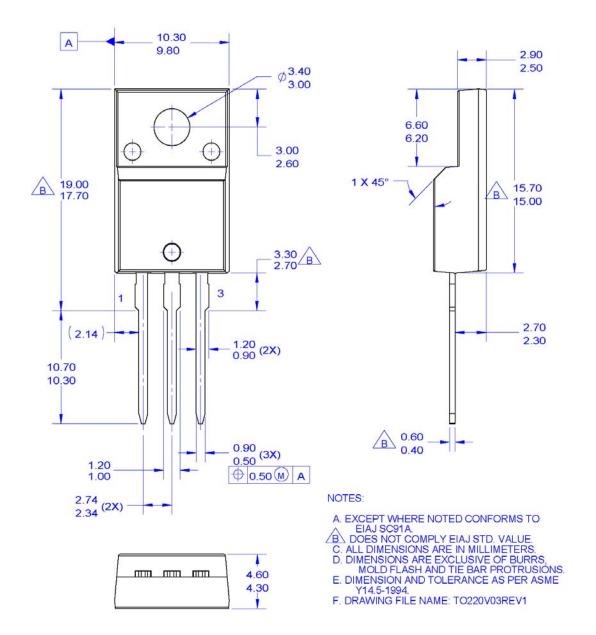




$$Qsync = \frac{1}{R_G} \cdot \int V_{R_G}(t) dt$$

### **Mechanical Dimensions**

# TO-220F



\* Front/Back Side Isolation Voltage: AC 2500V





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