

## GaAs PHEMT MMIC POWER AMPLIFIER, DC - 18 GHz

### Typical Applications

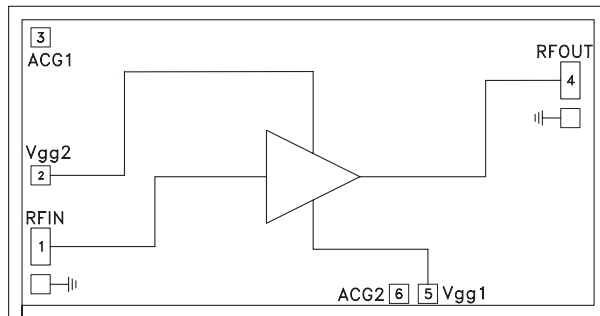
The HMC459 wideband driver is ideal for:

- Telecom Infrastructure
- Microwave Radio & VSAT
- Military & Space
- Test Instrumentation

### Features

- P1dB Output Power: +25 dBm
- Gain: 17 dB
- Output IP3: +31.5 dBm
- Supply Voltage: +8V @ 290 mA
- 50 Ohm Matched Input/Output
- Die Size: 3.12 x 1.63 x 0.1 mm

### Functional Diagram



### General Description

The HMC459 is a GaAs MMIC PHEMT Distributed Power Amplifier die which operates between DC and 18 GHz. The amplifier provides 17 dB of gain, +31.5 dBm output IP3 and +25 dBm of output power at 1 dB gain compression while requiring 290 mA from a +8V supply. Gain flatness is good making the HMC459 ideal for EW, ECM and radar driver amplifier applications. The HMC459 amplifier I/O's are internally matched to 50 Ohms facilitating easy integration into Multi-Chip-Modules (MCMs). All data is with the chip in a 50 Ohm test fixture connected via 0.025mm (1 mil) diameter wire bonds of minimal length 0.31mm (12 mils).

### Electrical Specifications, $T_A = +25^\circ\text{C}$ , $V_{dd} = 8\text{V}$ , $V_{gg2} = 3\text{V}$ , $I_{dd} = 290\text{mA}^*$

| Parameter  | Min.     | Typ. | Max. | Min.     | Typ.  | Max. | Min.      | Typ.  | Max. | Min.      | Typ.  | Max.  | Units |
|--|----------|------|------|----------|-------|------|-----------|-------|------|-----------|-------|-------|-------|
| Frequency Range                                  | DC - 2.0 |      |      | DC - 6.0 |       |      | DC - 10.0 |       |      | DC - 18.0 |       |       | GHz   |
| Gain   | 16.5     | 18.5 |      | 15       | 18    |      | 14        | 17    |      | 9         | 12    |       | dB    |
| Gain Flatness                                    |          | ±0.5 |      |          | ±0.75 |      |           | ±0.75 |      |           |       |       | dB    |
| Gain Variation Over Temperature                  |          | 0.02 | 0.03 |          | 0.02  | 0.03 |           | 0.03  | 0.04 |           | 0.035 | 0.045 | dB/°C |
| Input Return Loss                                |          | 22   |      |          | 19.5  |      |           | 19    |      |           | 10    |       | dB    |
| Output Return Loss                               |          | 27   |      |          | 15    |      |           | 14    |      |           | 14    |       | dB    |
| Output Power for 1 dB Compression (P1dB)         | 21       | 24   |      | 20.5     | 24.5  |      | 22        | 25    |      | 14        | 17    |       | dBm   |
| Saturated Output Power (Psat)                    |          | 26.5 |      |          | 26.5  |      |           | 26.5  |      |           | 21    |       | dBm   |
| Output Third Order Intercept (IP3)               |          | 40   |      |          | 34    |      |           | 31.5  |      |           | 26    |       | dBm   |
| Noise Figure                                     |          | 4.0  |      |          | 4.0   |      |           | 3.0   |      |           | 6.5   |       | dB    |
| Supply Current (Idd) (Vdd= 8V, Vgg1= -0.5V Typ.) |          | 290  |      |          | 290   |      |           | 290   |      |           | 290   |       | mA    |

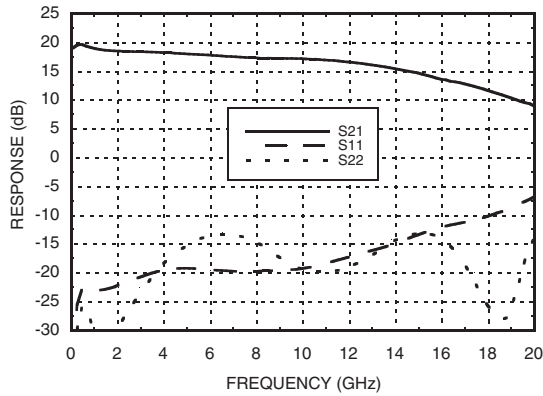
\* Adjust Vgg1 between -2 to 0V to achieve Idd= 290 mA typical.

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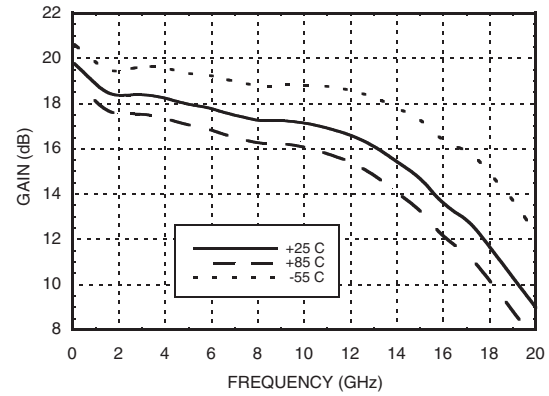
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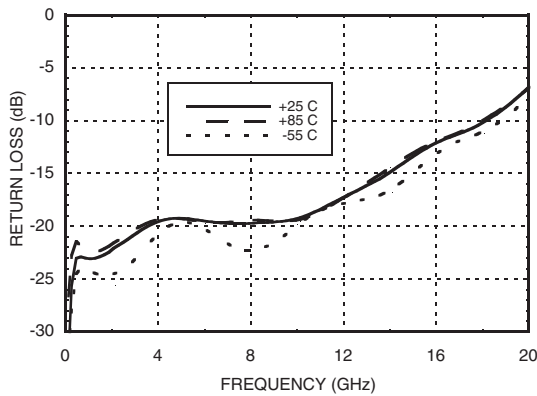
**Gain & Return Loss**



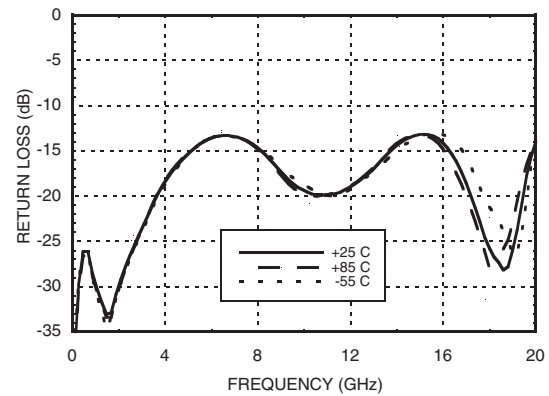
**Gain vs. Temperature**



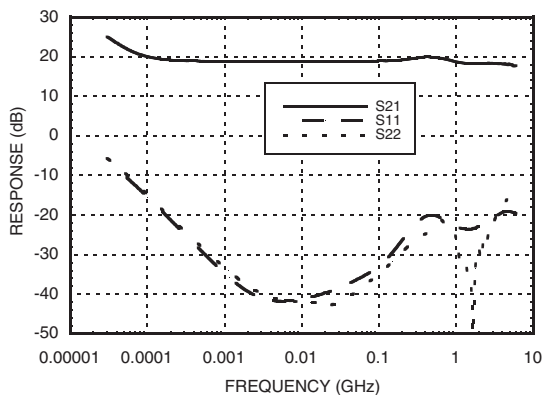
**Input Return Loss vs. Temperature**



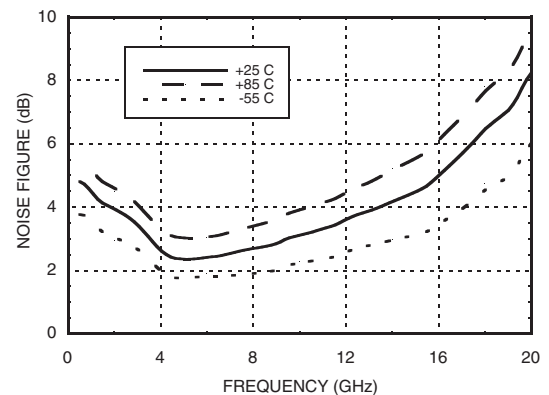
**Output Return Loss vs. Temperature**



**Low Frequency Gain & Return Loss**

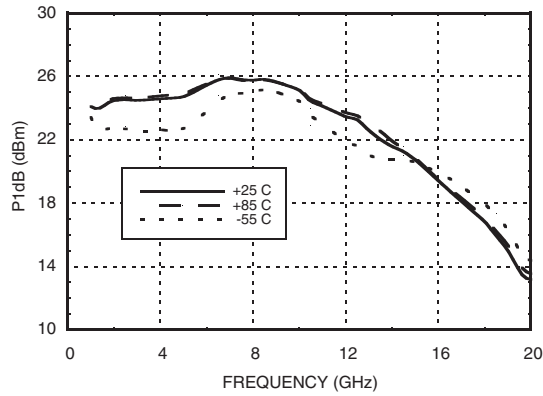


**Noise Figure vs. Temperature**

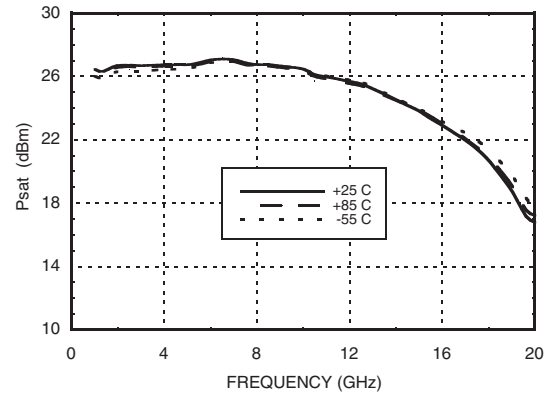


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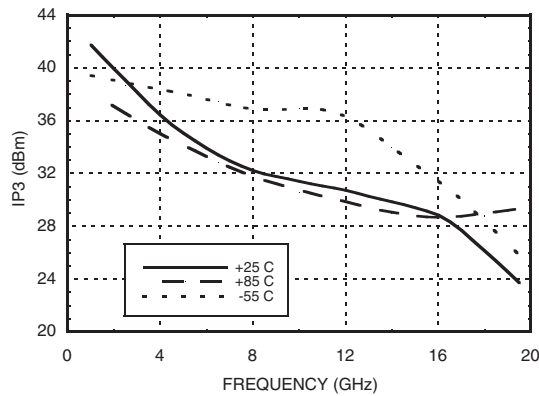
**Output P1dB vs. Temperature**



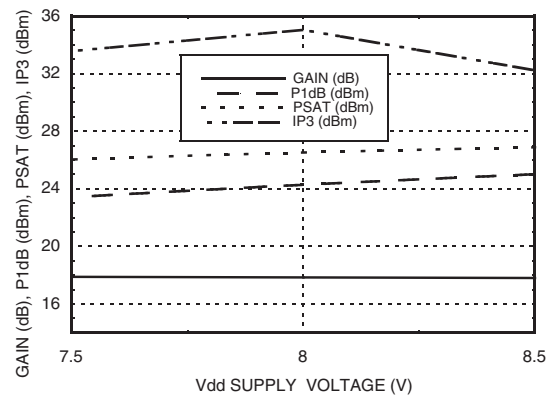
**Output Psat vs. Temperature**



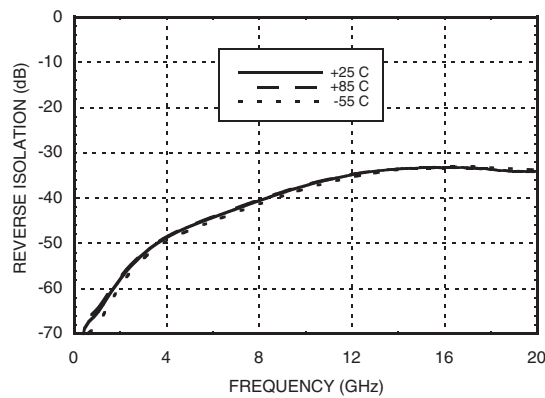
**Output IP3 vs. Temperature**



**Gain, Power & Output IP3  
vs. Supply Voltage @ 5 GHz, Fixed Vgg**



**Reverse Isolation vs. Temperature**



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**Absolute Maximum Ratings**

|  |                     |
|--|---------------------|
| Drain Bias Voltage (Vdd)                                       | +9 Vdc              |
| Gate Bias Voltage (Vgg1)                                       | -2 to 0 Vdc         |
| Gate Bias Voltage (Vgg2)                                       | (Vdd -8) Vdc to Vdd |
| RF Input Power (RFIN)(Vdd = +8 Vdc)                            | +16 dBm             |
| Channel Temperature  | 175 °C              |
| Continuous Pdiss (T= 85 °C)<br>(derate 51.5 mW/°C above 85 °C) | 4.64 W              |
| Thermal Resistance<br>(channel to die bottom)                  | 19.4 °C/W           |
| Storage Temperature  | -65 to +150 °C      |
| Operating Temperature  | -55 to +85 °C       |

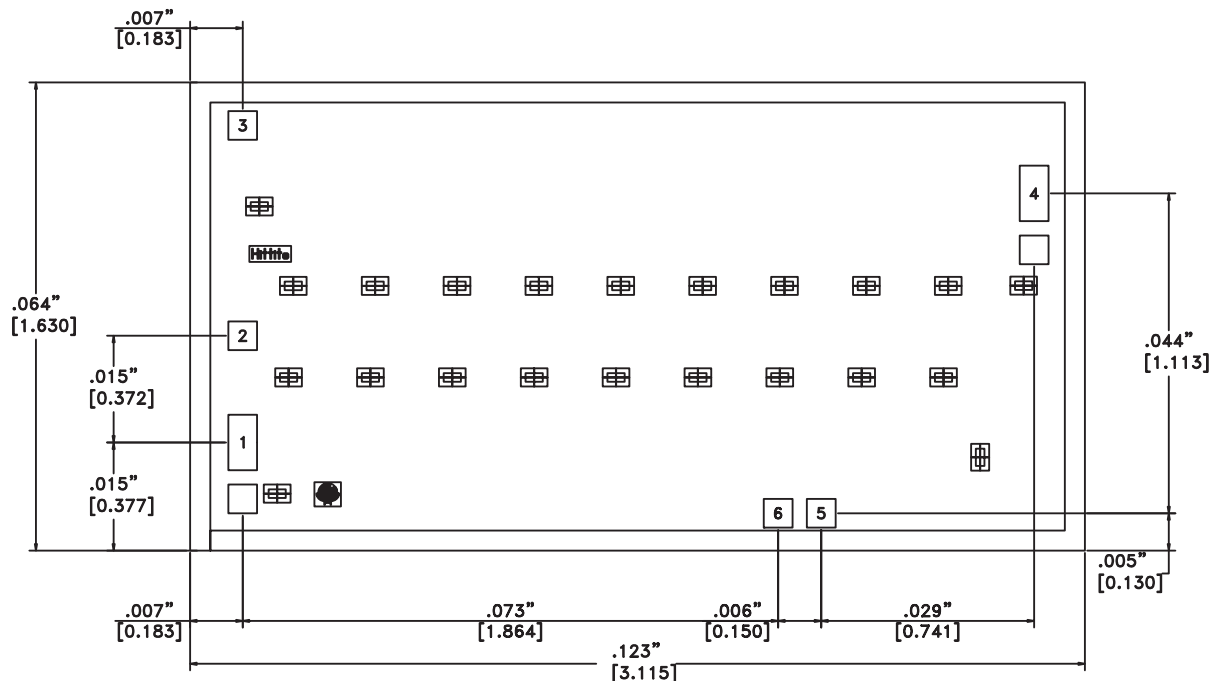
**Typical Supply Current vs. Vdd**

| Vdd (V) | Idd (mA) |
|---------|----------|
| +7.5    | 292      |
| +8.0    | 290      |
| +8.5    | 288      |



**ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS**

**Outline Drawing**



**Die Packaging Information [1]**

| Standard        | Alternate |
|-----------------|-----------|
| GP-1 (Gel Pack) | [2]       |

[1] Refer to the "Packaging Information" section for die packaging dimensions.

[2] For alternate packaging information contact Hittite Microwave Corporation.

**NOTES:**

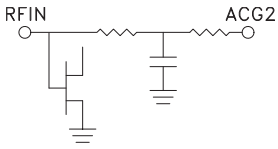
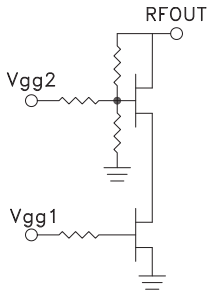
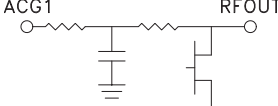
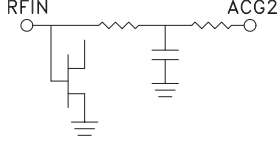

1. ALL DIMENSIONS IN INCHES [MILLIMETERS]
2. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
3. DIE THICKNESS IS 0.004 (0.100)
4. TYPICAL BOND PAD IS 0.004 (0.100) SQUARE
5. BACKSIDE METALLIZATION: GOLD
6. BACKSIDE METAL IS GROUND
7. BOND PAD METALIZATION: GOLD

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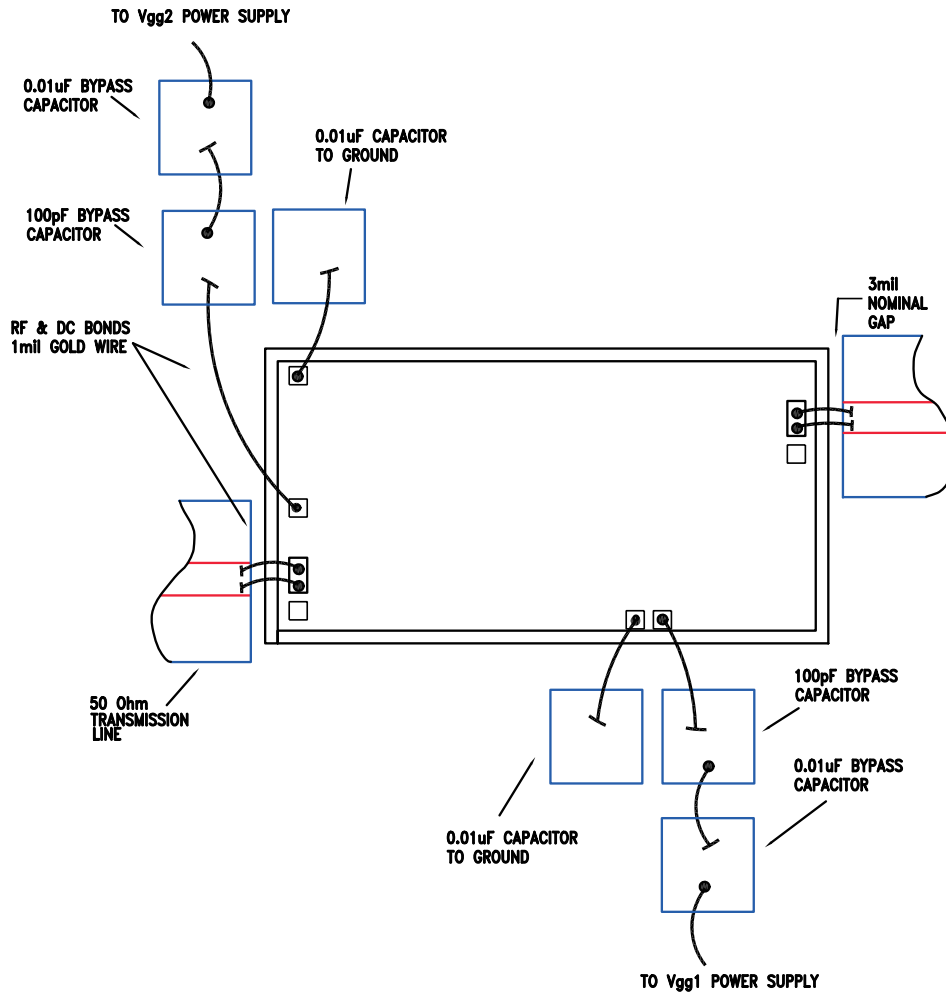
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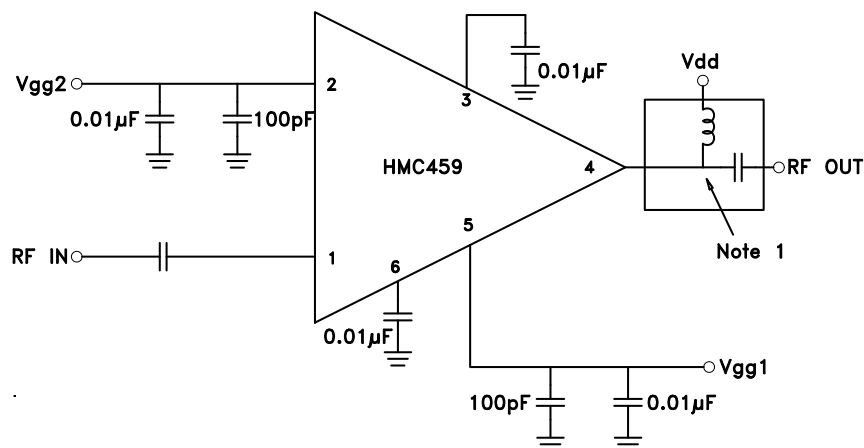
**Pad Descriptions**

| Pad Number | Function    | Description  | Interface Schematic   |
|------------|-------------|--|---|
| 1          | RFIN        | This pad is DC coupled and matched to 50 Ohms.   |    |
| 2          | Vgg2        | Gate Control 2 for amplifier. +3V should be applied to Vgg2 for nominal operation. Vgg2 may be adjusted between 0 to +5V to temperature compensate gain. |    |
| 4          | RFOUT & Vdd | RF output for amplifier. Connect the DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.                               |   |
| 5          | Vgg1        | Gate Control 1 for amplifier. Adjust between -2 to 0V to achieve Idd= 290 mA.  |   |
| 3          | ACG1        | Low frequency termination. Attach bypass capacitor per application circuit here in.  |  |
| 6          | ACG2        | Low frequency termination. Attach bypass capacitor per application circuit here in.  |  |
| Die Bottom | GND         | Die bottom must be connected to RF/DC ground.  |  |

**Assembly Diagram**



**Application Circuit**



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.

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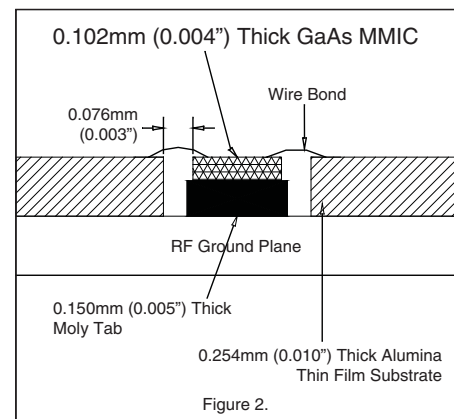
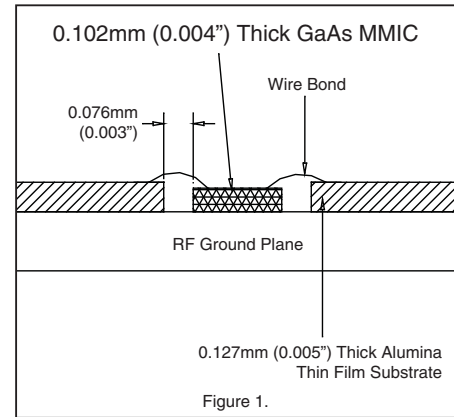
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**Mounting & Bonding Techniques for Millimeterwave GaAs MMICs**

The die should be attached directly to the ground plane eutectically or with conductive epoxy (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2).

Microstrip substrates should be brought as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076mm to 0.152 mm (3 to 6 mils).



**Handling Precautions**

Follow these precautions to avoid permanent damage.

**Storage:** All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

**Cleanliness:** Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

**Static Sensitivity:** Follow ESD precautions to protect against ESD strikes.

**Transients:** Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

**General Handling:** Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip may have fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

**Mounting**

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

**Eutectic Die Attach:** A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

**Epoxy Die Attach:** Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

**Wire Bonding**

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31mm (12 mils).

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**Notes:**