HMC713LP3E

54 dB, LOGARITHMIC DETECTOR / CONTROLLER, 50 - 8000 MHz

Typical Applications

The HMC713LP3E is ideal for:

- Cellular Infrastructure
- WiMAX, WiBro & LTE/4G
- Power Monitoring & Control Circuitry
- Receiver Signal Strength Indication (RSSI)
- Automatic Gain & Power Control
- Military, ECM & Radar

Features

Wide Dynamic Range: up to 54 dB

High Accuracy:
±1 dB with 54 dB Range Up To 2.7 GHz

Fast Output Response Time

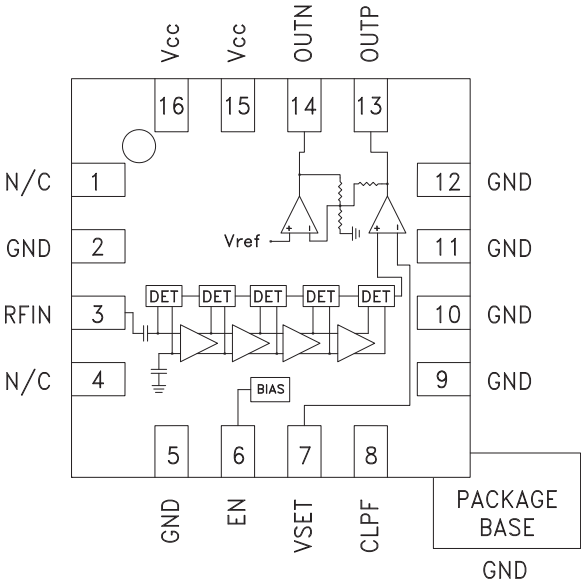
Supply Voltage: +2.7 to +5.5V

Power-Down Mode

Excellent Stability over Temperature

16 Lead 3x3 mm SMT Package: $9mm^2$

Functional Diagram



General Description

The HMC713LP3E Logarithmic Detector/Controller is ideal for converting the power of RF signals with frequencies in the 50 MHz to 8000 MHz range, to a DC voltage, proportional to input power, at its output. The HMC713LP3E employs a successive compression technology which delivers 54 dB of dynamic range with high measurement accuracy over a wide input frequency range. As the input signal is increased, successive amplifiers move into saturation one by one creating an accurate approximation of the logarithm function. The outputs of a series of detectors are summed, converted into voltage domain and buffered to drive the OUTP output.

For detection mode, the OUTP pin is connected to the VSET input and will provide a nominal logarithmic slope of 17 mV/dB and an intercept of -68 dBm. The HMC713LP3E can also be used in the controller mode where an external voltage is applied to the VSET pin to create an AGC or APC feedback loop.

Electrical Specifications, T_A = +25 °C, Vcc = +3V, EN = +3V [1]

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Frequency	50	100	500	900	1900	2700	3900	5800	7000	8000	MHz
±3 dB Dynamic Range	61	61	61	62	62	61	58	50	44	40	dB
±3 dB Dynamic Range Center	-27	-27	-27	-28	-28	-28	-26	-23	-20	-17	dBm
±1 dB Dynamic Range	54	53	53	54	55	54	49	39	33	31	dB
OUTP Slope	17.2	17.2	17.2	17.1	17	17.2	18.3	21.2	23.8	25.5	mV/dB
OUTP Intercept	-67.9	-68.1	-68.6	-68.9	-69.5	-69.2	-65.3	-55.9	-48.8	-44.2	dBm
Variation of OUTP with Temperature from -40°C to +85°C @ -20 dBm Input	-1.3	-1.3	-1.2	-1.2	-1.1	-1.1	-1.2	-2.1	-2.8	-3.5	dB

[1] Detector mode measurements; OUTP (Pin 13) is connected to VSET (Pin 7) through an RC network.

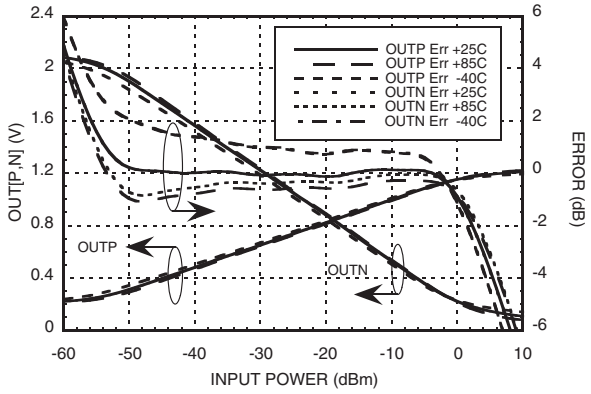
Electrical Specifications, (continued)

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Down (EN) Input					
Voltage Range for Normal Mode		0.8 x Vcc	Vcc/2		V
Voltage Range for Powerdown Mode			Vcc/2	0.2 x Vcc	V
Power Supply (Vcc)					
Operating Voltage Range			2.7 - 5.5		V
Supply Current in Normal Mode	EN Input at Vcc		17		mA
Supply Current in Power Down Mode	EN Input at GND		0.4		mA
OUTP Output					
Rise Time	CLPF= 0, No Power to -10 dBm, 10% - 90%		24		ns
Fall Time	CLPF= 0, -10 dBm to No Power, 90% - 10%		36		ns
Output Video BW	50mV reduction in output voltage swing (3 dB referred to the input) [1]		16		MHz
Voltage Range	Closed Loop (Eval Board Setup)		0.2 - 1.2		V
Voltage Range	Open Loop		0.1 to (Vcc -0.1)		V
Current Drive Source / Sink			4.2 / 0.48		mA
OUTN Output					
Current Drive Source / Sink			4.0 / 0.43		mA
Output Voltage Range			0.2 - 2.1		V
RF Input					
Input Return Loss (S11)	F= 50 MHz to 8 GHz Z_0= 50Ω, See plot		10		dB
VSET Input					
Input Impedance			1		MΩ
Input Voltage Range	Eval Board		0.2 - 1.2		V
Low Frequency Gain	VSET to OUTP		64		dB
Open Loop Corner Frequency			11		kHz

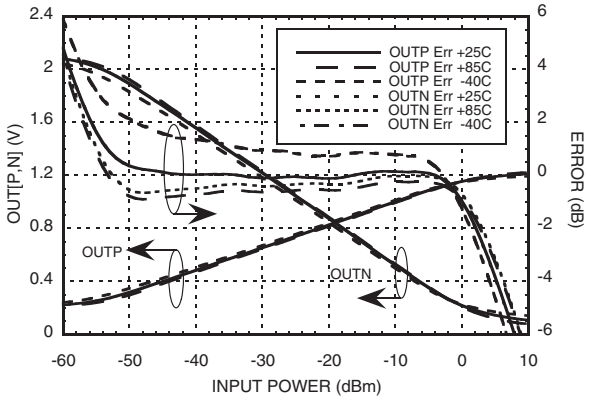
[1] Two tone test: Frequency = 900 MHz, Tone 1 Power = -20 dBm, Tone 2 Power = -28 dBm

RoHS✓ EARTH FRIENDLY

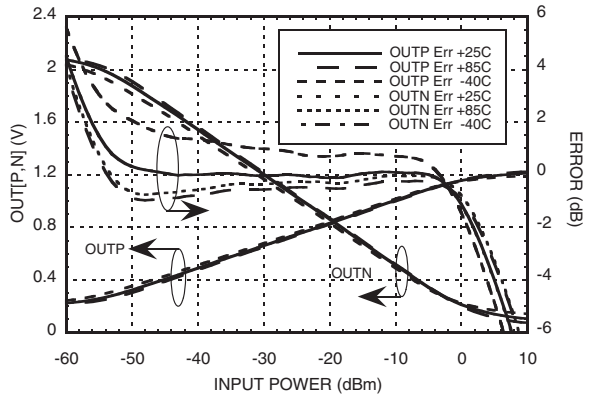
Output Voltage & Error vs. Input Power, Fin = 50 MHz



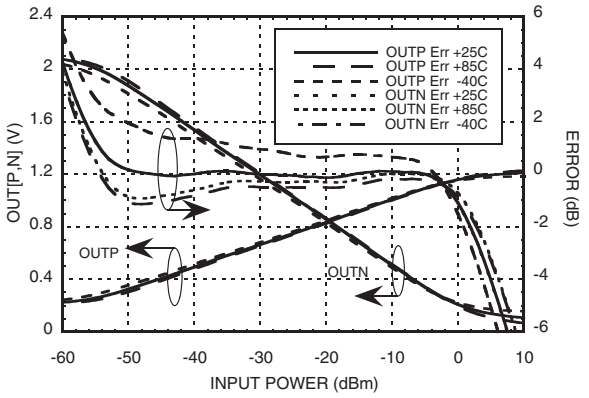
Output Voltage & Error vs. Input Power, Fin = 100 MHz



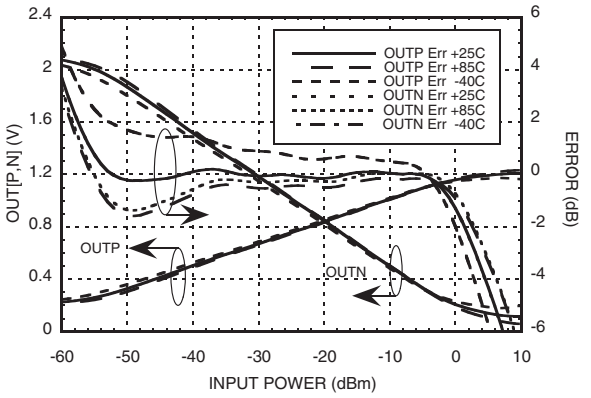
Output Voltage & Error vs. Input Power, Fin = 500 MHz



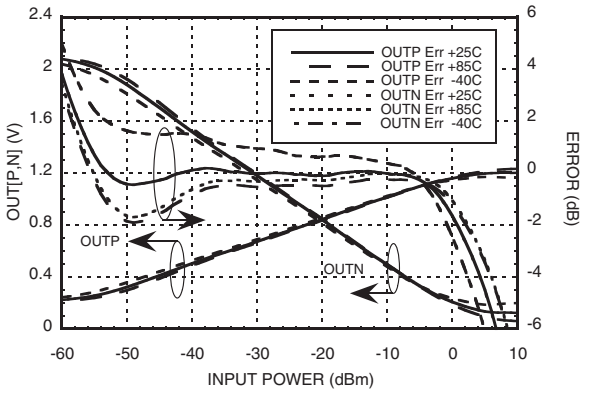
Output Voltage & Error vs. Input Power, Fin = 900 MHz



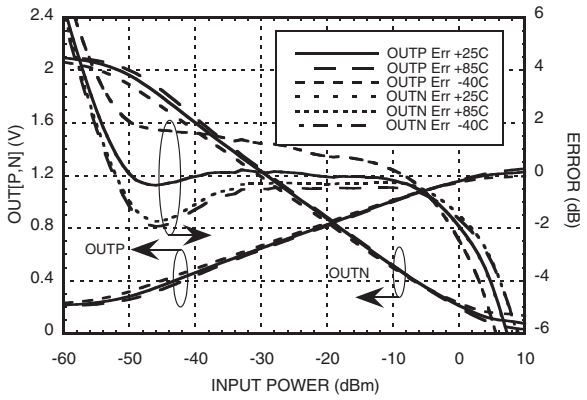
Output Voltage & Error vs. Input Power, Fin = 1900 MHz



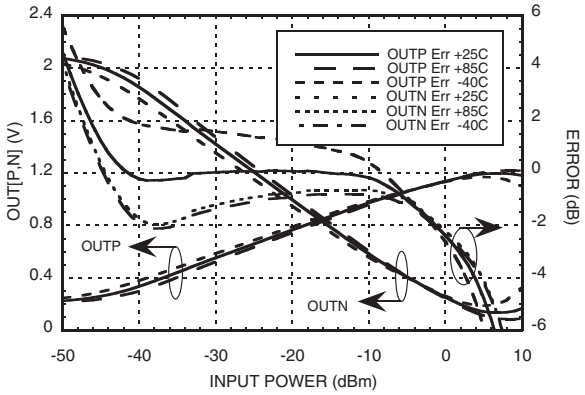
Output Voltage & Error vs. Input Power, Fin = 2700 MHz



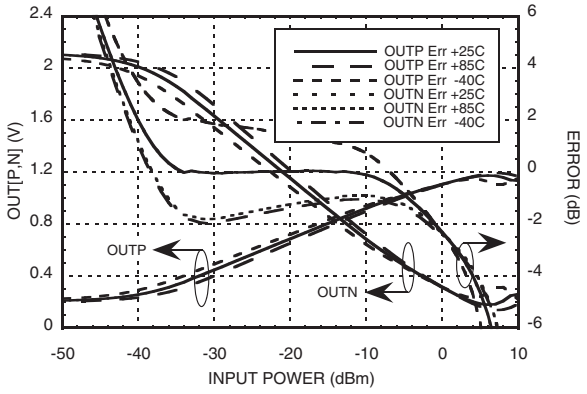
Output Voltage & Error vs. Input Power, Fin = 3900 MHz



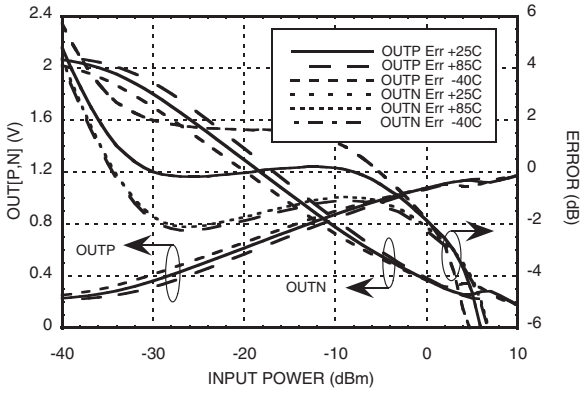
Output Voltage & Error vs. Input Power, Fin = 5800 MHz



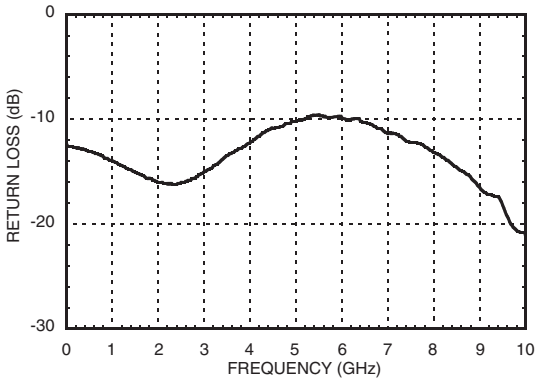
Output Voltage & Error vs. Input Power, Fin = 7000 MHz



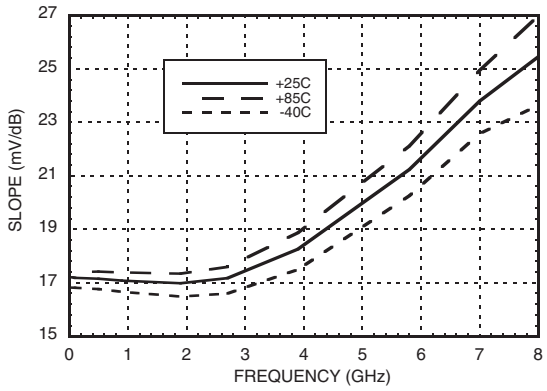
Output Voltage & Error vs. Input Power, Fin = 8000 MHz



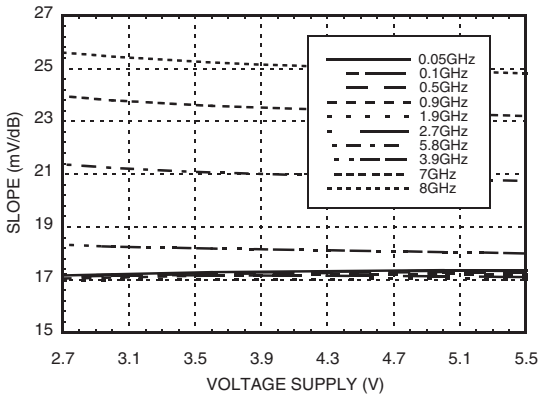
Input Return Loss



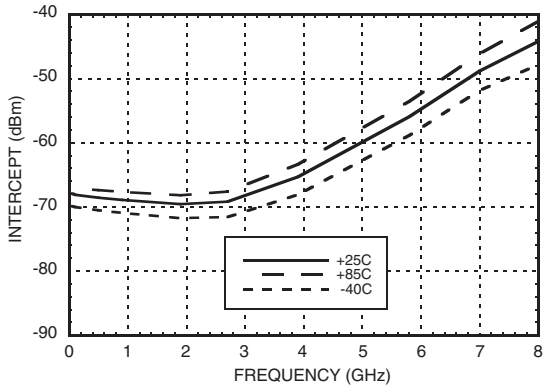
OUTP Slope vs. Frequency



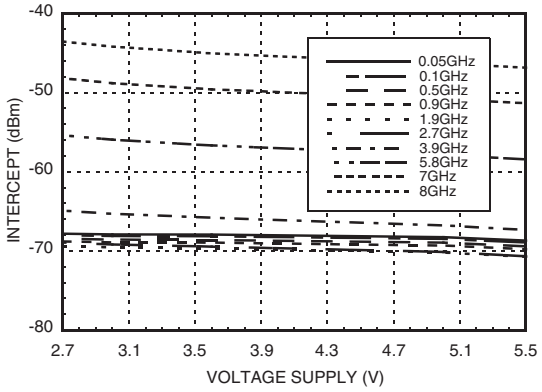
OUTP Slope vs. Supply Voltage



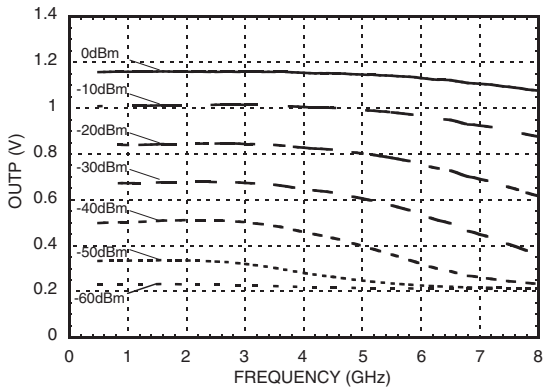
OUTP Intercept vs. Frequency



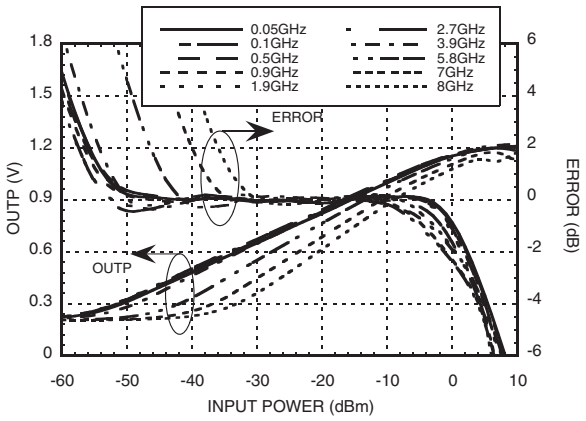
OUTP Intercept vs. Supply Voltage



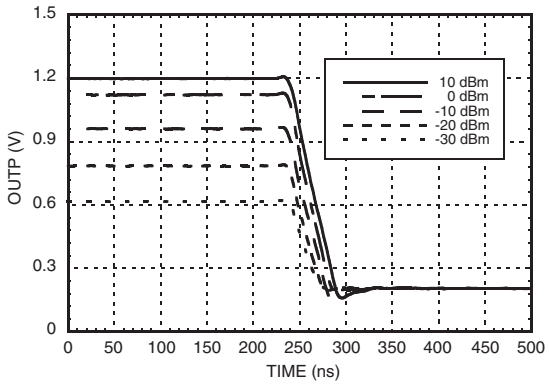
OUTP vs. Frequency & Input Power



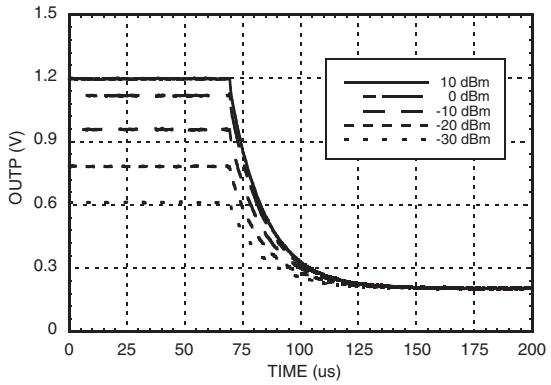
OUTP Voltage & Error vs. Frequency



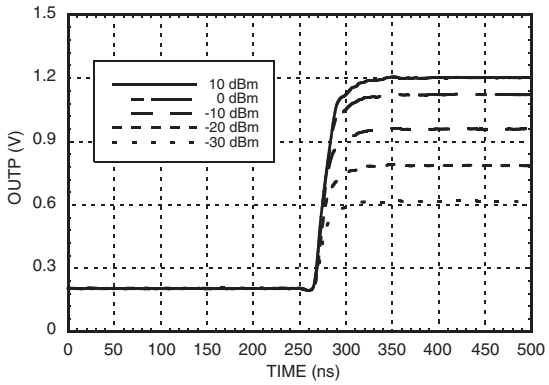
Output Response [1] Fall Time C1 = Open



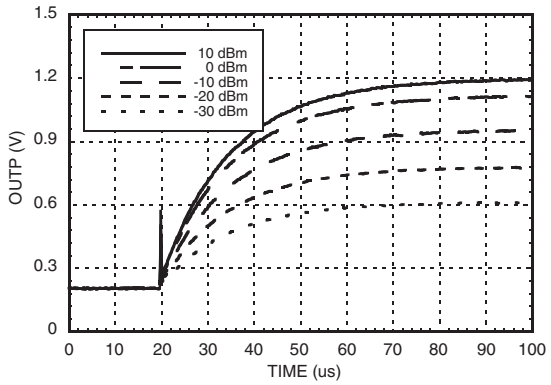
Output Response Fall Time [1] C1 = 10nF



Output Response Rise Time [1] C1 = Open



Output Response Rise Time [1] C1 = 10nF



[1] 900 MHz, Switched CW-Tone

HMC713LP3E

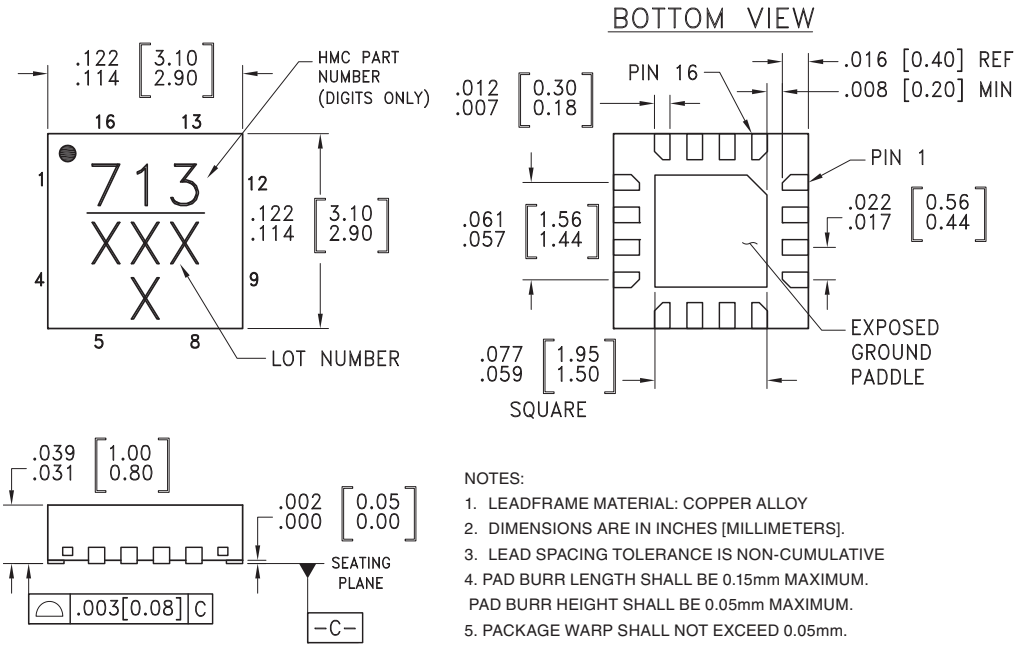
54 dB, LOGARITHMIC DETECTOR / CONTROLLER, 50 - 8000 MHz

Absolute Maximum Ratings

Vcc	0 to +5.6V
EN Input Voltage	0 to +5.6V
VSET Input Voltage	0 to +5.6V
OUTP Output Current	5 mA
OUTN Output Current	5 mA
RF Input Power	12 dBm
Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 5.43 mW/°C above 85°C)	0.22 Watts
Thermal Resistance (R_{th}) (junction to lead)	184 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

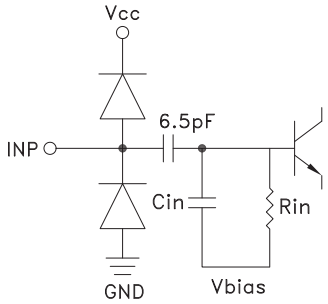
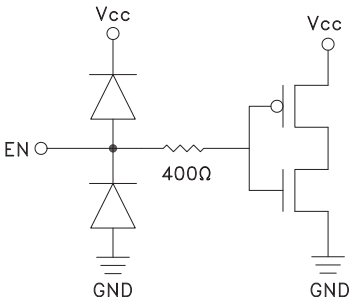
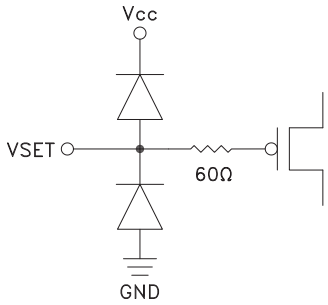
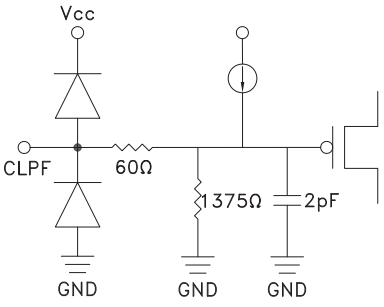
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

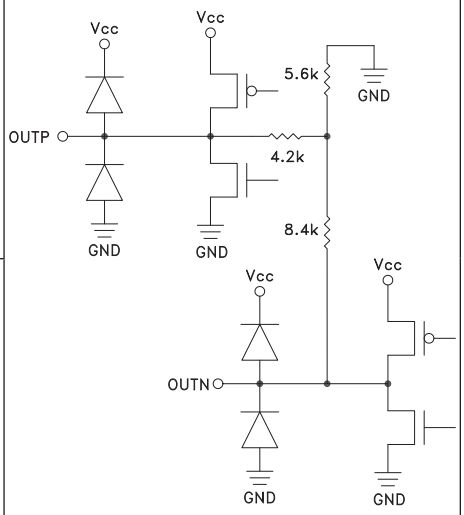
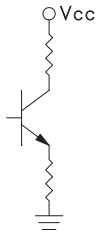
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC713LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	713 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

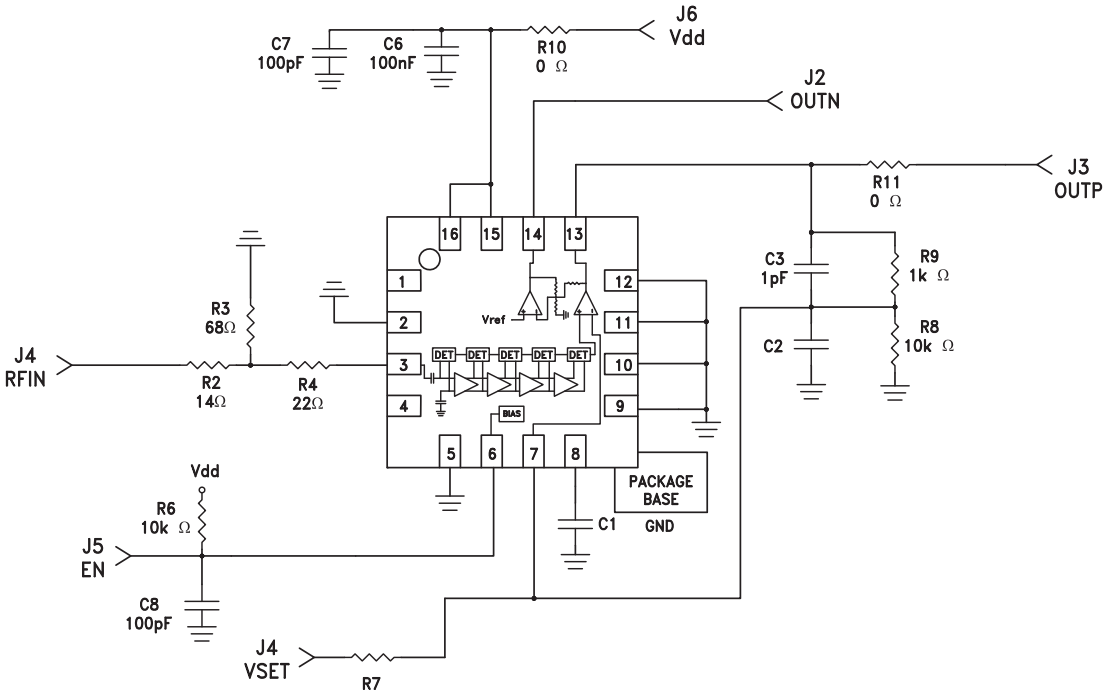
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4	N/C	These pins are not connected internally.	
2, 5, 9 - 12	GND	These pins and package bottom must be connected to RF/DC ground.	
3	RFIN	RF input pin.	
6	EN	Enable pin. Apply VEN >0.8 x Vcc for normal operation. Apply VEN <0.2xVcc to disable the HMC713LP3E and reduce supply current to 0.4mA.	
7	VSET	Set point input for controller mode. Connect to OUTP with the resistor network shown in evaluation board drawing for detector mode.	
8	CLPF	Connection for ground referenced external lowpass filter capacitor.	

Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
13	OUTP	Logarithmic output that converts the input power to a DC level in controller mode. Output voltage increases with increasing amplitude	
14	OUTN	Inverted logarithmic output. OUTN= 2.55 - 2 x OUTP	
15, 16	Vcc	Bias Supply. Connect supply voltage to these pins with appropriate filtering.	

Application & Evaluation PCB Schematic



Notes

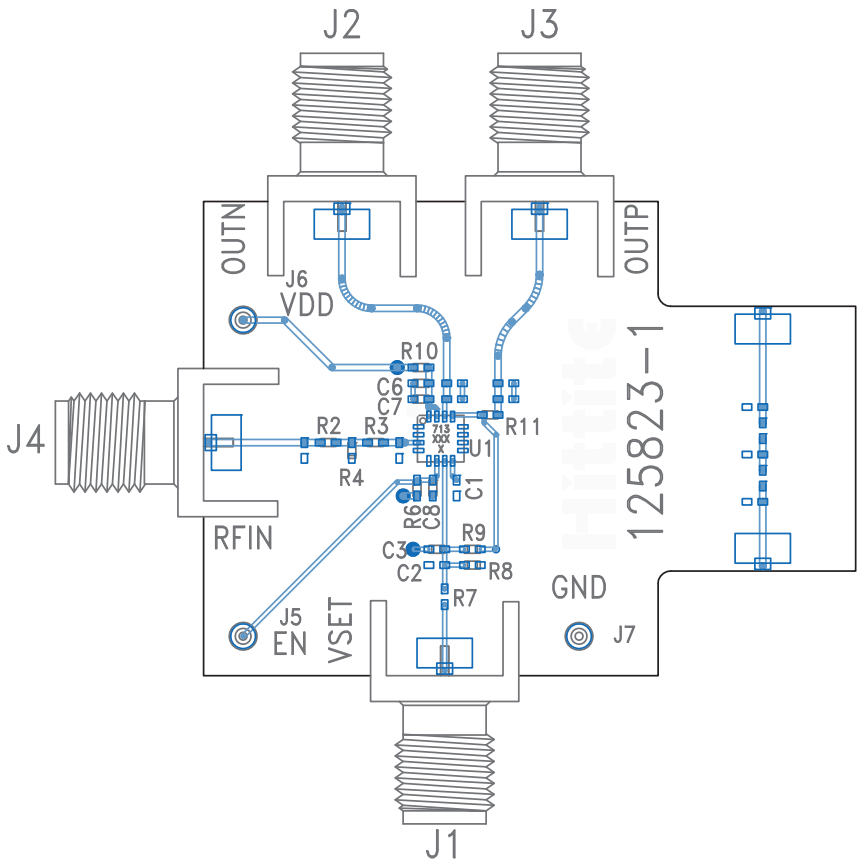
Note 1: The HMC713LP3E evaluation board is pre-assembled for single-ended input, and detector/RSSI mode.

Note 2: For detector mode, connect high impedance volt meter to the OUTP / OUTN port.

Note 3: For controller mode, remove R9 & C3 and install 1k Ω resistor (R7, not included) and 100pF capacitor (C2, not included), then make appropriate connection to OUTP and VSET. In controller mode, the OUTP / OUTN output can be used to drive a variable gain amplifier, or a variable attenuator, either directly or through a buffer or microcontroller. VSET should be connected to an external supply, typically between +0.2 and +1.2V.

Note 4: An external capacitance C1 can be connected to CLPF port for additional filtering of OUTP and OUTN outputs..

Evaluation PCB



List of Materials for Evaluation PCB 125825 [1]

Item	Description
J1 - J4	PC Mount SMA Connector
J5 - J7	DC Pin
C3	1 pF Capacitor, 0402 Pkg.
C6	0.1 µF Capacitor, 0402 Pkg.
C7, C8	100 pF Capacitor, 0402 Pkg.
R2	14Ω Resistor, 0402 Pkg.
R3	68Ω Resistor, 0402 Pkg.
R4	22Ω Resistor, 0402 Pkg.
R6, R8	10kΩ Resistor, 0402 Pkg.
R9	1kΩ Resistor, 0402 Pkg.
R10, R11	0Ω Resistor, 0402 Pkg.
U1	HMC713LP3E Logarithmic Amplifier
PCB [2]	125823 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Notes: