HMC722LC3C

v03.1209

13 Gbps, FAST RISE TIME AND/NAND/OR/NOR GATE, w/ PROGRAMMABLE OUTPUT VOLTAGE

Typical Applications

The HMC722LC3C is ideal for:

- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 13 Gbps
- Digital Logic Systems up to 13 GHz
- NRZ-to-RZ Conversion

Features

Supports High Data Rates: up to 13 Gbps

Differential & Singe-Ended Operation

Fast Rise and Fall Times: 19 / 18 ps

Low Power Consumption: 230 mW typ.

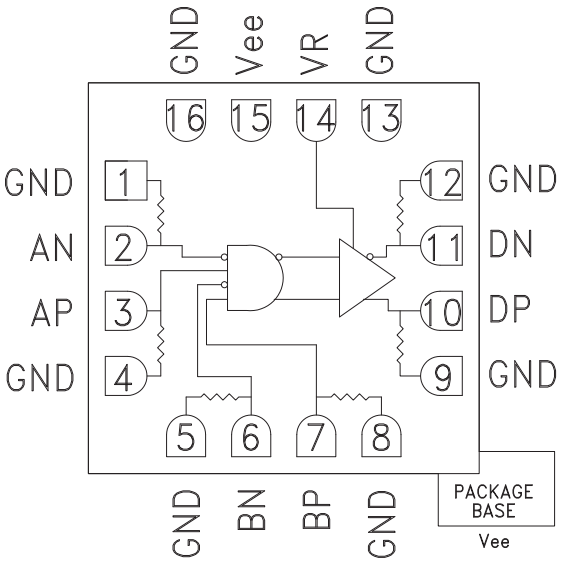
Programmable Differential
Output Voltage Swing: 600 - 1100 mV

Propagation Delay: 95 ps

Single Supply: -3.3V

16 Lead Ceramic 3x3mm SMT Package: $9mm^2$

Functional Diagram



General Description

The HMC722LC3C is an AND/NAND/OR/NOR function designed to support data transmission rates of up to 13 Gbps, and clock frequencies as high as 13 GHz. The HMC772LC3C may be easily configured to provide any of the following logic functions: AND, NAND, OR and NOR. The HMC722LC3C also features an output level control pin, VR, which allows for loss compensation or for signal level optimization.

All input signals to the HMC722LC3C are terminated with 50 Ohms to ground on-chip, and may be either AC or DC coupled. The differential outputs of the HMC722LC3C may be either AC or DC coupled. Outputs can be connected directly to a 50 Ohm to ground terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to a non-ground DC voltage. The HMC722LC3C operates from a single -3.3V DC supply, and is available in a ceramic RoHS compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25 °C, Vee = -3.3V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		-3.6	-3.3	-3.0	V
Power Supply Current			70		mA
Maximum Data Rate			13		Gbps
Maximum Clock Rate			13		GHz
Input High Voltage		-0.5		0.5	V
Input Low Voltage		-1.0		0.0	V
Input Return Loss	Frequency <13 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		550		mVp-p
	Differential, peak-to-peak		1100		mVp-p
Output High Voltage			-10		mV

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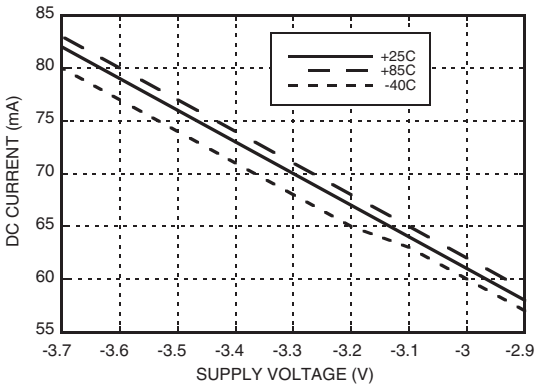
Electrical Specifications, (continued)

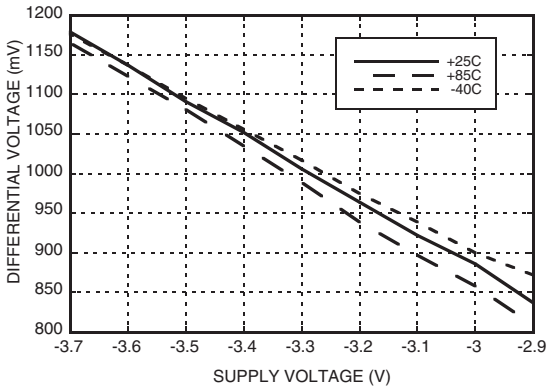
Parameter	Conditions	Min.	Typ.	Max	Units
Output Low Voltage			-570		mV
Output Rise / Fall Time	Differential, 20% - 80%		19 / 18		ps
Output Return Loss	Frequency <13 GHz		10		dB
Small Signal Gain			27		dB
Random Jitter Jr	rms			0.2	ps rms
Deterministic Jitter, Jd	peak-to-peak, 2^{15}-1 PRBS input [1]		2		ps, p-p
Propagation Delay, td			95		ps

[1] Deterministic jitter calculated by simultaneously measuring the jitter of a 300 mV, 13 GHz, 2^{15}-1 PRBS input, and a single-ended output

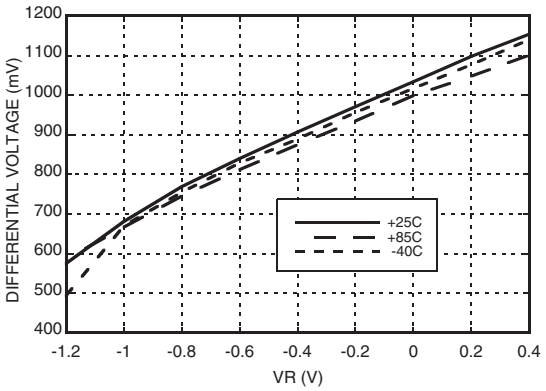
DC Current vs. Supply Voltage [1] [2]



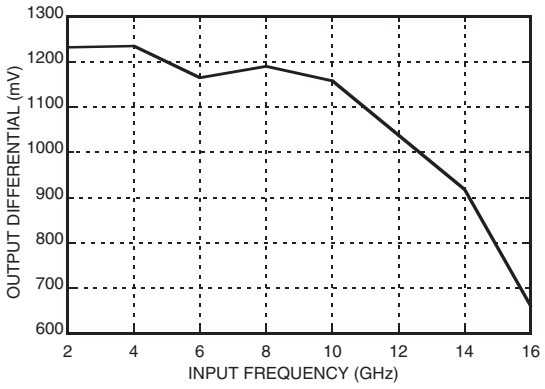
Output Differential vs. Supply Voltage [1] [3]



Output Differential vs. VR [2]



Output Differential vs. Frequency [3]



[1] VR = 0.0V [2] Frequency = 13 GHz [3] Frequency = 10 GHz

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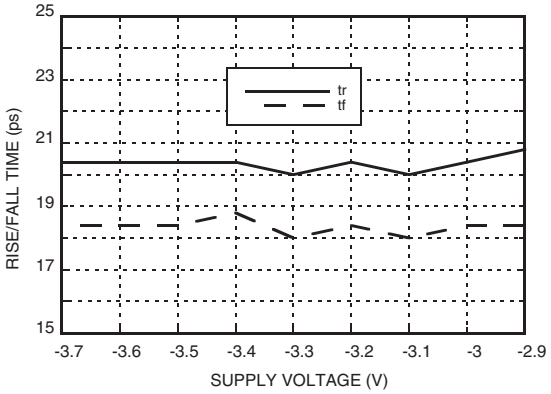
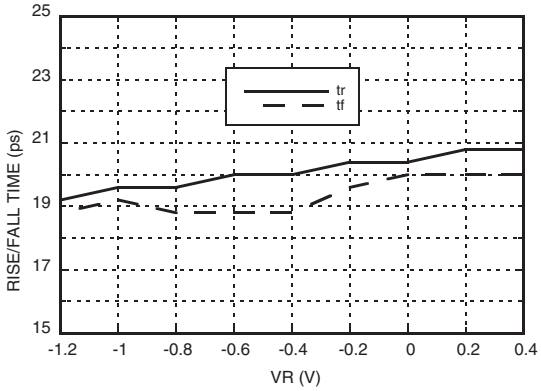
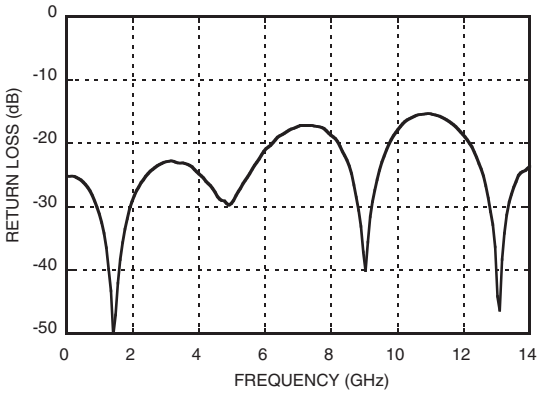
Rise / Fall Time vs. Supply Voltage [3]



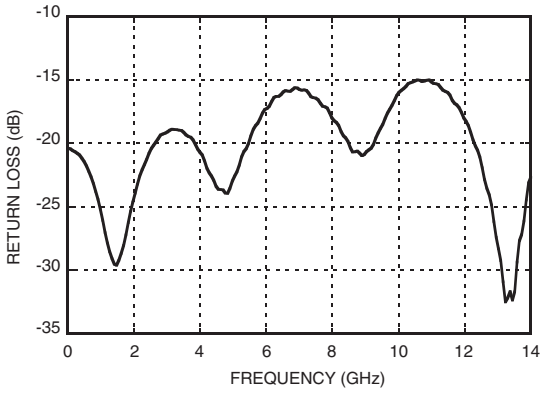
Rise / Fall Time vs. VR [3]



Input Return Loss vs. Frequency



Output Return Loss vs. Frequency



[1] VR = 0.0V [2] Frequency = 13 GHz [3] Frequency = 10 GHz

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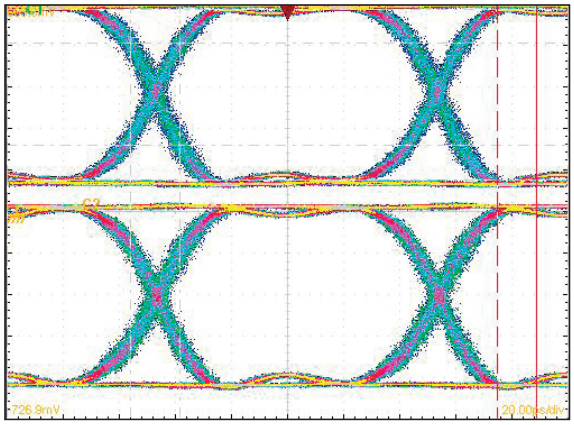
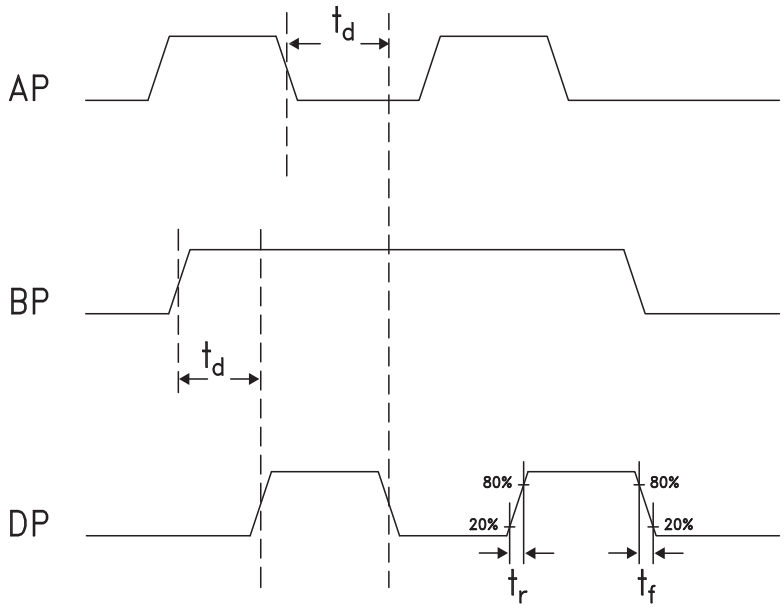
Eye Diagram



[1] Test Conditions:
Pattern generated with an Agilent N4903A Serial BERT.
Eye Diagram presented on a Tektronix CSA 8000.
Device input = 10 Gbps PN code, Vin = 300mVp-p differential.

Timing Diagram



Truth Table

Input		Outputs
A	B	D
L	L	L
L	H	L
H	L	L
H	H	H
Notes: A = AP - AN B = BP - BN D = DP - DN	H - Positive voltage level L - Negative voltage level	

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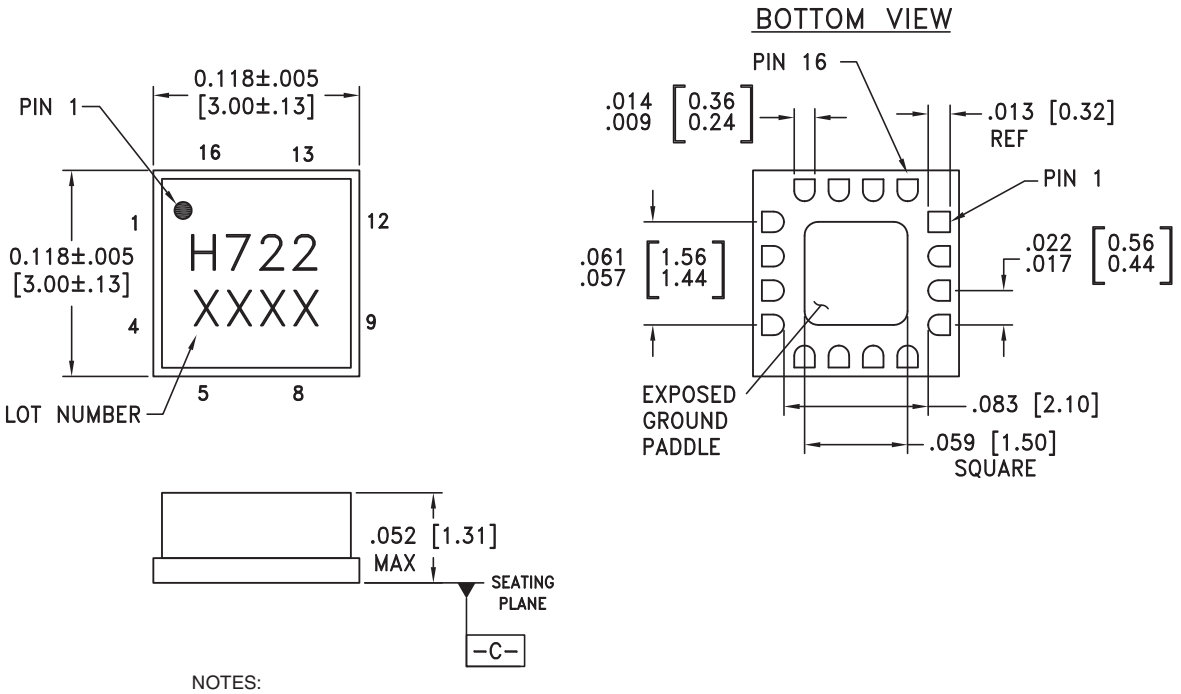
Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75V to +0.5V
Input Signals	-2V to +0.5V
Output Signals	-1.5V to +1V
Storage Temperature	-65°C to +150°C
Operating Temperature	-40°C to +85°C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. GROUND PADDLE MUST BE SOLDERED TO Vee.

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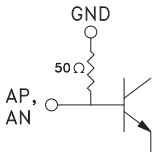
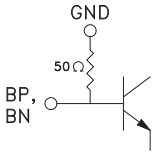
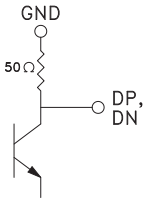
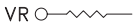
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12	GND	Signal Grounds	
2, 3	AN, AP	Clock / Data Input A	
6, 7	BN, BP	Clock / Data Input B	
10, 11	DP, DN	Clock / Data Output	
13, 16	GND	Supply Ground	
14	VR	Output level control. Output level may be adjusted by either applying a voltage to VR per “Output Differential vs. VR” plot.	
15, Package Base	Vee	Negative Supply	

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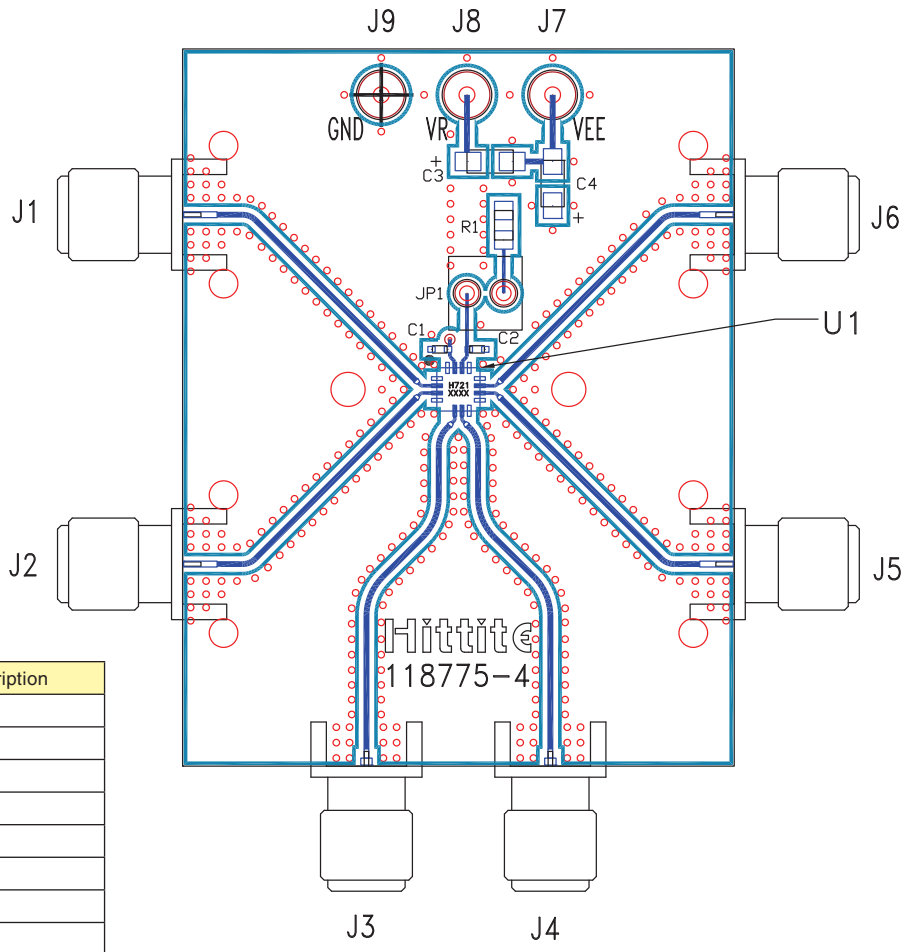
Evaluation PCB



Item	Description
J1	AN
J2	AP
J3	BN
J4	BP
J5	DP
J6	DN
J7	Vee
J8	VR
J9	GND

List of Materials for Evaluation PCB 118777 [1]

Item	Description
J1 - J6	PCB Mount SMA RF Connectors
J7 - J9	DC Pin
C1, C2	100 pF Capacitor, 0402 Pkg.
C3, C4	4.7 µF Capacitor, Tantalum
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC722LC3C High Speed Logic, AND / NAND / OR / NOR
PCB [2]	118775 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed package base should be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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Application Circuit