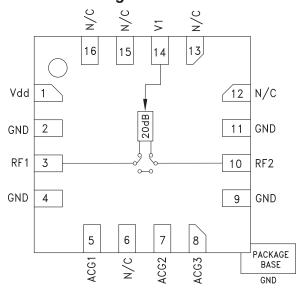


Typical Applications

The HMC802LP3E is ideal for both RF and IF applications:

- Test Equipment and Sensors
- ISM, MMDS, WLAN, WiMAX, WiBro
- Microwave Radio & VSAT
- Cellular Infrastructure

Functional Diagram



Features

± 0.6 dB Typical Step Error Low Insertion Loss: 3 dB

High IP3: +55 dBm Single Control Line

TTL/CMOS Compatible Control

Single +5V Supply

16 Lead 3x3mm SMT Package: 9mm²

General Description

The HMC802LP3E is a broadband bidirectional 1-bit GaAs IC digital attenuator in a low cost leadless surface mount package. This single positive control line digital attenuator utilizes off chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. Covering DC to 10 GHz, the insertion loss is less than 3 dB typical and attenuation accuracy is excellent at ± 0.6 dB typical. The attenuator also features a high IIP3 of ± 5.5 dBm. One TTL/CMOS control input is used to select the attenuation state and a single Vdd bias of ± 5.5 is required.

Electrical Specifications, $T_A = +25^{\circ}$ C, With Vdd = +5V & Vctl = 0/+5V

Parameter	Frequency (GHz)	Min.	Тур.	Max.	Units
Insertion Loss	DC - 4 GHz 4 - 8 GHz 8 - 10 GHz		1.5 3.0 3.5	2.5 4.0 4.5	dB dB dB
Attenuation Range	DC - 10 GHz		20		dB
Return Loss (RF1 & RF2, Both States)	DC - 6 GHz 6 - 10 GHz		18 12		dB dB
Attenuation Accuracy: (Referenced to Insertion Loss)	DC - 8 GHz 8 - 10 GHz		± 0.4 ± 0.8	± 0.6 ± 1.2	dB dB
Input Power for 0.1 dB Compression	DC - 0.4 GHz 0.4 - 10 GHz		20 30*		dBm dBm
Input Third Order Intercept Point (Two-Tone Input Power= 0 dBm Each Tone)	DC - 0.4 GHz 0.4 - 10 GHz		45 55		dBm
Switching Characteristics					
tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)	DC - 10 GHz		120 150		ns ns

^{*} For frequencies greater than 0.4 GHz, the 0.1 dB compression point is greater than the absolute maximum RF input power of 30 dBm.

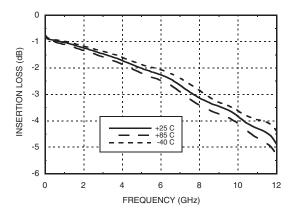


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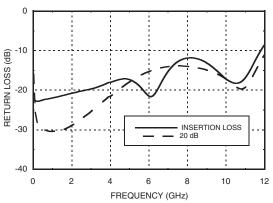


20 dB GaAs MMIC 1-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 10 GHz

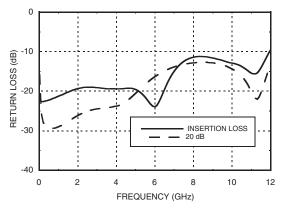
Insertion Loss



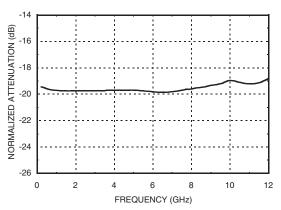
Input Return Loss



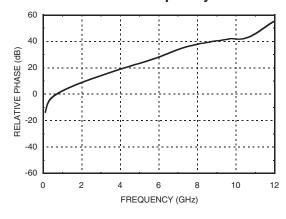
Output Return Loss



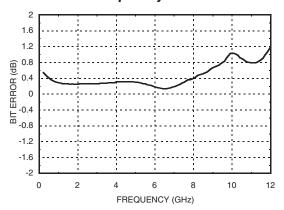
Relative Attenuation



Relative Phase vs. Frequency



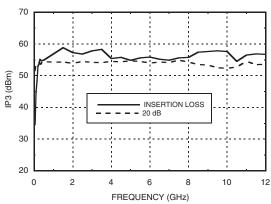
Bit Error vs. Frequency



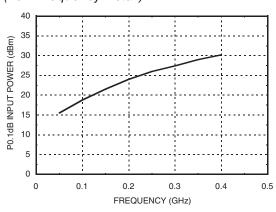




Input IP3 vs. Frequency

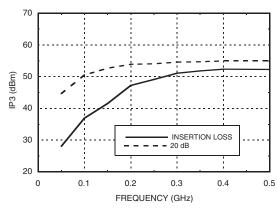


Input Power for 0.1 dB Compression* (Low Frequency Detail)



Input IP3 vs. Frequency

(Low Frequency Detail)



Truth Table

Control Voltage Input	Attenuation State
V1	RF1 - RF2
High	Reference Insertion Loss
Low	20 dB

Bias Voltage & Current

$Vdd = +5 Vdc \pm 10\%$		
Vdd (Vdc)	ldd (Typ.) (mA)	
4.5	0.21	
5.0	0.23	
5.5	0.25	

Control Voltage

State	Bias Condition		
Low	0 to +0.8V @ -1 μA Typ.		
High	+2 to +5V @ 30 μA Typ.		
Note: Vdd = +5V			

^{*} For frequencies greater than 0.4 GHz, the 0.1 dB compression point is greater than the absolute maximum RF input power of 30 dBm.



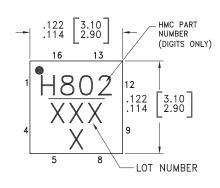


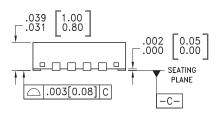
Absolute Maximum Ratings

RF Input Power (DC - 10 GHz)	+30 dBm
Control Voltage Range (V1)	-1 to Vdd + 1V
Bias Voltage (Vdd)	+7 Vdc
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 12 mW/°C above 85 °C)	0.783 W
Thermal Resistance (channel to ground paddle)	83 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A



Outline Drawing





BOTTOM VIEW

NOTES:

- 1. LEADFRAME MATERIAL: COPPER ALLOY
- 2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
- 3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
- PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM.
 PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
- 5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
- ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
- 7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC802LP3E RoHS-compliant Low Stress Injection Molded Plastic		100% matte Sn	MSL1 [1]	H802 XXXX

^[1] Max peak reflow temperature of 260 °C

^{[2] 4-}Digit lot number XXXX

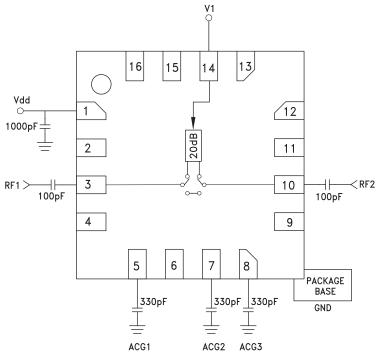




Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	Vdd	Supply Voltage.	
2, 4, 9, 11	GND	These pins and the exposed ground paddle must be connected to RF/DC ground.	⊖ GND =
3, 10	RF1, RF2	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	RF1 RF2
5, 7, 8	ACG1, ACG2, ACG3	External capacitor to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible.	
6, 12, 13, 15, 16	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
14	V1	See truth table and control voltage table.	V1 0 180K V1 0 =

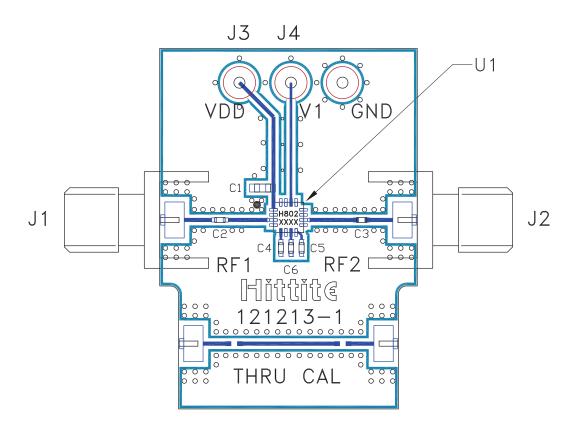
Application Circuit







Evaluation PCB



List of Materials for Evaluation PCB 127103 [1]

Item	Description
J1, J2	PCB Mount SMA Connector
J3, J4	DC Connector
C1	1000 pF Capacitor, 0603 Pkg.
C2, C3	100 pF Capacitor, 0402 Pkg.
C4 - C6	330 pF Capacitor, 0402 Pkg.
U1	HMC802LP3E Digital Attenuator
PCB [2]	121213 Evaluation PCB

^[1] Reference this number when ordering complete evaluation PCB

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

^[2] Circuit Board Material: Rogers 4350