HMC870LC5

MZ OPTICAL MODULATOR DRIVER, DC - 20 GHz

Typical Applications

The HMC870LC5 is ideal for:

- 10 Gbps NRZ MZ & Low V_{Π} Modulator Driver
- 10 Gbps RZ Transmission
- 40 Gbps DQPSK
- Broadband Gain Block for Test & Measurement Equipment
- Military & Space

Features

Wide Supply Range from 3.3V to 7V

Adjustable Output Amplitude: 2.5 to 8 Vp-p

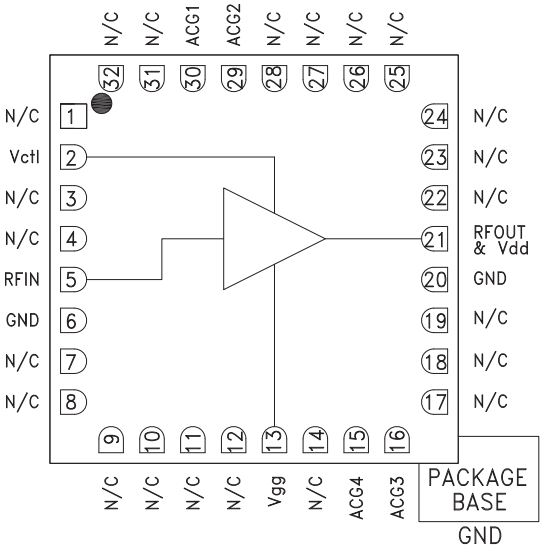
Low Additive RMS Jitter, <300 fs

Low DC Power Consumption
1W for Vout = 8 Vp-p at Vdd = 7V

Cross Point Adjustment

32 Lead 5x5mm SMT Package: 25mm²

Functional Diagram



General Description

The HMC870LC5 is a GaAs MMIC pHEMT Distributed Driver Amplifier packaged in a leadless 5x5 mm surface mount package which operates between DC and 20 GHz. The amplifier provides 17 dB of gain, 8Vp-p saturated output swing and features output swing cross point adjustment. Gain flatness is excellent at ±0.5 dB as well as very low additive RMS jitter of 300 fs for 10 Gbps operation. HMC870LC5 provides Metro and Long Haul designers with scalable power dissipation for varying output drive requirements. (<0.4W at Vout = 3.6 Vp-p and <1W at Vout = 8.5 Vp-p) The HMC870LC5 has a very wide supply (Vdd) operating range from +3.3V to +7V, and the RF I/Os are internally matched to 50 Ohms.

Electrical Specifications, T_A = +25° C, Vdd = 7V, Vctl = 1V, Idd = 165mA*

Parameter	Conditions	Min.	Typ.	Max.	Units
Gain	Frequency = 1 - 8 GHz Frequency = 8 - 16 GHz Frequency = 16 - 20 GHz	14 13 12	17.5 16.5 16		dB dB dB
Small Signal Bandwidth	3-dB cutoff		20		GHz
Input Return Loss	Frequency = 1 - 10 GHz Frequency = 10 - 20 GHz		20 15		dB dB
Output Return Loss	Frequency = 1 - 10 GHz Frequency = 10 - 20 GHz		20 15		dB dB
Gain Variation over Temperature	Frequency = 1 - 10 GHz Frequency = 10 - 20 GHz		0.015 0.032	0.02 0.045	dB/°C dB/°C
Group Delay Variation	Frequency = 1 - 12 GHz		±15		ps
Saturated Output Power (Psat)	Frequency = 1 - 12 GHz Frequency = 12 - 20 GHz		24 23		dBm dBm

** Adjust Vgg between -2V to 0V to achieve Idd= 165 mA typical.*

Electrical Specifications, T_A = +25° C, Vdd = 7V, Vctl = 1V, Idd = 165mA* Continued

Parameter	Conditions	Min.	Typ.	Max.	Units
Output Power for 1 dB Compression (P1dB)	Frequency = 1 - 12 GHz Frequency = 12 - 20 GHz	19 18	22 21		dBm dBm
Rise Time [1]	20% - 80%		20		ps
Fall Time [1]	20% - 80%		20		ps
Additive RMS Jitter [2]				300	fs
Supply Current (Idd) (Vgg = -0.6V Typ.)			165		mA
Bias Current Adjust (Vgg)		-2		0	V
Output Voltage Adjust (Vctl)		0		2	V

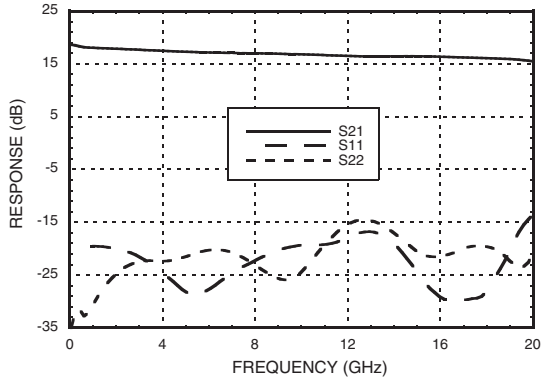
[1] Data input = 22.5 Gbps NRZ PRBS 2^{23}-1 pattern, 1.2 Vp-p.
[2] RMS jitter is calculated with 22.5 Gbps 10101... pattern.
* Adjust Vgg between -2V to 0V to achieve Idd = 165 mA typical.

Electrical Specifications, T_A = +25° C, Vdd = 5V, Vctl = 1V, Idd = 140mA*

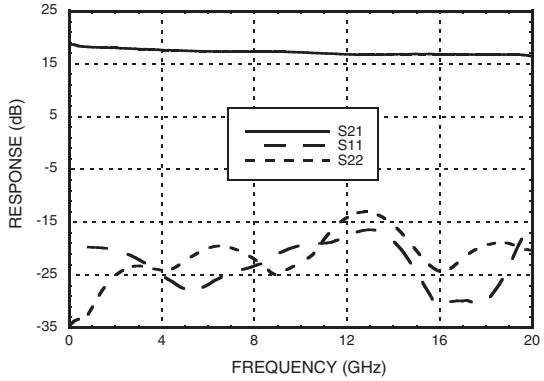
Parameter	Conditions	Min.	Typ.	Max.	Units
Gain	Frequency = 1 - 8 GHz Frequency = 8 - 16 GHz Frequency = 16 - 20 GHz	14 13.5 12	17.5 17.0 16.5		dB dB dB
Small Signal Bandwidth	3-dB cutoff		20		GHz
Input Return Loss	Frequency = 1 - 10 GHz Frequency = 10 - 20 GHz		20 15		dB dB
Output Return Loss	Frequency = 1 - 10 GHz Frequency = 10 - 20 GHz		15 10		dB dB
Gain Variation over Temperature	Frequency = 1 - 10 GHz Frequency = 10 - 20 GHz		0.016 0.029	0.02 0.045	dB/°C dB/°C
Group Delay Variation	Frequency = 1 - 12 GHz		±15		deg
Saturated Output Power (Psat)	Frequency = 1 - 12 GHz Frequency = 12 - 20 GHz		22.5 22		dBm dBm
Output Power for 1 dB Compression (P1dB)	Frequency = 1 - 12 GHz Frequency = 12 - 20 GHz	18 17	20.5 20		dBm dBm
Rise Time [1]	20% - 80%		20		ps
Fall Time [1]	20% - 80%		20		ps
Additive RMS Jitter [2]				300	fs
Supply Current (Idd) (Vgg = -0.6V Typ.)			140		mA
Bias Current Adjust (Vgg)		-2		0	V
Output Voltage Adjust (Vctl)		0		2	V

[1] Data input = 22.5 Gbps NRZ PRBS 2^{23}-1 pattern, 1.2 Vp-p.
[2] RMS jitter is calculated with 22.5 Gbps 10101... pattern.
* Adjust Vgg between -2V to 0V to achieve Idd = 140 mA typical.

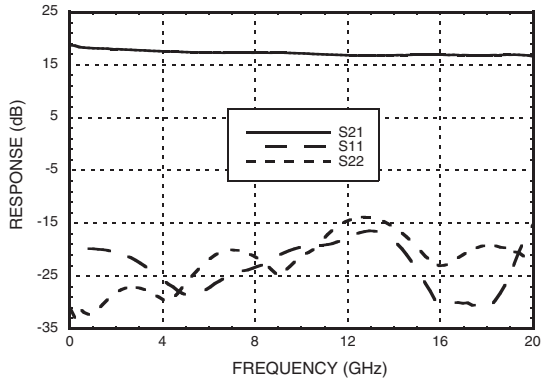
Gain & Return Loss @ Vdd = 7V



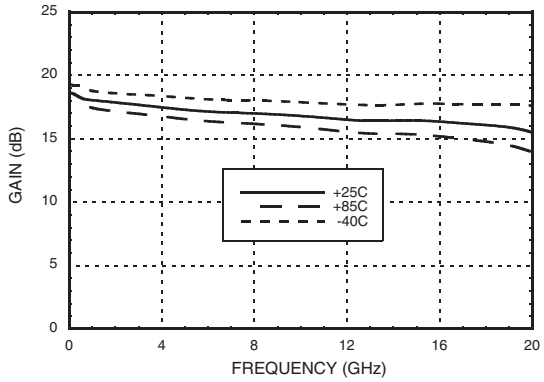
Gain & Return Loss @ Vdd = 5V



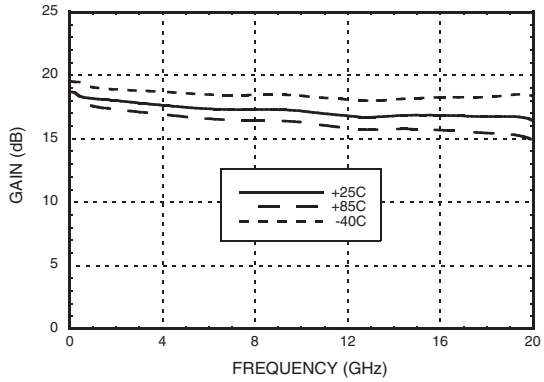
Gain & Return Loss @ Vdd = 3.3V



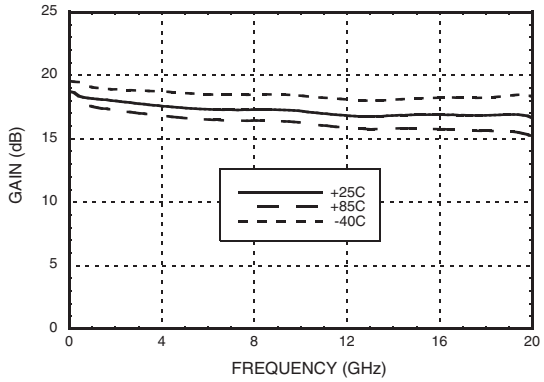
Gain vs. Temperature @ Vdd = 7V



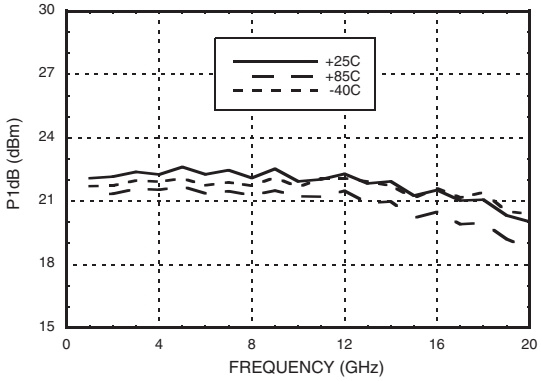
Gain vs. Temperature @ Vdd = 5V



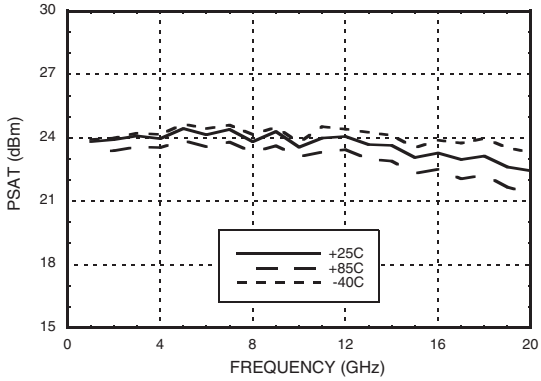
Gain vs. Temperature @ Vdd = 3.3V



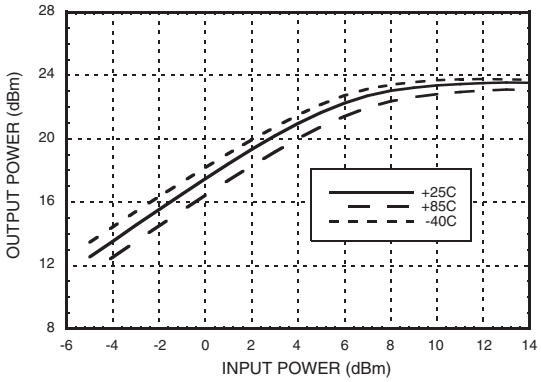
P1dB vs. Temperature @ Vdd = 7V



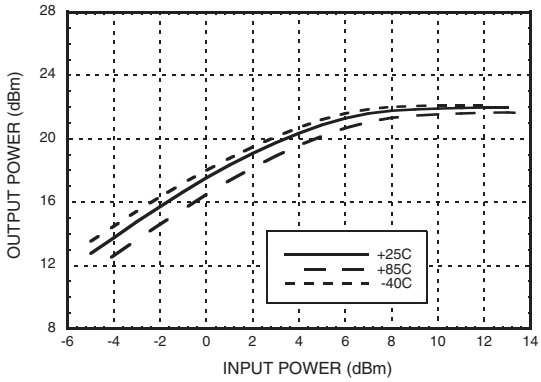
Psat vs. Temperature @ Vdd = 7V



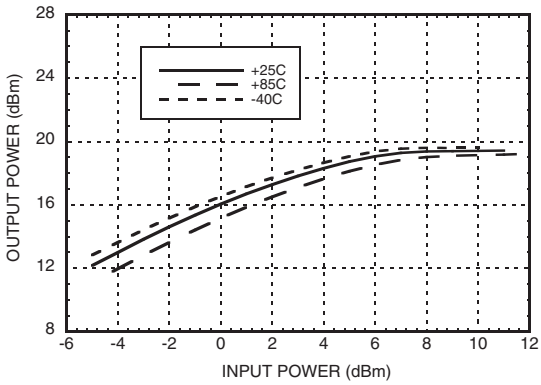
Output Power vs. Input Power @ 10 GHz, Vdd = 7V



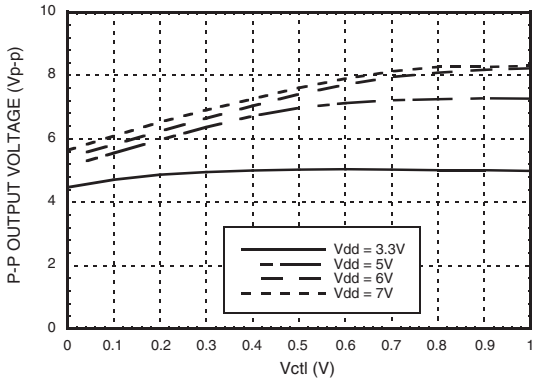
Output Power vs. Input Power @ 10 GHz, Vdd = 5V



Output Power vs. Input Power @ 10 GHz, Vdd = 3.3V

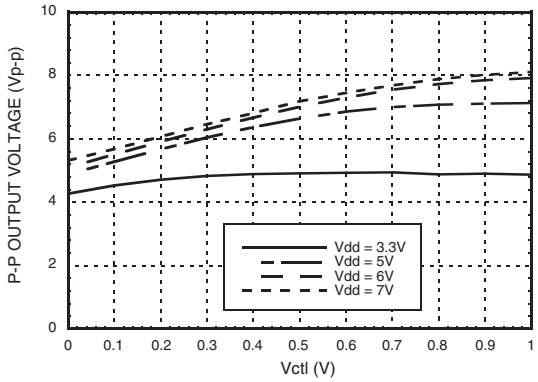


Peak-to-Peak Output Voltage vs. Vdd @ 11.25 Gbps [1]

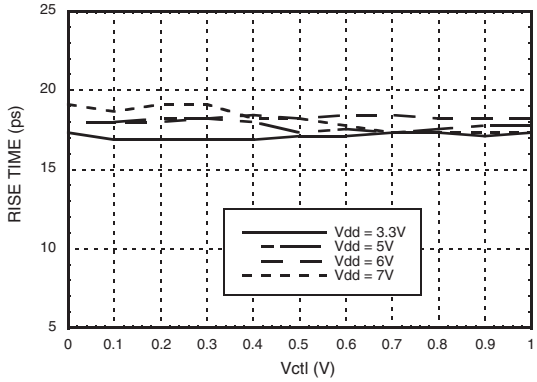


[1] Data input = 11.25 Gbps NRZ PRBS 2^{23}-1 pattern, 1.2 Vp-p.

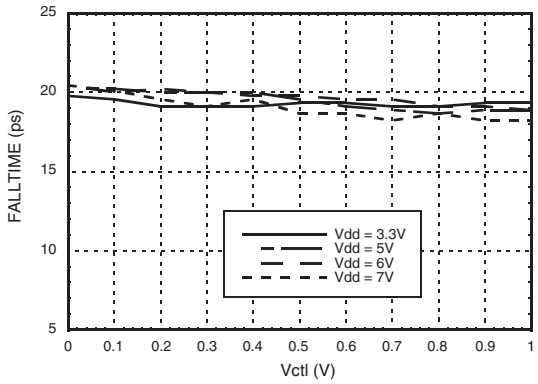
Peak-to-Peak Output Voltage vs. Vdd @ 22.5 Gbps [1]



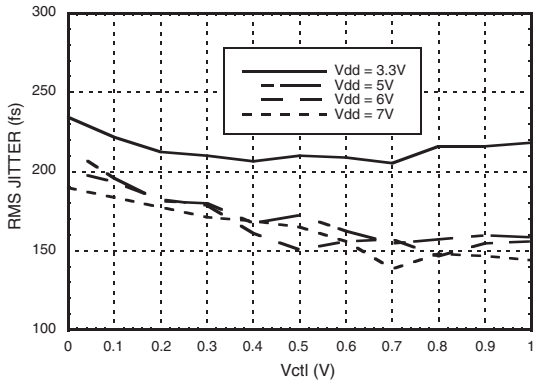
Rise Time vs. Vdd @ 22.5 Gbps [1]



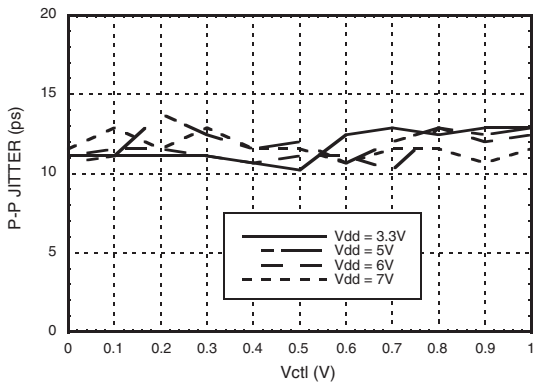
Fall Time vs. Vdd@ 22.5 Gbps [1]



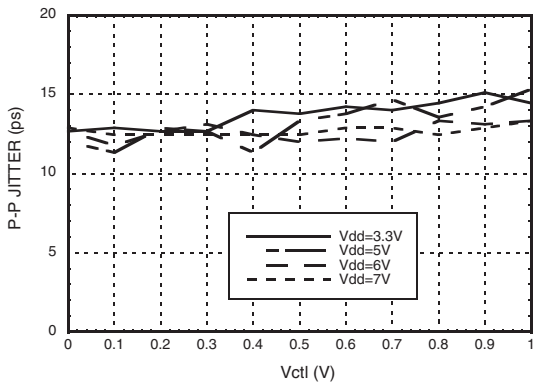
RMS Jitter vs. Vdd @ 22.5 Gbps [2]



Peak-to-Peak Jitter vs. Vdd @ 11.25 Gbps [3][4]



Peak-to-Peak Jitter vs. Vdd @ 22.5 Gbps [1][4]



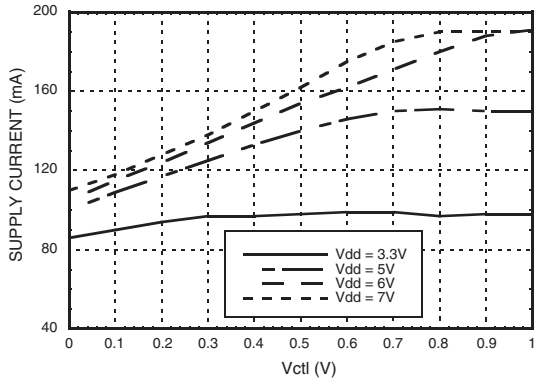
[1] Data input = 22.5 Gbps NRZ PRBS 2^{23}-1 pattern, 1.2 Vp-p.

[2] RMS jitter is measured with 22.5 Gbps 10101... pattern.

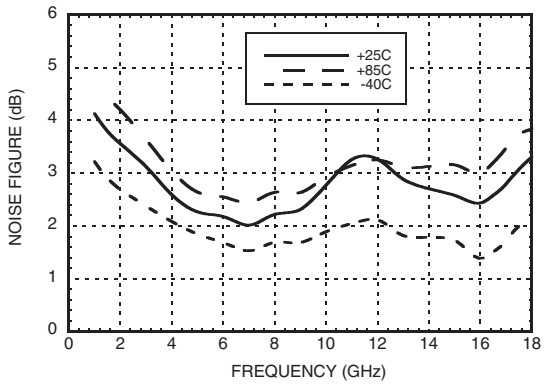
[3] Data input = 11.25 Gbps NRZ PRBS 2^{23}-1 pattern, 1.2 Vp-p.

[4] Source jitter was not de-embedded.

Supply Current vs. Vdd @ 22.5 Gbps [1]

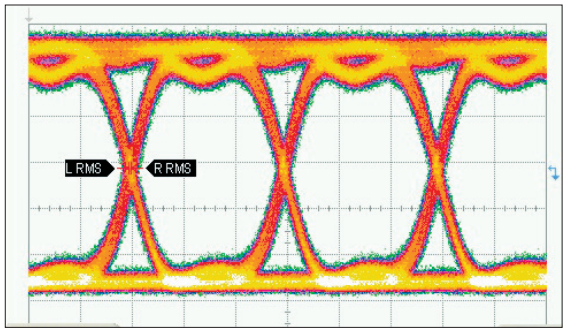


Noise Figure vs. Temperature @ Vdd = 7V



[1] Data Input = 22.5 Gbps NRZ PRBS 223-1 pattern, 1.2 Vp-p

11.25 Gbps NRZ Output Eye Diagram

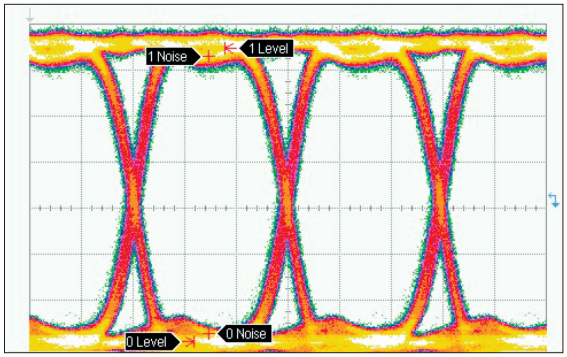


	Measurements			
	Current	Min	Max	Units
Eye Amplitude	3.6	3.6	3.6	V
Rise Time	20	20	20	ps
Fall Time	21.33	20.67	22	ps
Jitter RMS	1.893	1.87	2.072	ps

Time scale: 30.0 ps/div
Amplitude scale: 762 mV/div

Vdd = 3.3V, Vin: 11.25 Gbps NRZ PRBS 2^{31}-1, 0.5 Vp-p
Vout: 3.6Vp-p
Vctl = 1V

11.25 Gbps NRZ Output Eye Diagram

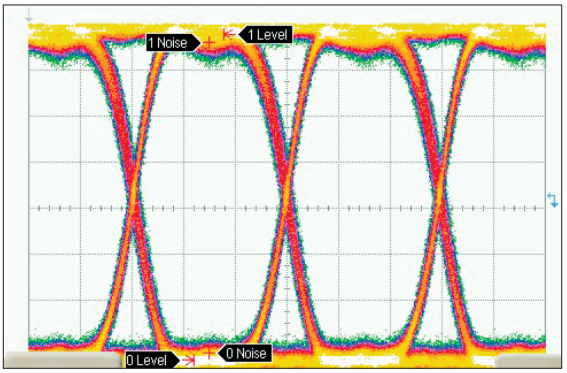


	Measurements			
	Current	Min	Max	Units
Eye Amplitude	7.47	7.47	7.47	V
SNR	17.97	17.88	18.12	V/V

Time scale: 30.0 ps/div
Amplitude scale: 1.17 V/div

Vdd = 5V, Vin: 11.25Gbps NRZ PRBS 2^{31}-1, 1.2V p-p,
Vout: 7.5Vp-p
Vctl = 1V

11.25 Gbps NRZ Output Eye Diagram *(Continued)*

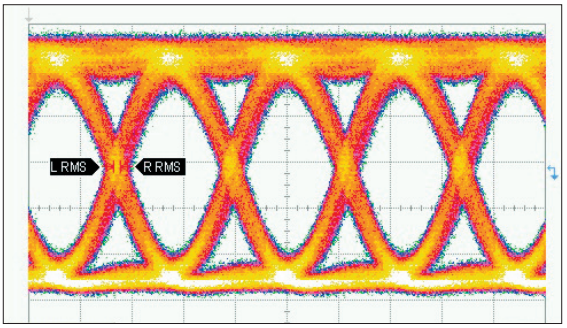


	Measurements			
	Current	Min	Max	Units
Eye Amplitude	8.26	8.26	8.27	V
SNR	22.35	22.26	22.51	V/V

Time scale: 30.0 ps/div
Amplitude scale: 1.17 V/div

Vdd = 7V, Vin: 11.25Gbps NRZ PRBS 2^{31}-1, 1.2V p-p,
Vout: 8.3Vp-p
Vctl = 1V

22.5 Gbps NRZ Output Eye Diagram

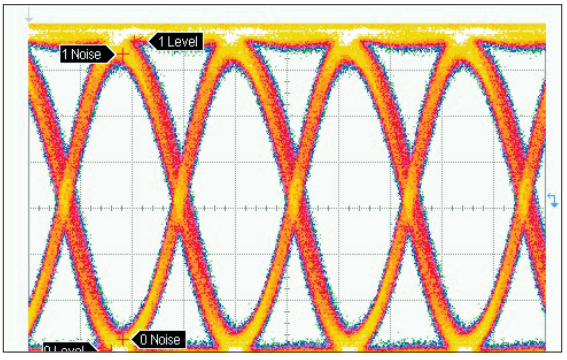


	Measurements			
	Current	Min	Max	Units
Eye Amplitude	3.53	3.53	3.54	V
Rise Time	18.22	17.33	18.22	ps
Fall Time	20.44	19.56	20.89	ps
Jitter RMS	2.417	2.187	2.422	ps

Time scale: 20.0 ps/div
Amplitude scale: 762 mV/div

Vdd = 3.3V, Vin: 22.5Gbps NRZ PRBS 2^{31}-1, 0.5V p-p,
Vout: 3.5Vp-p
Vctl = 1V

22.5 Gbps NRZ Output Eye Diagram

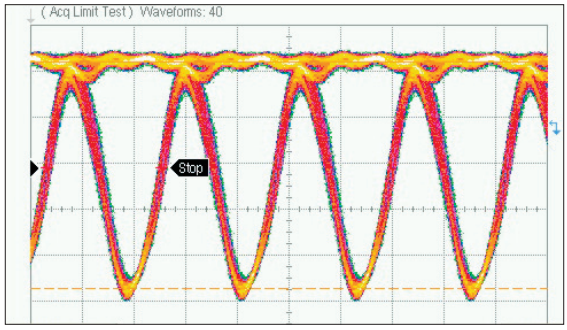


	Measurements			
	Current	Min	Max	Units
Eye Amplitude	7.85	7.84	7.85	V
SNR	13.74	13.69	14.07	V/V

Time scale: 20.0 ps/div
Amplitude scale: 1.17 V/div

Vdd = 7V, Vin: 22.5Gbps NRZ PRBS 2^{31}-1, 1.2 V p-p,
Vout: 7.9Vp-p
Vctl = 1V

11.25 Gbps RZ Output Eye Diagram

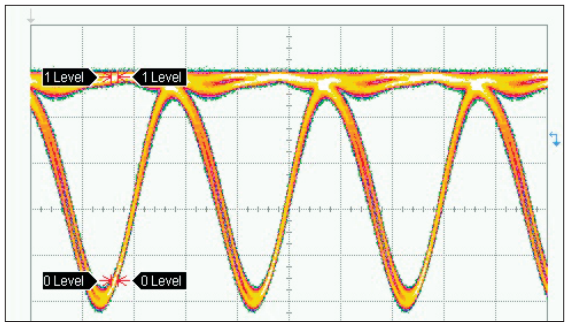


	Measurements	
	Current	Units
Jitter RMS	1.93	ps
Bit Rate	11.2	Gb/s

Time scale: 40.0 ps/div
Amplitude scale: 1.22 V/div

Vdd = 3.3V, Vin: 11.25Gbps RZ PRBS 2^{31}-1, 0.3V p-p,
Vout: 2.9Vp-p
Vctl = 1V

11.25 Gbps RZ Output Eye Diagram



	Measurements			
	Current	Min	Max	Units
Duty Cycle	51.5	50.4	57.1	%
SNR	20.85	13.35	20.96	V/V
Jitter RMS	1.753	1.689	1.795	ps
Eye Amplitude	2.85	2.37	2.86	V

Time scale: 30.0 ps/div
Amplitude scale: 647 mV/div

Vdd = 5V, Vin: 11.25Gbps RZ PRBS 2^{31}-1, 1.2V p-p,
Vout: 6Vp-p
Vctl = 1V

Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+9V
Gate Bias Voltage (Vgg)	-2V to 0V
Control Bias Voltage (Vctl)	(Vdd -7) to Vdd (V)
RF Input Power (RFIN)(Vdd = +7 Vdc)	+23 dBm
Channel Temperature	175 °C
Continuous Pdiss (T = 85 °C) (derate 24 mW/°C above 85 °C)	1.5 W
Thermal Resistance (channel to ground paddle)	59.4 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

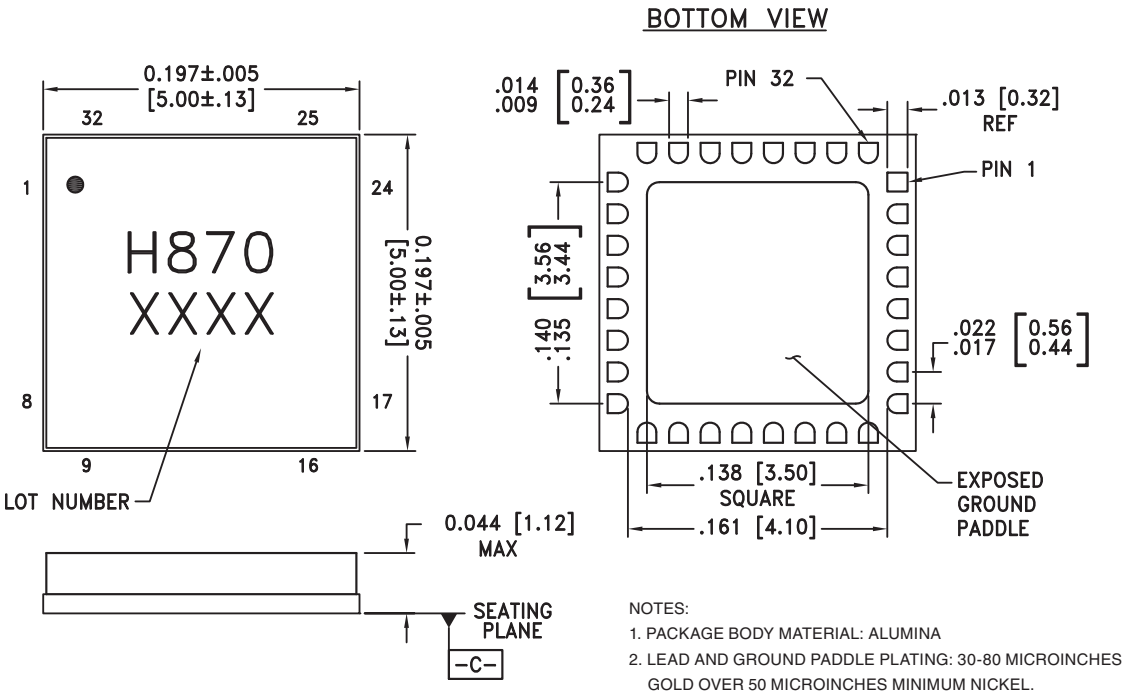
Typical Supply Current vs. Vdd*

Vdd (V)	Idd (mA)*	Power Dissipation (W)
+3.3	100	0.33
+5.0	140	0.70
+6.0	160	0.96
+7.0	165	1.115

* Adjust Vgg between -2V to 0V to achieve Idd shown.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

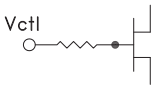
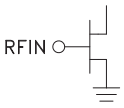
Outline Drawing



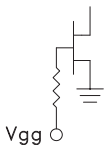
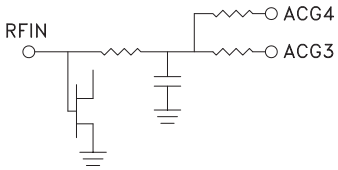
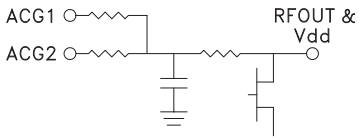
NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

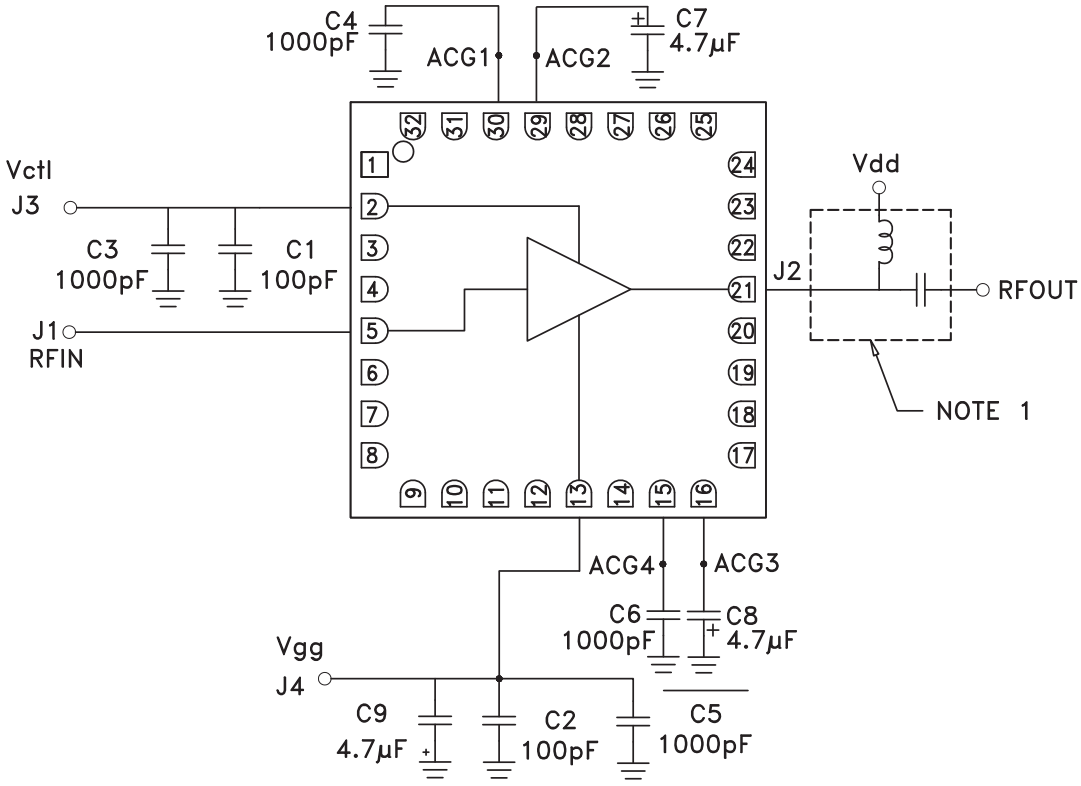
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 3, 4, 7 - 12, 14, 17 - 19, 22 - 28, 31, 32	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
2	Vctl	Output voltage swing adjustment. +1V should be applied to Vctl for nominal operation.	
5	RFIN	This pin is DC coupled and matched to 50 Ohms.	
6, 20	GND	RF/DC Ground. These pins and the package base must be connected to RF/DC ground.	

Pin Descriptions *(Continued)*

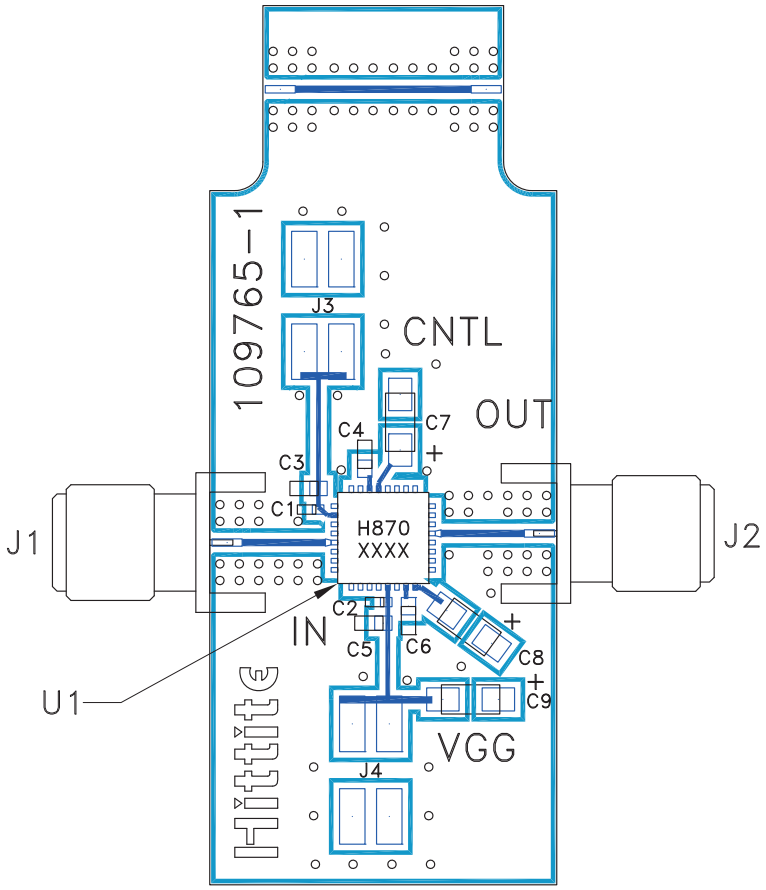
Pin Number	Function	Description	Interface Schematic
13	Vgg	Gate Control for amplifier.	
15	ACG4	Low frequency termination. Attach bypass capacitor per application circuit herein.	
16	ACG3		
21	RFOUT & Vdd	RF output for amplifier. Connect the DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.	
29	ACG2	Low frequency termination. Attach bypass capacitor per application circuit herein.	
30	ACG1		

Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.

Evaluation PCB



List of Materials for Evaluation PCB 108347 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3 - J4	2mm Molex Header
C1, C2	100 pF Capacitor, 0402 Pkg.
C3 - C6	1000 pF Capacitor, 0603 Pkg.
C7 - C9	4.7 µF Capacitor, Tantalum
U1	HMC870LC5, Modulator Driver
PCB [2]	109765 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.

Device Operation

These devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

The input to this device should be AC-coupled. To provide the typical 8Vp-p output voltage swing, a 1.2Vp-p AC-coupled input voltage swing is required.

Device Power Up Instructions

1. Ground the device
2. Set Vgg to -2V (no drain current)
3. Set Vctl to +1V (no drain current)
4. Set Vdd to +5V (no drain current)
5. Adjust Vgg for Idd = 140mA

- Vgg may be varied between -1V and 0V to provide the desired eye crossing point percentage (i.e. 50% crosspoint) and a limited cross point control capability.
- Vdd may be increased to +7V if required to achieve greater output voltage swing.
- Vctl may be adjusted between +2V and +0V to vary the output voltage swing.

Device Power Down Instructions

1. Reverse the sequence identified above in steps 1 through 4.