# MAADCC0006



Digital Attenuator 15.0 dB, 4-Bit, TTL Driver, DC-4.0 GHz

Rev. V5

#### **Features**

- Attenuation: 1 dB Steps to 15 dB
- Low DC Power Consumption
- Small Footprint, JEDEC Package
- Integral TTL Driver
- 50 Ohm Impedance
- Test Boards Available
- Tape and Reel Packaging Available
- Lead-Free CSP-1 Package
- 100% Matte Tin Plating over Copper
- Halogen-Free "Green" Mold Compound
- 260°C Reflow Compatible
- RoHS\* Compliant Version of AT90-0413

#### **Description**

M/A-COM's MAADCC0006 is a GaAs FET 4-Bit digital attenuator with integral driver. Step size is 1 dB providing a 15 dB attenuation range. This device is in an PQFN plastic surface mount package. The MAADCC0006 is suited for applications where accuracy, fast speed, low power consumption and low costs are required.

### **Ordering Information**

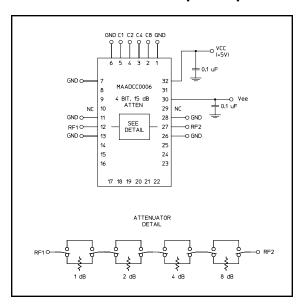
Part Number	Package			
MAADCC0006	Bulk Packaging			
MAADCC0006TR	1000 piece reel			
MAADCC0006-TB	Sample Test Board			

Note: Reference Application Note M513 for reel size information.

typical. Mechanical outline has been fixed. Engineering samples

Commitment to produce in volume is not g

### **Schematic with Off-Chip Components**



# Pin Configuration<sup>2</sup>

Pin No.	Function	Pin No.	Function
1	GND	17	N/C
2	C8	18	N/C
3	C4	19	N/C
4	C2	20	N/C
5	C1	21	N/C
6	GND	22	N/C
7	GND	23	N/C
8	N/C	24	N/C
9	N/C	25	N/C
10	N/C <sup>1</sup>	26	GND
11	GND	27	RF2
12	RF1	28	GND
13	GND	29	N/C <sup>1</sup>
14	N/C	30	Vee
15	N/C	31	N/C
16	N/C	32	+Vcc

- 1. Pins 10 & 29 must be isolated.
- The exposed pad centered on the package bottom must be connected to RF and DC ground. (For PQFN Packages)

<sup>\*</sup> Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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# Electrical Specifications: $T_A = 25$ °C

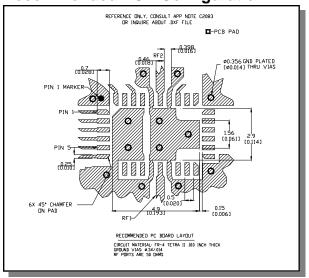
Parameter	Test Conditions	Frequency	Units	Min	Тур	Max
Insertion Loss	_	DC-2.5 GHz DC-4.0 GHz	dB dB	_	2.0 2.5	2.5 3.0
Attenuation Accuracy	Individual Bits or Combination of Bits	DC-2.5 GHz DC-4.0 GHz	dB dB	_	_	±(0.3+4% of atten setting) ±(0.3+6% of atten setting)
VSWR	Full Attenuation Range	DC-2.5 GHz DC-4.0 GHz	Ratio Ratio	_	1.5:1 1.8:1	1.8:1 2.0:1
Switching Speed	50% Cntl to 90%/10% RF 10% to 90% or 90% to 10%	=	ns ns	_	25 4	_
1 dB Compression	_	50 MHz 0.5-4.0 GHz	dB dB	_	+21 +27	_
Input IP <sub>3</sub>	Two-tone Inputs up to +5 dBm	50 MHz 0.5-4.0 GHz	dB dB	_	+35 +48	_
+Vcc	_	_	V	4.75	5.0	5.25
-Vee	_	_	V	-8.0	-5.0	-4.75
V <sub>IL</sub> V <sub>IH</sub>	LOW-level input voltage HIGH-level input voltage	=	V	0.0 2.0	_	0.8 5.0
lin (Input Leakage Current)	Vin = V <sub>CC</sub> or GND	_	uA	-1.0	_	1.0
Icc (Quiescent Supply Current)	Vcntrl = V <sub>CC</sub> or GND	_	uA	_	250	400
∆lcc (Additional Supply Current Per TTL Input Pin)	V <sub>CC</sub> = Max, Vcntrl = V <sub>CC</sub> - 2.1 V	_	mA	_	_	1.5
lee	VEE min to max, Vin = $V_{IL}$ or $V_{IH}$	_	mA	-1.0	-0.2	_
Thermal Resistance θjc	_	_	°C/W	_	15	_

# **Absolute Maximum Ratings** <sup>3,4</sup>

Parameter	Absolute Maximum
Max. Input Power 0.05 GHz 0.5 - 4.0 GHz	+27 dBm +34 dBm
V <sub>CC</sub>	-0.5V ≤ V <sub>CC</sub> ≤ +7.0V
V <sub>EE</sub>	-8.5V ≤ V <sub>EE</sub> ≤ +0.5V
V <sub>CC</sub> - V <sub>EE</sub>	-0.5V ≤ V <sub>CC</sub> - V <sub>EE</sub> ≤ 14.5V
Vin <sup>5</sup>	-0.5V ≤ Vin ≤ V <sub>CC</sub> + 0.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +125°C

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- 5. Standard CMOS TTL interface, latch-up will occur if logic signal applied prior to power supply.

# Recommended PCB Configuration<sup>6</sup>



- 6. Application Note S2083 is available on line at www.macom.com
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## **Handling Procedures**

Please observe the following precautions to avoid damage:

# **Static Sensitivity**

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

### **Moisture Sensitivity**

The MSL rating for this part is defined as Level 2 per IPC/JEDEC J-STD-020. Parts shall be stored and/or baked as required for MSL Level 2 parts.

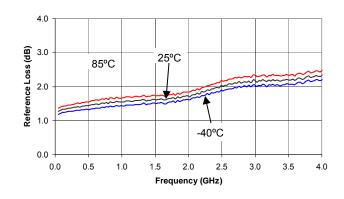
## **Truth Table (Digital Attenuator)**

C8	C4	C2	C1	Attenuation
0	0	0	0	Loss, Reference
0	0	0	1	1.0 dB
0	0	1	0	2.0 dB
0	1	0	0	4.0 dB
1	0	0	0	8.0 dB
1	1	1	1	15.0 dB

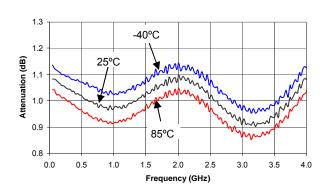
0 = TTL Low. 1 = TTL High

#### Typical Performance Curves

#### Reference Loss vs. Frequency

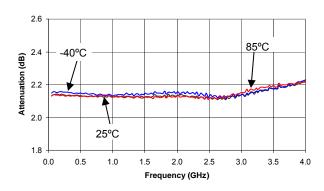


#### Attenuation - 1 dB Bit vs. Frequency

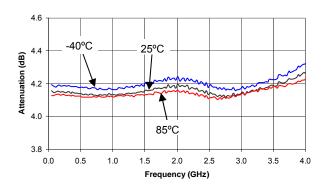


#### Attenuation - 2 dB Bit vs. Frequency

typical. Mechanical outline has been fixed. Engineering samples Commitment to produce in volume is not guaranteed.



#### Attenuation - 4dB Bit vs. Frequency



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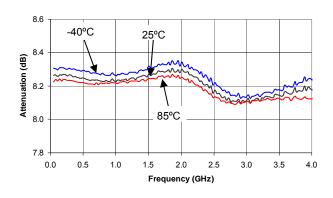


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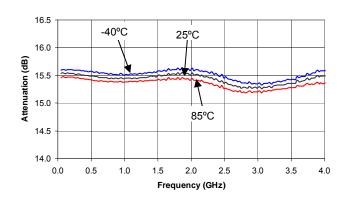
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# **Typical Performance Curves**

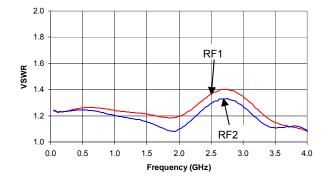
#### Attenuation - 8 dB Bit vs. Frequency



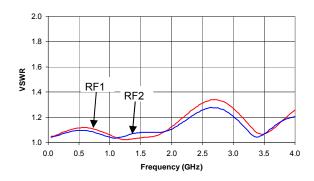
#### Attenuation - 15 dB Attenuation vs. Frequency



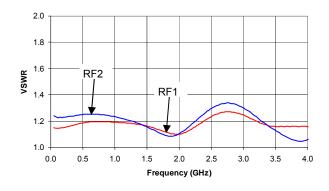
VSWR vs. Frequency Reference Loss State



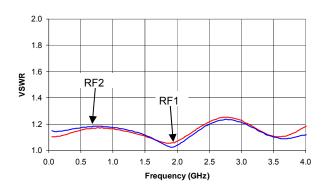
VSWR - 1 dB Bit vs. Frequency



VSWR - 2 dB Bit vs. Frequency



VSWR - 4 dB Bit vs. Frequency



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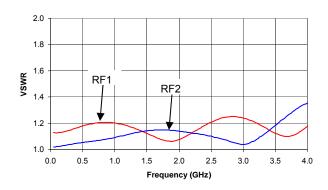


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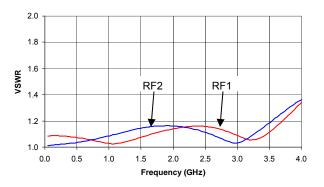
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#### **Typical Performance Curves**

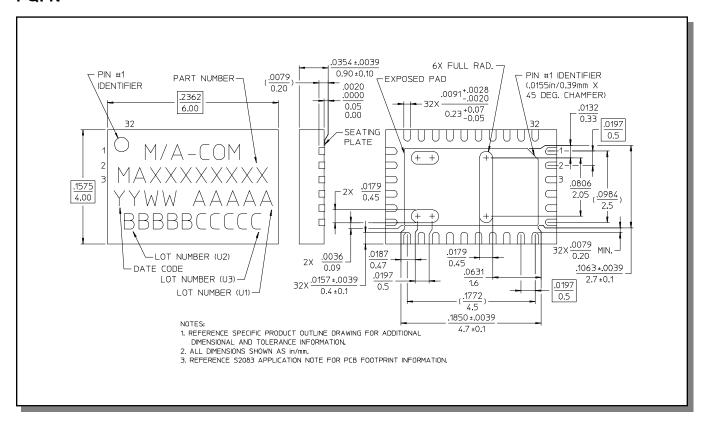
#### VSWR - 8 dB Bit vs. Frequency



#### VSWR - 15 dB Attenuation vs. Frequency



# CSP-1, Lead-Free 4 x 6 mm, 32-lead PQFN<sup>†</sup>



<sup>&</sup>lt;sup>†</sup> Reference Application Note M538 for lead-free solder reflow recommendations.

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