XP1042-QT

Power Amplifier
12.0-16.0 GHz

Rev. V1
Mimix Broadband

Features

- 21 dB Small Signal Gain
- 25 dBm P1dB Compression Point
- 38 dBm Output IP3 Linearity
- 17 dB Gain Control with Bias Adjust
- 3x3mm Standard QFN Package
- 100% RF Testing
- RoHS* Compliant and 260°C Reflow Compatible

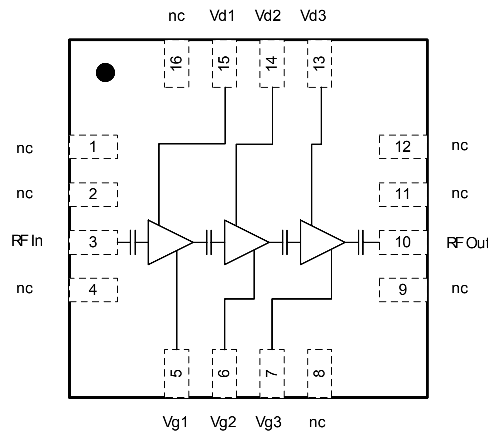
Description

The XP1042-QT is a packaged driver amplifier that operates over the 12.0-16.0 GHz frequency band. The device provides 21 dB gain and 38 dBm Output Third Order Intercept Point (OIP3) across the band and is offered in an industry standard, fully molded 3x3mm QFN package. The device includes on-chip ESD protection structures and DC by-pass capacitors to ease the implementation and volume assembly of the packaged part. The device is manufactured in 0.5um GaAs PHEMT device technology with BCB wafer coating to enhance ruggedness and repeatability of performance. The XP1042-QT is well suited for Point-to-Point Radio, LMDS, SATCOM and VSAT applications.

Ordering Information

Part Number	Package
XP1042-QT-0G00	bulk quantity
XP1042-QT-0G0T	tape and reel
XP1042-QT-EV1	evaluation module

Functional Block Diagram/Board Layout



Pin Configuration

Pin No.	Function	Pin No.	Function
1-2	Not Connected	10	RF Output
3	RF Input	11-12	Not Connected
4	Not Connected	13	Drain 3 Bias
5	Gate 1 Bias	14	Drain 2 Bias
6	Gate 2 Bias	15	Drain 1 Bias
7	Gate 3 Bias	16	Not Connected
8-9	Not Connected		

Absolute Maximum Ratings[1]

Parameter	Absolute Max.
Supply Voltage (Vd1,2,3)	+8.0 V
Supply Current (Id1,2,3)	550 mA
Gate Bias Voltage (Vg1,2,3)	-2.4 V
Max Power Dissipation (Pdiss)	2.8W
RF Input Power	15 dBm
Operating Temperature (Ta)	-55 ºC to +85 ºC
Storage Temperature (Tstg)	-65 ºC to +165 ºC
Channel Temperature (Tch)[2]	150 ºC
ESD Min. - Machine Model (MM)	Class A
ESD Min. - Human Body Model (HBM)	Class 1A
MSL Level	MSL3

(1) Operation of this device above any one of these parameters may cause permanent damage.
(2) Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

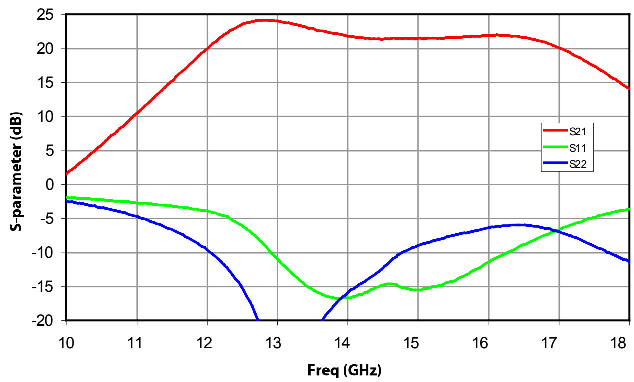
• **North America** Tel: 800.366.2266 • **Europe** Tel: +353.21.244.6400
• **India** Tel: +91.80.43537383 • **China** Tel: +86.21.2407.1588
Visit www.macomtech.com for additional data sheets and product information.

Electrical Specifications: 12-16 GHz (Ambient Temperature T = 25°C)

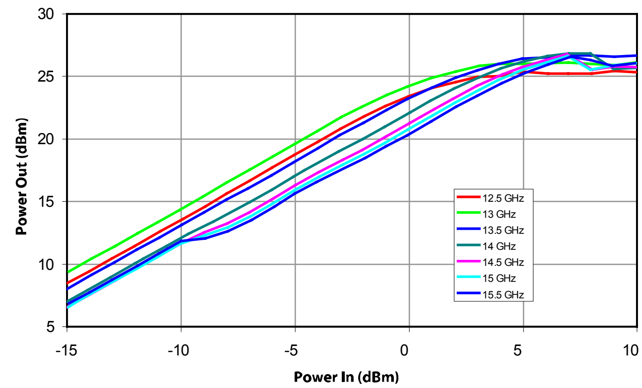
Parameter	Units	Min.	Typ.	Max.
Small Signal Gain (S21)	dB	19.0	21.0	
Input Return Loss (S11)	dB		12.0	
Output Return Loss (S22)	dB		10.0	
Reverse Isolation (S12)	dB		50.0	
NF at Max Gain	dB		6.0	8.0
P1dB	dB		25.0	
OIP3 at Pout = 8 dBm per Tone	dBm	36.0	38.0	
Drain Bias Voltage (Vd1,2,3)	VDC		5	
Gate Bias Voltage (Vg1,2,3)	VDC	-2	-1	
Supply Current (Id1)	mA		75	125
Supply Current (Id2)	mA		75	125
Supply Current (Id3)	mA		150	250

Typical Performance Curves

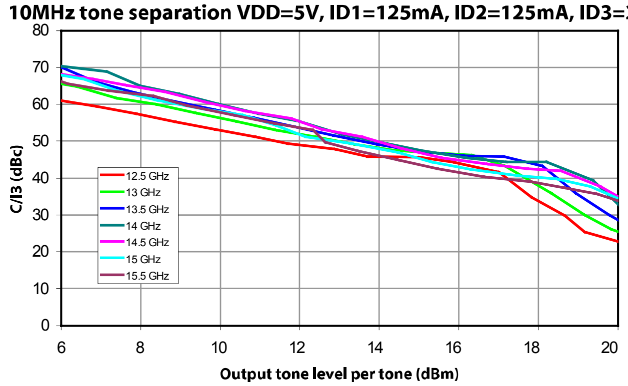
XP1042-QT: S-parameters (dB) vs. Freq (GHz), VDD=5V, ID1=125mA, ID2=125mA, ID3=250mA



XP1042-QT: Power Out (dBm) vs. Power In (dBm), VDD=5V, ID1=125mA, ID2=125mA, ID3=250mA

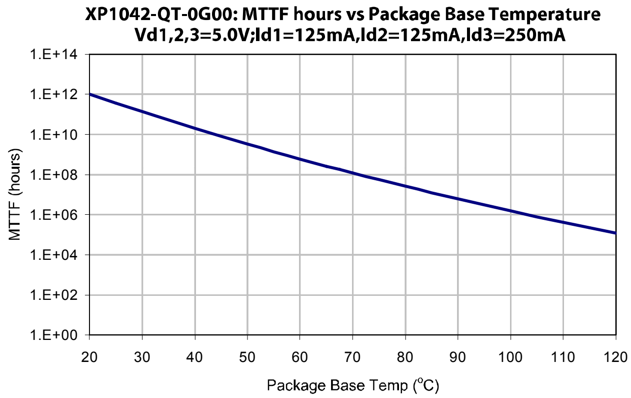


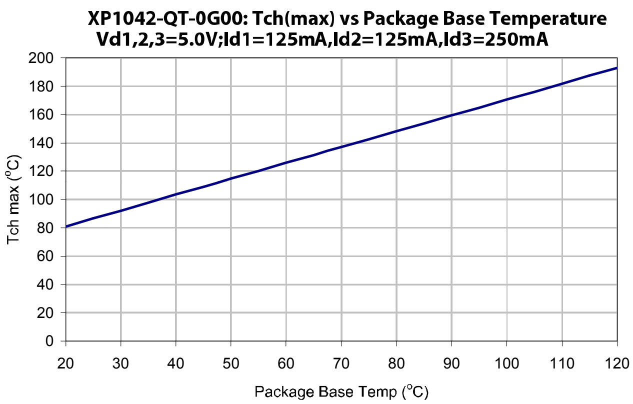
XP1042-QT: C/I3 (dBc) vs. Output Tone Power (per tone) dBm 10MHz tone separation VDD=5V, ID1=125mA, ID2=125mA, ID3=250mA

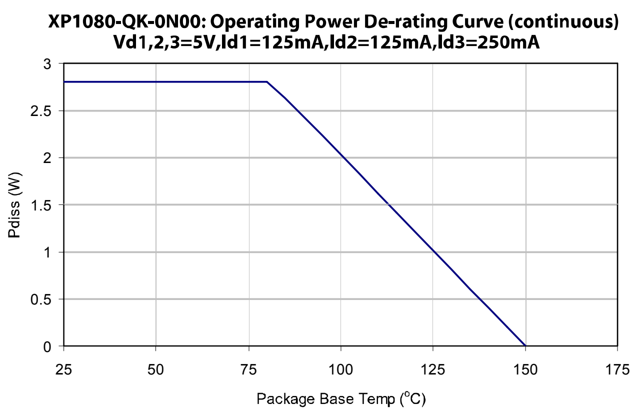


MTTF

These numbers were calculated based on accelerated life test information and thermal model analysis received from the fabricating foundry.



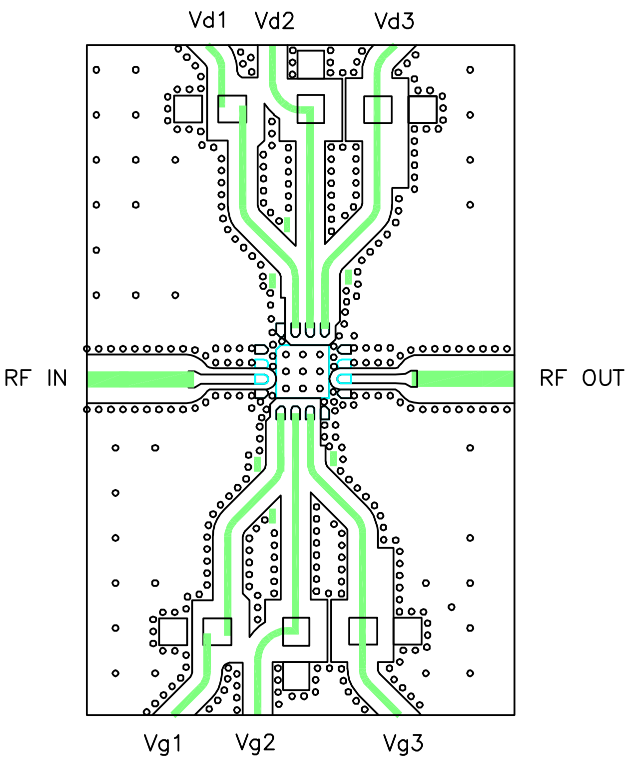




App Note [1] Biasing - As shown in the Pin Designations table, the device is operated by biasing VD1,2,3 at 5.0V with 125, 125, 250 mA respectively. It is recommended to use active bias to keep the currents constant in order to maintain the best performance over temperature. Depending on the supply voltage available and the power dissipation constraints, the bias circuit may be a single transistor or a low power operational amplifier, with a low value resistor in series with the drain supply used to sense the current. The gate of the pHEMT is controlled to maintain correct drain current and thus drain voltage. The typical gate voltage needed to do this is -1.0V. Make sure to sequence the applied voltage to ensure negative gate bias is available before applying the positive drain supply.

App Note [2] Board Layout - As shown in the board layout, it is recommended to provide 100pF decoupling caps as close to the bias pins as possible, with additional 10μF decoupling caps.

Recommended Layout

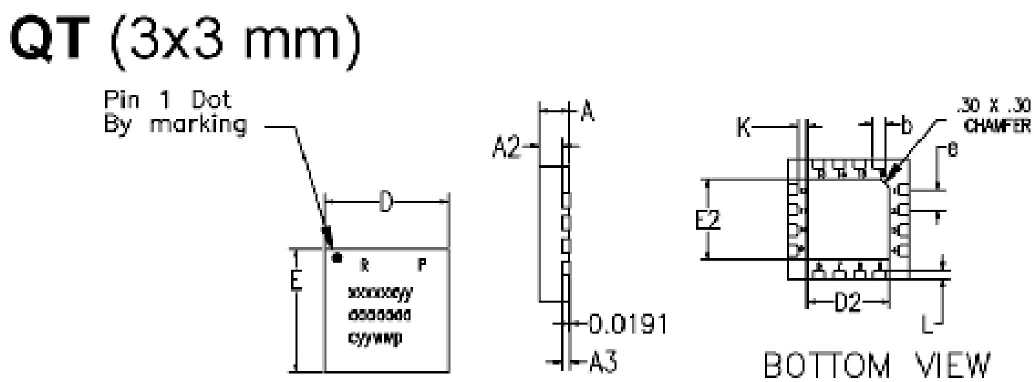


Recommended Caps:

(6x) 100pF, 0402

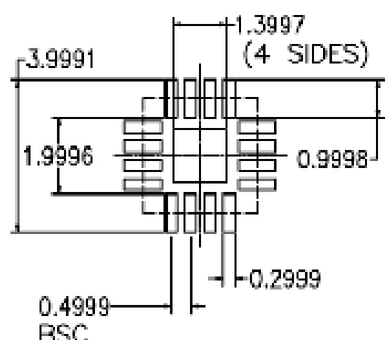
(6x) 10nF, 0805

Lead-Free Package Dimensions/Layout



Note:
1. ALL DIMENSIONS ARE IN mm.

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



	MIN	TYP	MAX
A	0.80	0.90	1.00
A3	0.20 REF		
A2	0.00	0.65	1.00
b	0.20	0.25	0.30
K	0.20	–	–
D	3.00 BSC		
E	3.00 BSC		
e	0.50		
D2	1.50	1.65	1.80
E2	1.50	1.65	1.80
L	0.16	0.26	0.36

1. VIEWS ARE NOT TO SCALE: USE DIMENSIONS AND TABLE.

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these class 2 devices.