

PM50B4LA060FLAT-BASE TYPE
INSULATED PACKAGE**PM50B4LA060****FEATURE**

- a) Adopting new 5th generation IGBT (CSTBT™) chip, which performance is improved by 1μm fine rule process.
For example, typical $V_{ce(sat)}=1.55V @T_j=125^{\circ}C$
- b) Over-temperature protection by detecting T_j of the CSTBT™ chips and error output is possible from all each conservation upper and lower arm of IPM.
- c) New small package
Reduce the package size by 10%, thickness by 22% from S-DASH series.
 - 2φ 50A, 600V Current-sense IGBT type inverter
 - Monolithic gate drive & protection logic
 - Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage (P-Fo available from upper arm devices)
 - UL Recognized Yellow Card No.E80276(N)
File No.E80271

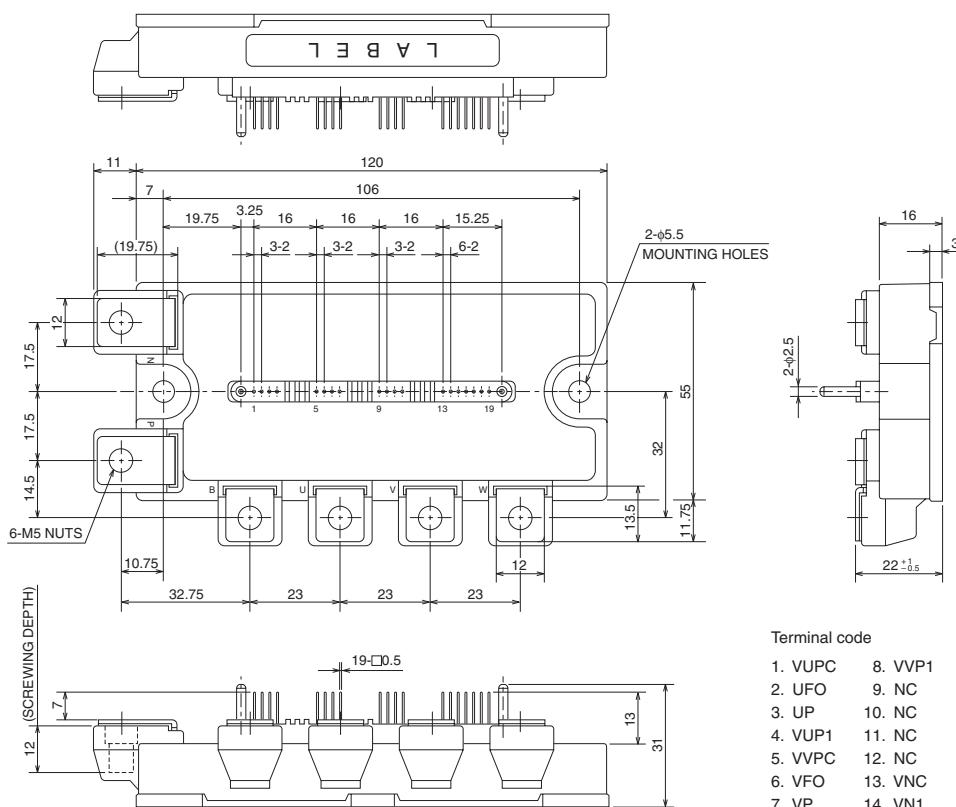
APPLICATION

Photo voltaic power conditioner

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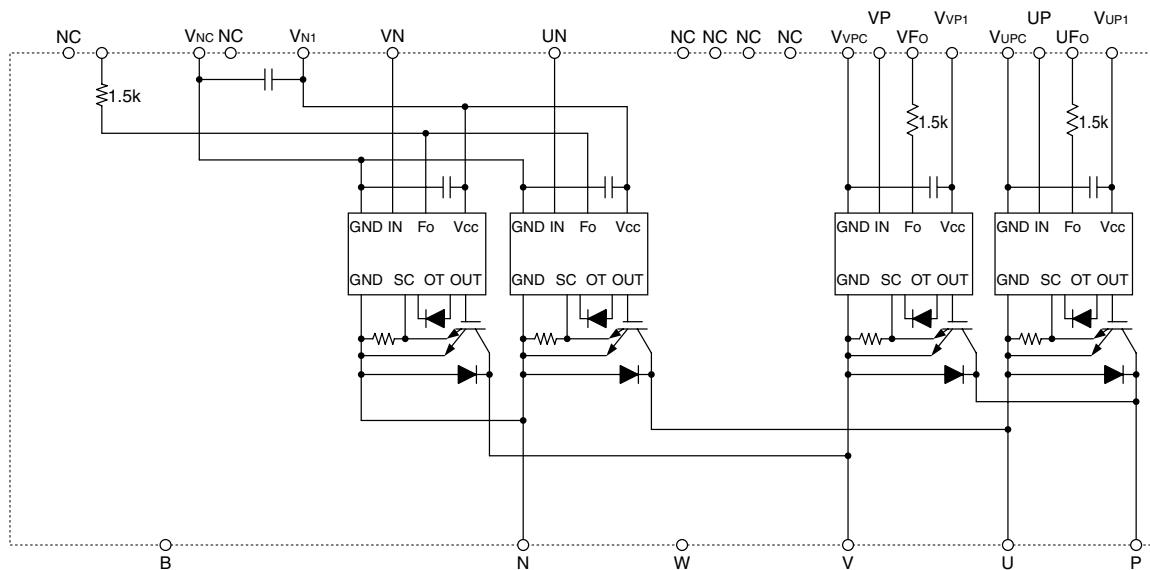
PACKAGE OUTLINES

Dimensions in mm



Oct. 2005

INTERNAL FUNCTIONS BLOCK DIAGRAM



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MAXIMUM RATINGS ($T_j = 25^\circ\text{C}$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
V _{CES}	Collector-Emitter Voltage	$V_D = 15\text{V}$, $V_{CIN} = 15\text{V}$	600	V
$\pm I_C$	Collector Current	$T_c = 25^\circ\text{C}$	50	A
$\pm I_{CP}$	Collector Current (Peak)	$T_c = 25^\circ\text{C}$	100	A
P _c	Collector Dissipation	$T_c = 25^\circ\text{C}$	131	W
T _j	Junction Temperature		-20 ~ +150	°C

CONTROL PART

Symbol	Parameter	Condition	Ratings	Unit
V _D	Supply Voltage	Applied between : V _{UP1} -V _{UPC} V _{VP1} -V _{VPC} , V _{N1} -V _{NC}	20	V
V _{CIN}	Input Voltage	Applied between : U _P -V _{UPC} , V _P -V _{VPC} U _N • V _N -V _{NC}	20	V
V _{FO}	Fault Output Supply Voltage	Applied between : U _{FO} -V _{UPC} , V _{FO} -V _{VPC} , F _O -V _{NC}	20	V
I _{FO}	Fault Output Current	Sink current at U _{FO} , V _{FO} , F _O terminals	20	mA

PM50B4LA060FLAT-BASE TYPE
INSULATED PACKAGE**TOTAL SYSTEM**

Symbol	Parameter	Condition	Ratings	Unit
VCC(prot)	Supply Voltage Protected by SC	VD = 13.5 ~ 16.5V, Inverter Part, T _j = +125°C Start	450	V
VCC(surge)	Supply Voltage (Surge)	Applied between : P-N, Surge value	500	V
T _{stg}	Storage Temperature		-40 ~ +125	°C
V _{iso}	Isolation Voltage	60Hz, Sinusoidal, Charged part to Base, AC 1 min.	2500	V _{rms}

THERMAL RESISTANCES

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
R _{th(j-c)Q}	Junction to case Thermal Resistances	Inverter IGBT part (per 1/4 module)	(Note-1)	—	—	0.95
		Inverter FWDi part (per 1/4 module)		—	—	1.61
R _{th(c-f)}	Contact Thermal Resistance	Case to fin, (per 1 module) Thermal grease applied	(Note-1)	—	—	0.038

(Note-1) T_c (under the chip) measurement point is below.

(unit : mm)

axis	arm	UP		VP		UN		VN	
		IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi
X		31.1	30.6	61.0	60.5	38.2	40.7	52.9	50.4
Y		-10.0	-2.2	-10.0	-2.2	8.0	0.2	8.0	0.2



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ELECTRICAL CHARACTERISTICS (T_j = 25°C, unless otherwise noted)**INVERTER PART**

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
V _{CE(sat)}	Collector-Emitter Saturation Voltage	VD = 15V, IC = 50A	T _j = 25°C	—	1.7	2.3
		VCIN = 0V		—	1.55	2.0
V _{EC}	FWDi Forward Voltage	—IC = 50A, VD = 15V, VCIN = 15V	(Fig. 2)	—	2.2	3.3
ton	Switching Time	VD = 15V, VCIN = 0V↔15V VCC = 300V, IC = 50A T _j = 125°C Inductive Load	(Fig. 3,4)	0.3	0.7	1.4
trr				—	0.1	0.2
tc(on)				—	0.2	0.4
toff				—	0.9	1.8
tc(off)				—	0.2	0.2
IC _{ES}	Collector-Emitter Cutoff Current	VCE = VC _{ES} , VCIN = 15V	T _j = 25°C	—	—	1
			T _j = 125°C	—	—	10

CONTROL PART

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
Id	Circuit Current	VD = 15V, VCIN = 15V	VN1-VNC	—	10	20	mA
			V*P1-V*PC	—	5	10	
Vth(ON)	Input ON Threshold Voltage	Applied between : UP-VUPC, VP-VVPC UN • VN-VNC		1.2	1.5	1.8	V
				1.7	2.0	2.3	
SC	Short Circuit Trip Level	—20 ≤ Tj ≤ 125°C, VD = 15V	(Fig. 3,6)	100	—	—	A
toff(SC)	Short Circuit Current Delay Time	VD = 15V	(Fig. 3,6)	—	0.2	—	μs
OT	Over Temperature Protection	VD = 15V Detect Tj of IGBT chip	Trip level	135	145	—	°C
			Reset level	—	125	—	
UV	Supply Circuit Under-Voltage Protection	—20 ≤ Tj ≤ 125°C	Trip level	11.5	12.0	12.5	V
			Reset level	—	12.5	—	
IFO(H)	Fault Output Current	VD = 15V, VFO = 15V	(Note-2)	—	—	0.01	mA
			(Note-2)	—	10	15	
tFO	Minimum Fault Output Pulse Width	VD = 15V	(Note-2)	1.0	1.8	—	ms

(Note-2) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

MECHANICAL RATINGS AND CHARACTERISTICS

Symbol	Parameter	Condition	Limits			Unit	
			Min.	Typ.	Max.		
—	Mounting torque	Main terminal	screw : M5	2.5	3.0	3.5	N • m
—	Mounting torque	Mounting part	screw : M5	2.5	3.0	3.5	N • m
—	Weight	—	—	300	—	—	g

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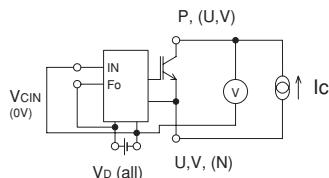
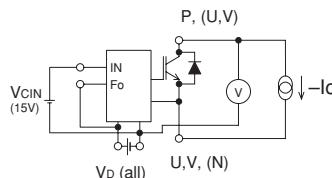
RECOMMENDED CONDITIONS FOR USE

Symbol	Parameter	Condition	Recommended value	Unit
VCC	Supply Voltage	Applied across P-N terminals	≤ 450	V
VD	Control Supply Voltage	Applied between : VUP1-VUPC, VVP1-VVPC VN1-VNC	15 ± 1.5	V
VCIN(ON)	Input ON Voltage	Applied between : UP-VUPC, VP-VVPC UN • VN-VNC	≤ 0.8	V
			≥ 9.0	
fPWM	PWM Input Frequency	Using Application Circuit of Fig. 8	≤ 20	kHz
tdead	Arm Shoot-through Blocking Time	For IPM's each input signals	≥ 2.0	μs

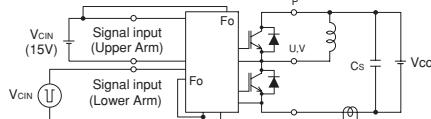
(Note-3) With ripple satisfying the following conditions : dv/dt swing ≤ ±5V/μs, Variation ≤ 2V peak to peak

PRECAUTIONS FOR TESTING

- Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
After this, the specified ON and OFF level setting for each input signal should be done.
- When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)

Fig. 1 $V_{CE(sat)}$ TestFig. 2 V_{EC} Test

a) Lower Arm Switching



b) Upper Arm Switching



Fig. 3 Switching Time and SC Test Circuit

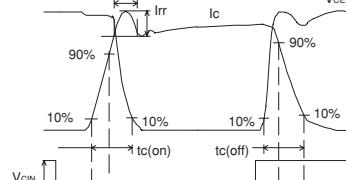


Fig. 4 Switching Time Test Waveform

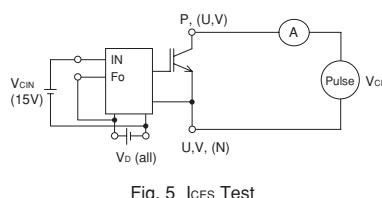


Fig. 5 ICES Test

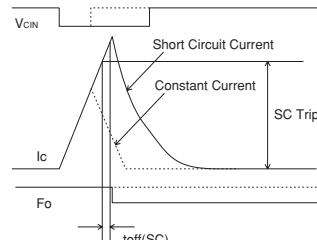


Fig. 6 SC Test Waveform

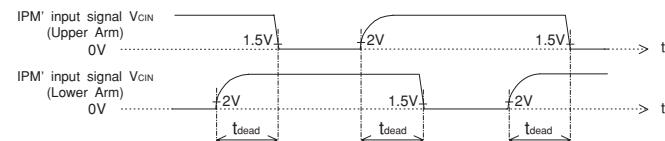
1.5V: Input on threshold voltage $V_{th(on)}$ typical value, 2V: Input off threshold voltage $V_{th(off)}$ typical value

Fig. 7 Dead Time Measurement Point Example

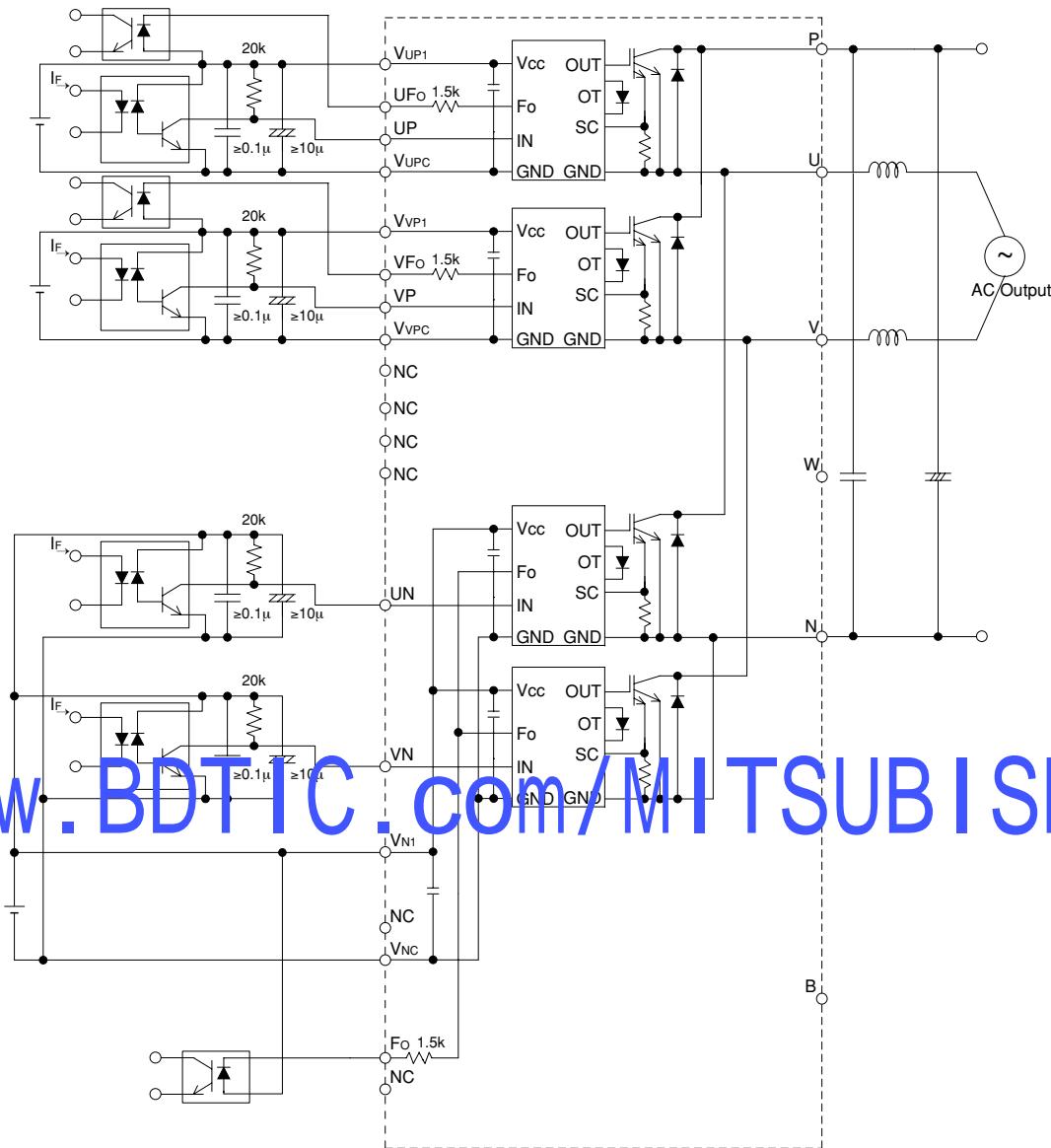
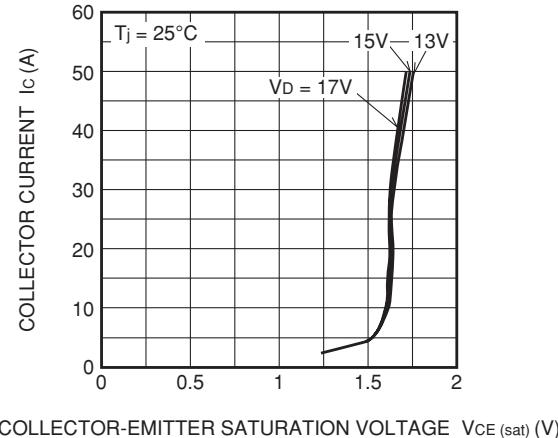
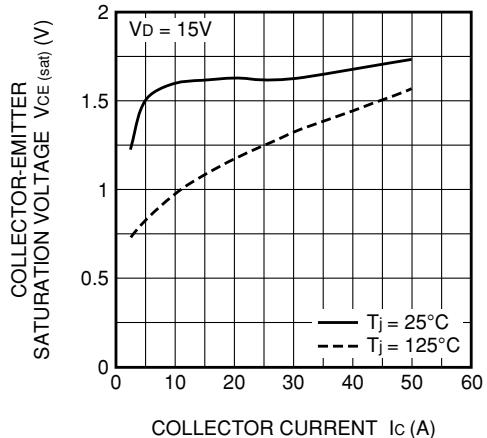
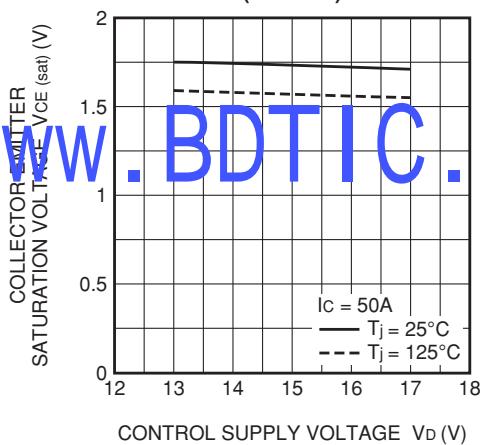
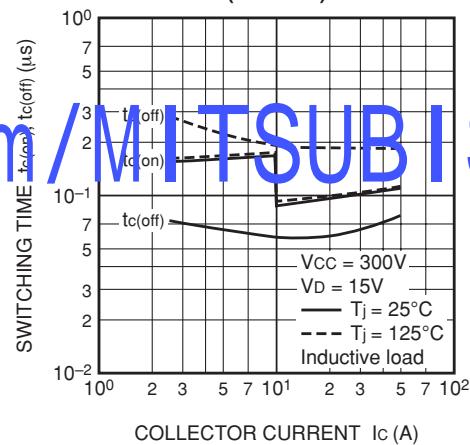
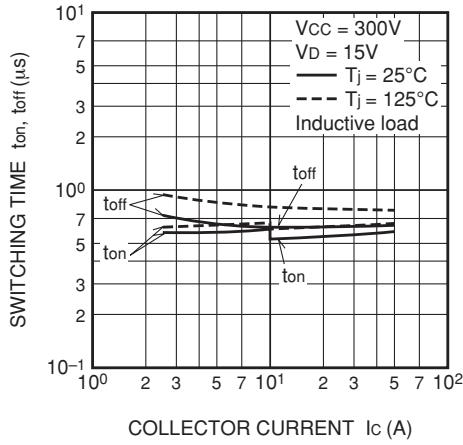
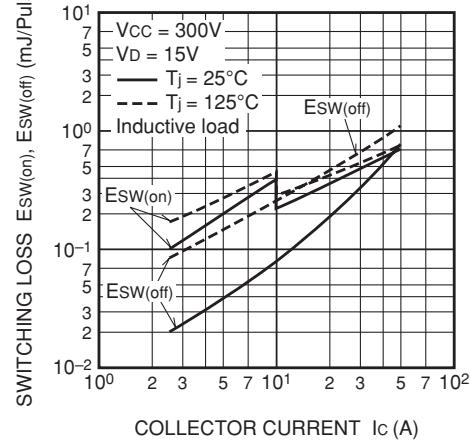
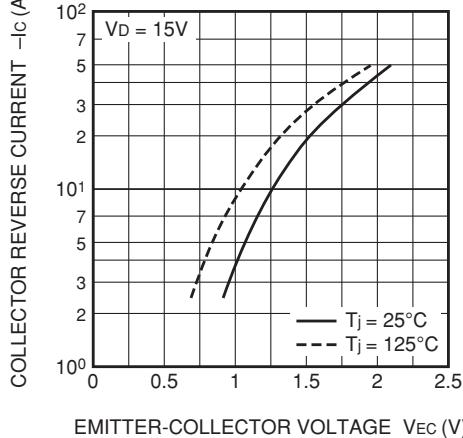
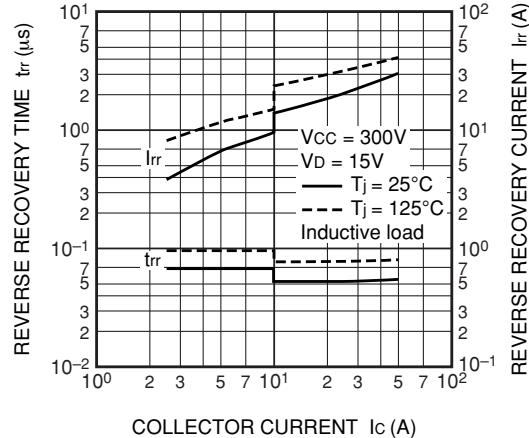
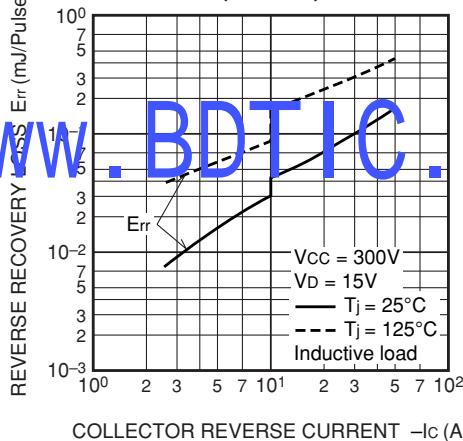


Fig. 8 Application Example Circuit

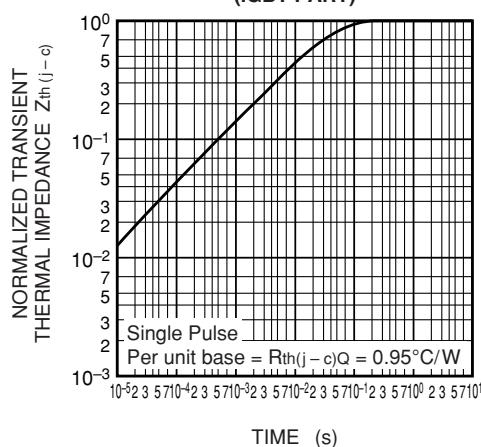
NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: $t_{PLH}, t_{PHL} \leq 0.8\mu s$, Use High CMR type.
- Slow switching opto-coupler: $CTR > 100\%$
- Use 3 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage change of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.

PERFORMANCE CURVES**OUTPUT CHARACTERISTICS
(TYPICAL)****COLLECTOR-EMITTER SATURATION VOLTAGE (VS. Ic) CHARACTERISTICS
(TYPICAL)****COLLECTOR-EMITTER SATURATION VOLTAGE (VS. Vd) CHARACTERISTICS
(TYPICAL)****SWITCHING TIME CHARACTERISTICS
(TYPICAL)****SWITCHING TIME CHARACTERISTICS
(TYPICAL)****SWITCHING LOSS CHARACTERISTICS
(TYPICAL)**

FWD_i FORWARD VOLTAGE CHARACTERISTICS
(TYPICAL)FWD_i REVERSE RECOVERY CHARACTERISTICS
(TYPICAL)FWD_i REVERSE RECOVERY LOSS CHARACTERISTICS
(TYPICAL)

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