EMI4162MU

Common Mode Filter with ESD Protection

Functional Description

The EMI4162MU is an integrated common mode filter providing both ESD protection and EMI filtering for high speed digital serial interfaces such as HDMI or MIPI D-PHY.

The EMI4162MU provides protection for two differential data line pairs in a small RoHS-compliant UDFN10 package.

Features

- Highly Integrated Common Mode Filter (CMF) with ESD Protection provides protection and EMI reduction for systems using High Speed Serial Data Lines with cost and space savings over discrete solutions
- Large Differential Mode Bandwidth with Cutoff Frequency > 2 GHz
- High Common Mode Stop Band Attenuation: >25 dB at 700 MHz, >30 dB at 800 MHz
- Provides ESD Protection to IEC61000-4-2 Level 4, ±15 kV Contact Discharge
- Low Channel Input Capacitance Provides Superior Impedance Matching Performance
- Low Profile Package with Small Footprint in UDFN10 2 x 2.5 mm Pb−Free Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- HDMI/DVI Display in Mobile Phones
- MIPI D-PHY (CSI-2, DSI, etc) in Mobile Phones and Digital Still Cameras

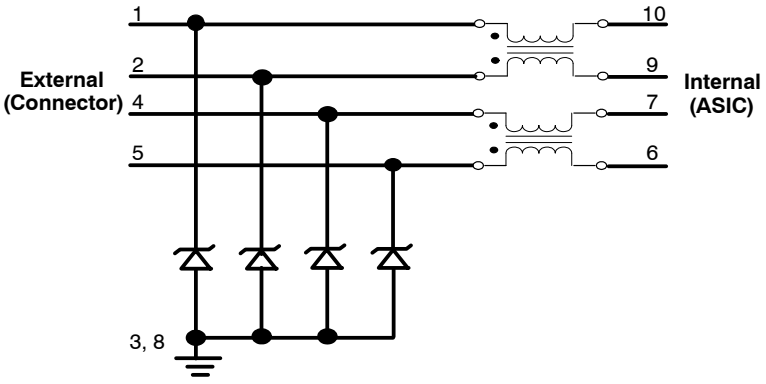

Figure 1. EMI4162MU Electrical Schematic

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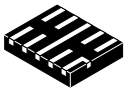
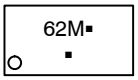
http://onsemi.com

MARKING DIAGRAMS



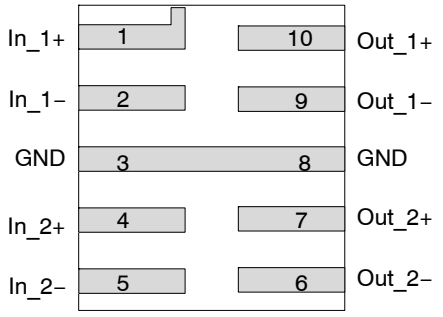
UDFN10
CASE 517CJ



62 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(*Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
EMI4162MUTAG	UDFN10 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Publication Order Number:
EMI4162MU/D

PIN FUNCTION DESCRIPTION

Pin Name	Pin No.	Type	Description
In_1+	1	I/O	CMF Channel 1+ to Connector
In_1−	2	I/O	CMF Channel 1− to Connector
Out_1+	10	I/O	CMF Channel 1+ to ASIC
Out_1−	9	I/O	CMF Channel 1− to ASIC
In_2+	4	I/O	CMF Channel 2+ to Connector
In_2−	5	I/O	CMF Channel 2− to Connector
Out_2+	7	I/O	CMF Channel 2+ to ASIC
Out_2−	6	I/O	CMF Channel 2− to ASIC
V_N	3, 8	GND	Ground

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Operating Temperature Range	T_{OP}	−40 to +85	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C
ESD Discharge IEC61000−4−2 Contact Discharge	V_{PP}	±15	kV
Maximum Lead Temperature for Soldering Purposes (1/8” from Case for 10 seconds)	T_L	260	°C
DC Current per Line	I_{LINE}	100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{LEAK}	Channel Leakage Current	T_A = 25°C, V_{IN} = 5 V, GND = 0 V			1.0	μA
V_F	Channel Negative Voltage	T_A = 25°C, I_F = 10 mA	0.1		1.5	V
C_{IN}	Channel Input Capacitance to Ground (Pins 1, 2, 4, 5 to Pins 3, 8)	T_A = 25°C, At 1 MHz, GND = 0 V, V_{IN} = 1.65 V		0.8	1.3	pF
R_{CH}	Channel Resistance (Pins 1−10, 2−9, 4−7 and 5−6)			8.0		Ω
f_{3dB}	Differential Mode Cut−off Frequency	50 Ω Source and Load Termination		2.0		GHz
F_{atten}	Common Mode Stop Band Attenuation	@ 800 MHz		30		dB
V_{ESD}	ESD Protection − Peak Discharge Voltage at any channel input, in system: Contact discharge per IEC61000−4−2 standard	T_A = 25°C (Notes 1 and 2) Pins 1, 2, 4, 5	±15			kV
V_{CL}	TLP Clamping Voltage (See Figure 12)	Forward I_{PP} = 8 A Forward I_{PP} = 16 A Forward I_{PP} = −8 A Forward I_{PP} = −16 A		12 18 −6 −12		V V V V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	T_A = 25°C, I_{PP} = 1 A, t_P = 8/20 μs Any I/O pin to Ground; Notes 1 and 3		 1.36 0.6		
V_{RWM}	Reverse Working Voltage	(Note 3)			5.0	V
V_{BR}	Breakdown Voltage	I_T = 1 mA; (Note 4)	5.6		9.0	V

1. Standard IEC61000−4−2 with $C_{Discharge}$ = 150 pF, $R_{Discharge}$ = 330, GND grounded.
2. These measurements performed with no external capacitor.
3. TVS devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal to or greater than the DC or continuous peak operating voltage level.
4. V_{BR} is measured at pulse test current I_T.

TYPICAL CHARACTERISTICS

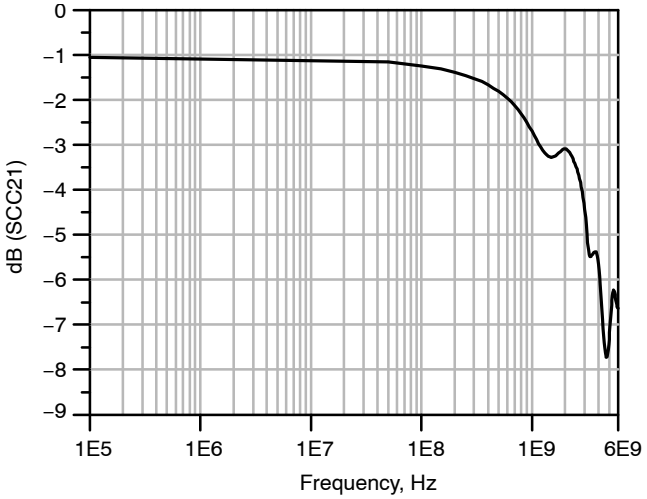


Figure 2. Differential Mode Attenuation vs. Frequency (Zdiff = 100 Ω)

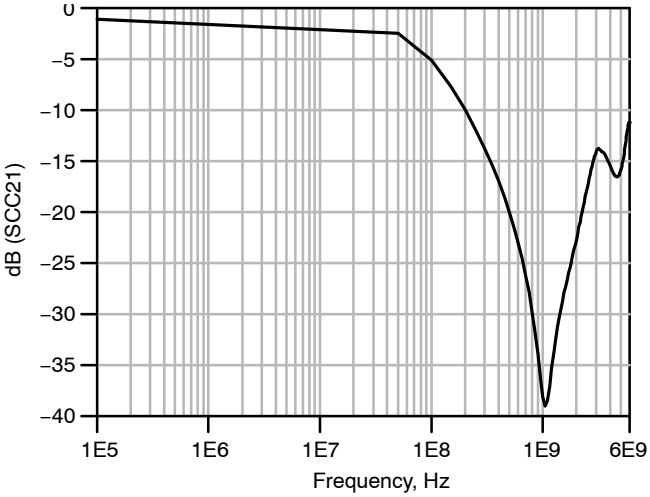


Figure 3. Common Mode Attenuation vs. Frequency (Zcomm = 50 Ω)

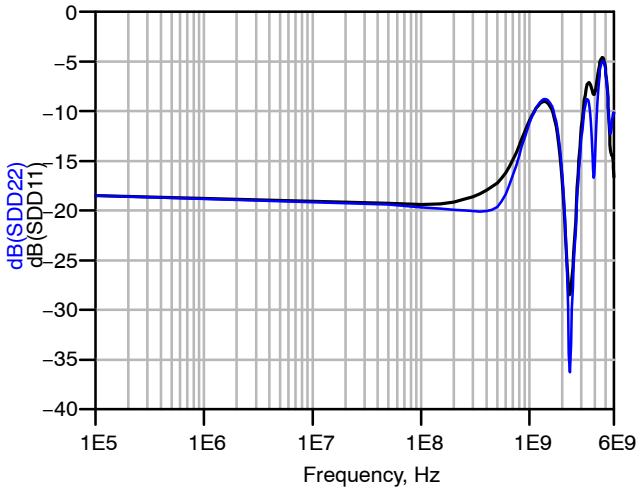


Figure 4. Differential Return Loss vs. Frequency (Zdiff=100 Ω)

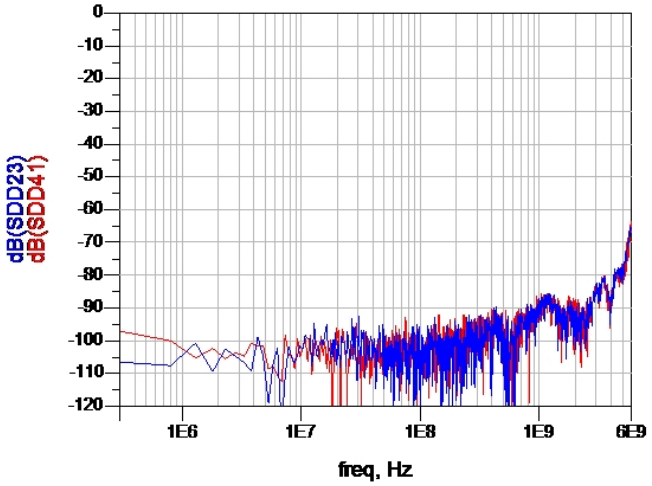


Figure 5. Differential Inter−Lane Cross−Coupling

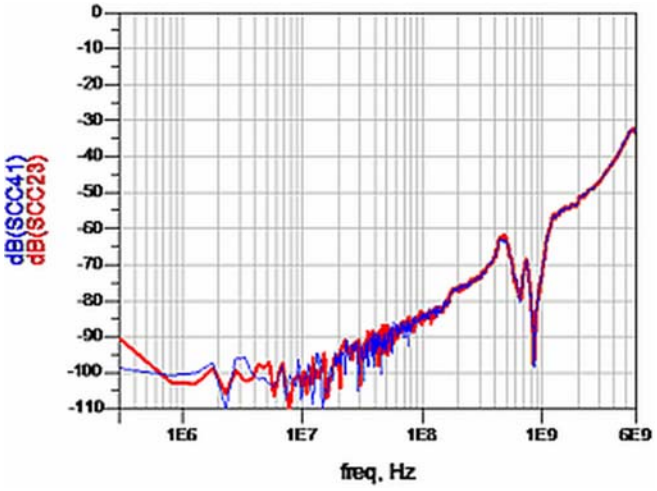


Figure 6. Common Mode Inter−Lane Cross−Coupling

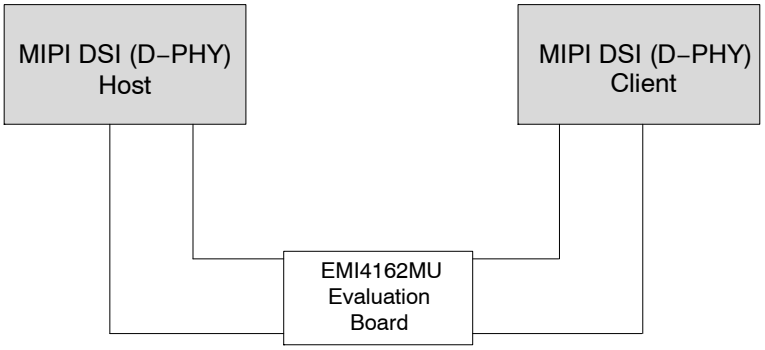


Figure 7. MIPI D−PHY LP Mode Test Setup

Figure 8. EMI4162MU MIPI D−PHY LP Mode Measured Results

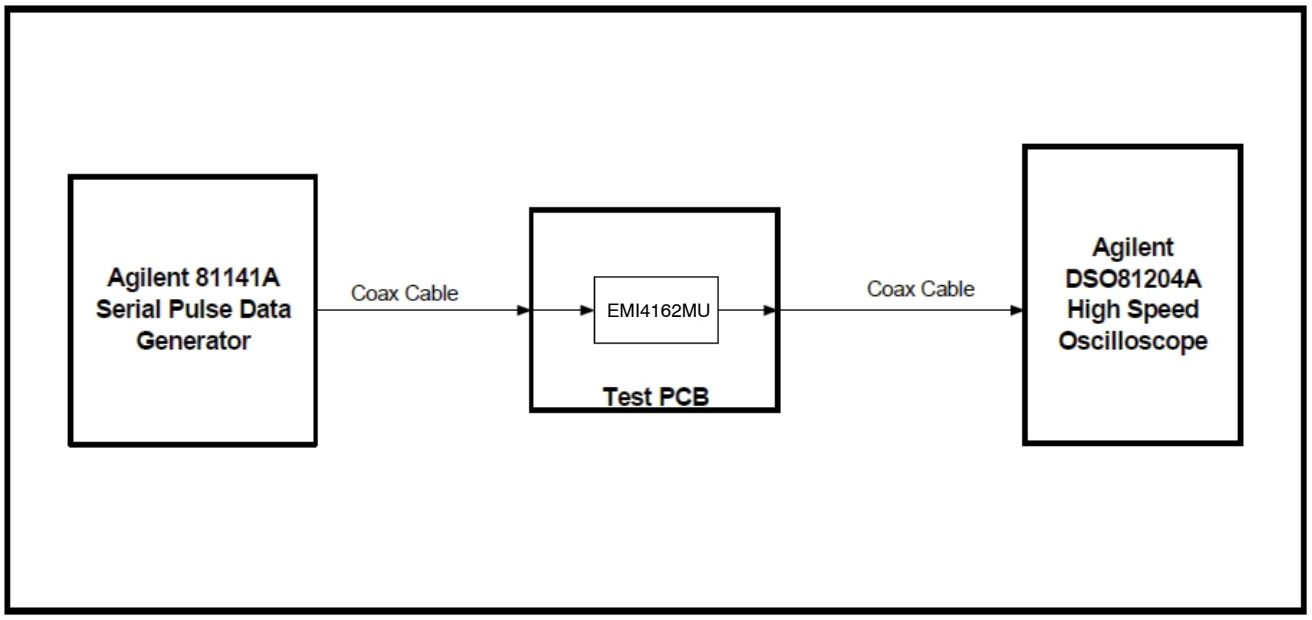


Figure 9. EMI4162MU Eye Diagram Test Setup

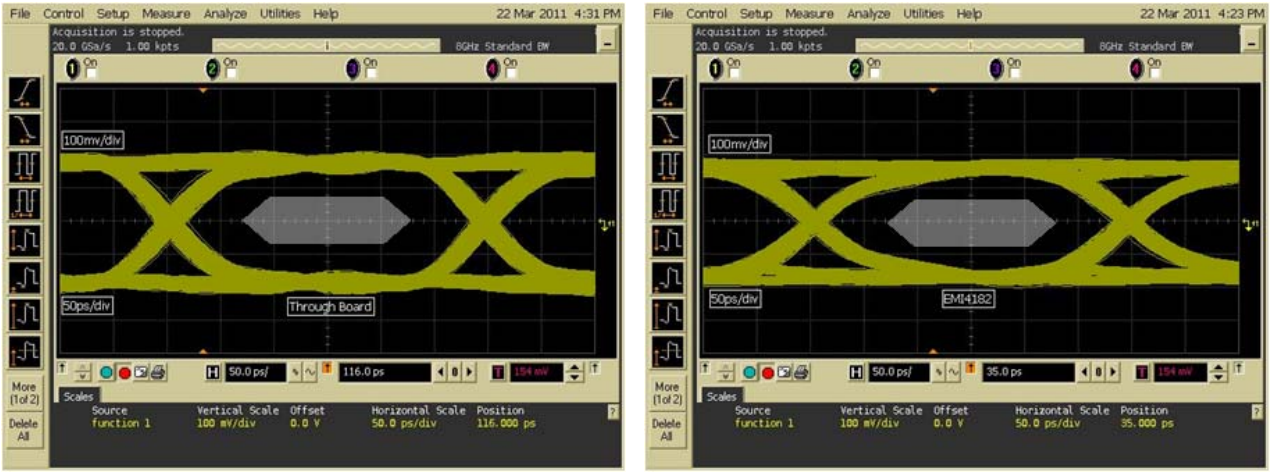


Figure 10. EMI4162MU Measured Eye Diagram @ 3.4Gbps (EVB through on left, EVB with EMI4162 on right)

Transmission Line Pulse (TLP) Measurements

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 11. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10 s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 12 where an 8 kV IEC61000-4-2 current waveform is compared with TLP current pulses at 8 and 16 A. A TLP curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. Typical TLP I-V curves for the EMI4162 are shown in Figure 13.

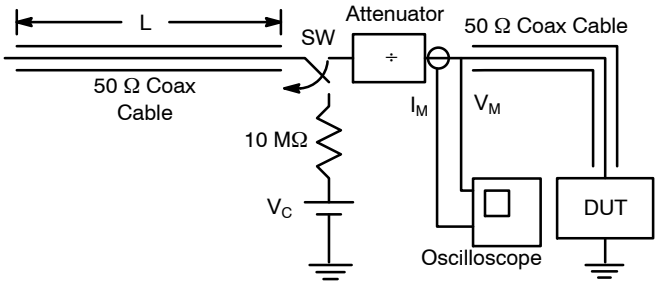


Figure 11. Simplified Schematic of a Typical TLP System

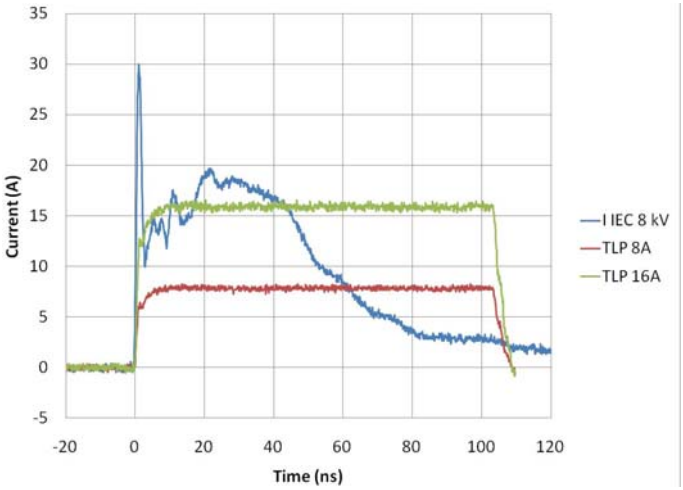


Figure 12. Comparison Between 8 kV IEC61000−4−2 and 8 A and 16 A TLP Waveforms

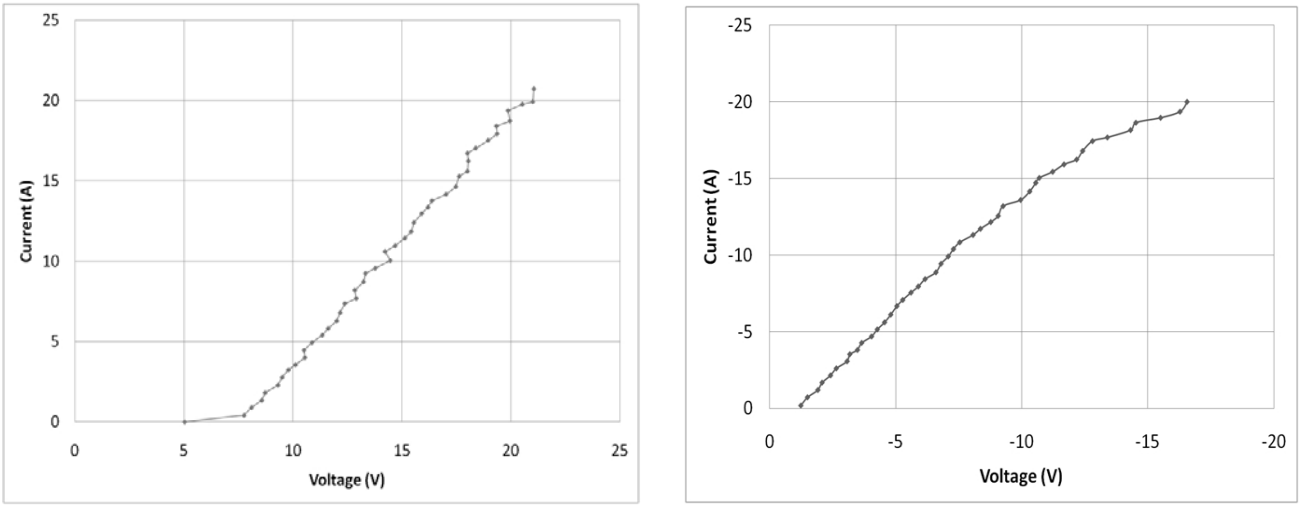


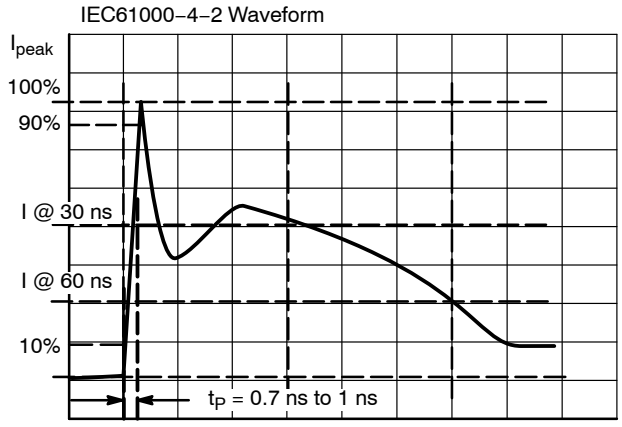
Figure 13. Positive and Negative TLP Waveforms

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to On Semiconductor Application Notes AND8307/D and AND8308/D.

IEC61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



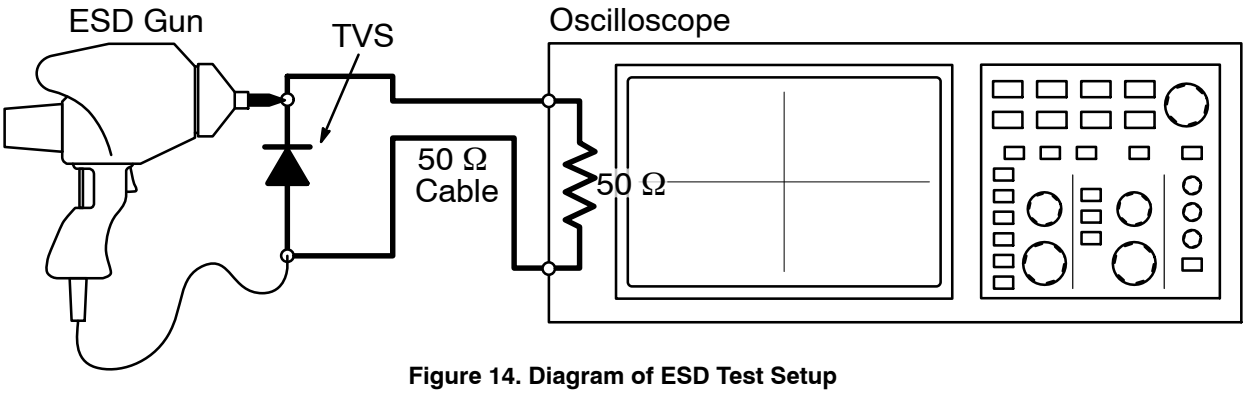


Figure 14. Diagram of ESD Test Setup

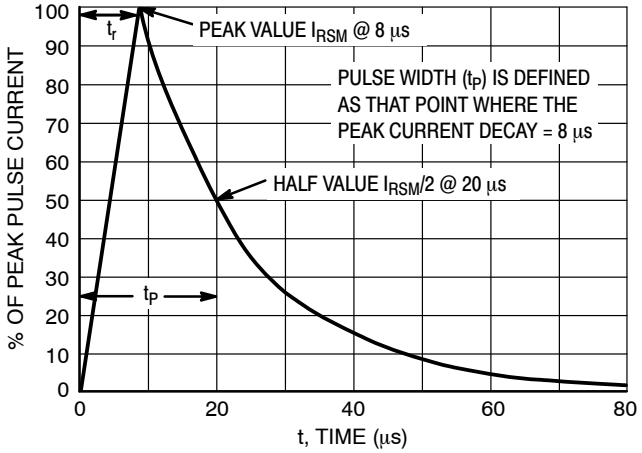


Figure 15. 8 x 20 μs Pulse Waveform

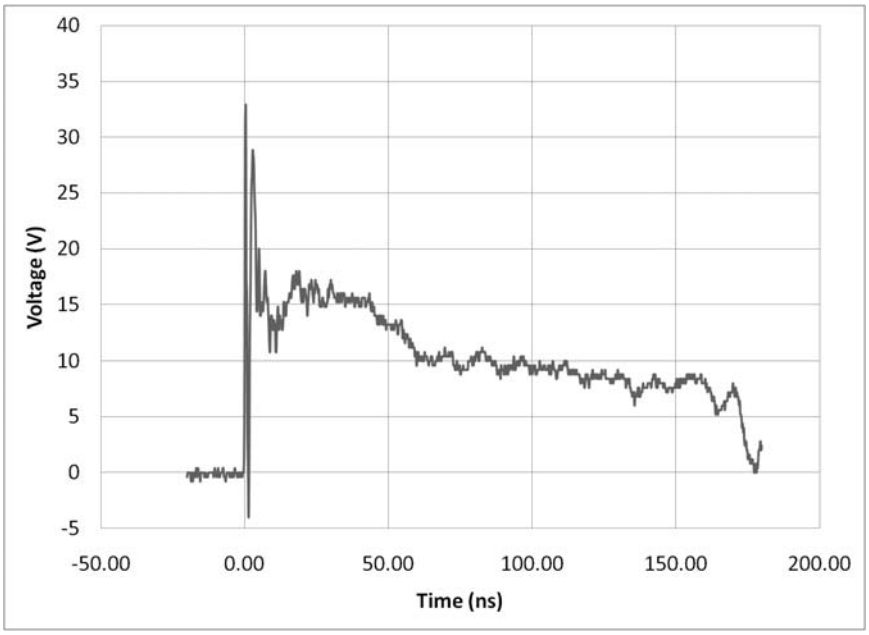


Figure 16. ESD Clamping Voltage +8 kV per IEC6100−4−2 (external to internal pin)

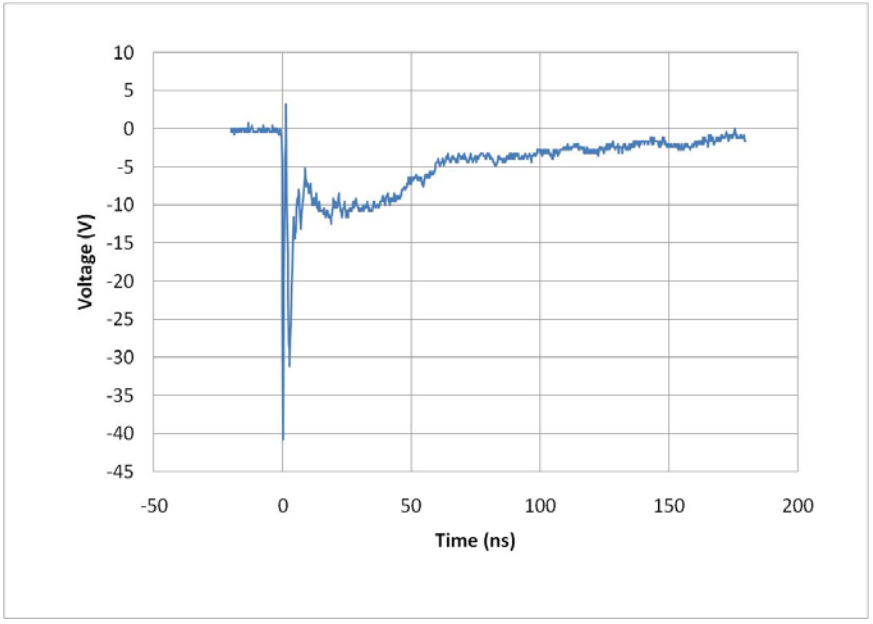


Figure 17. ESD Clamping Voltage −8 kV per IEC6100−4−2 (external to internal pin)

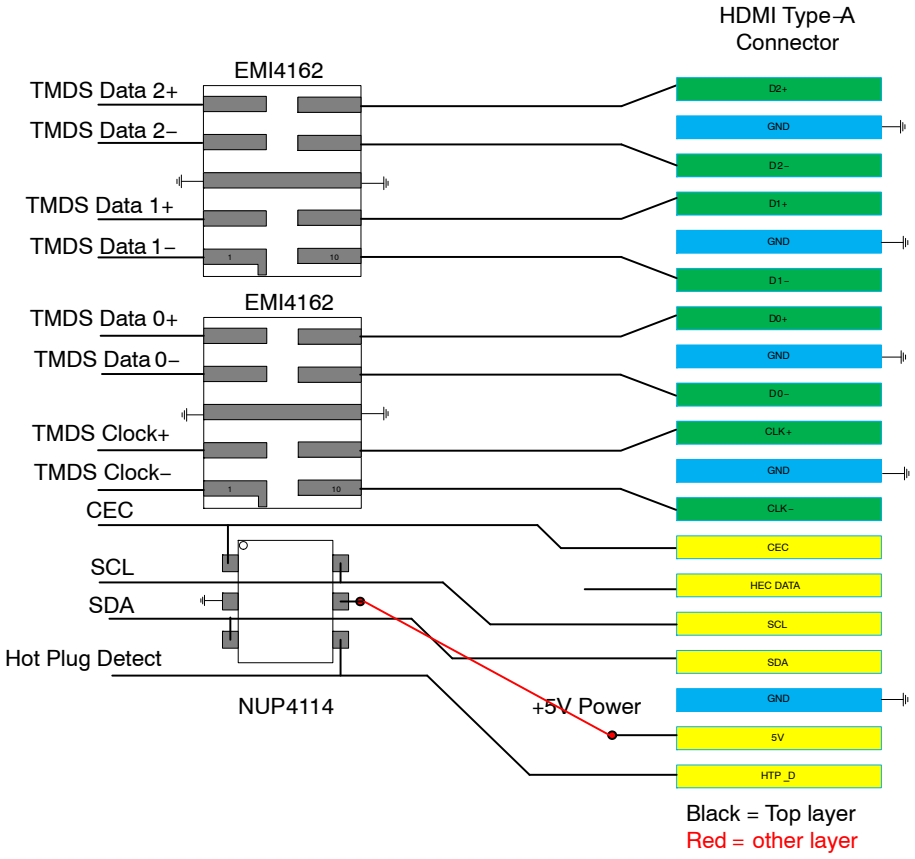


Figure 18. EMI4162 HDMI Type – A Connector Application Diagram

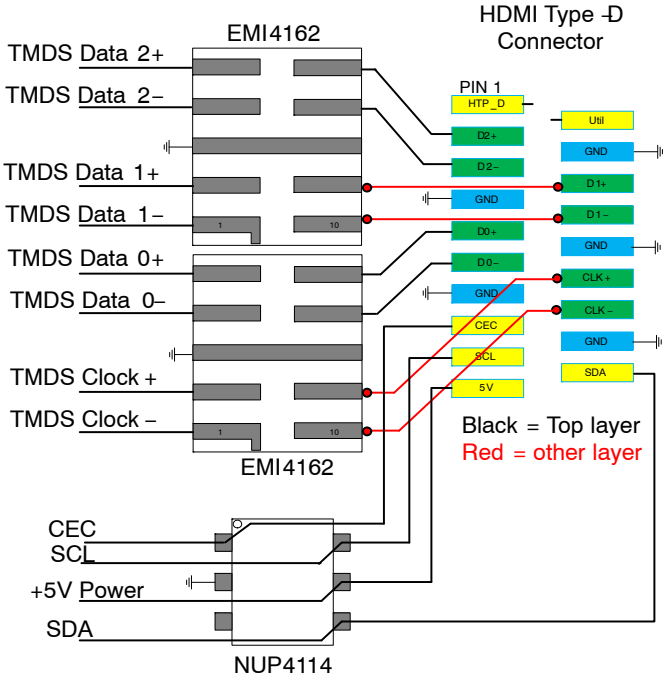
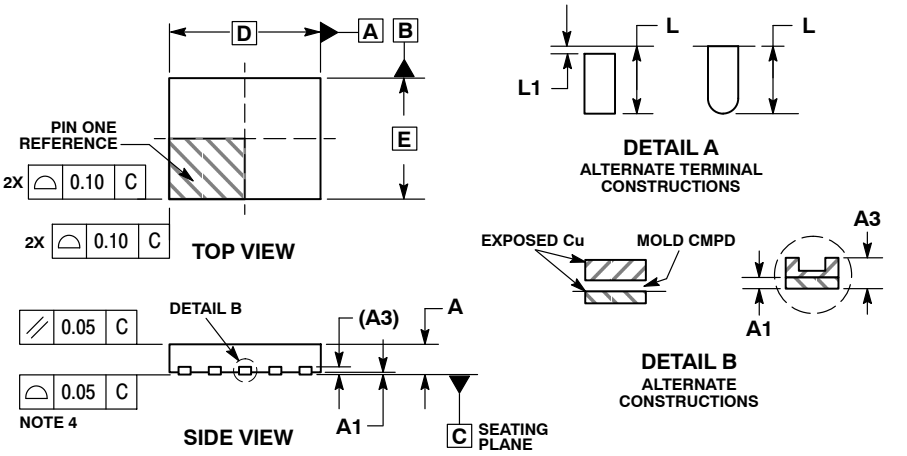


Figure 19. EMI4162 HDMI Type – D Connector Application Diagram

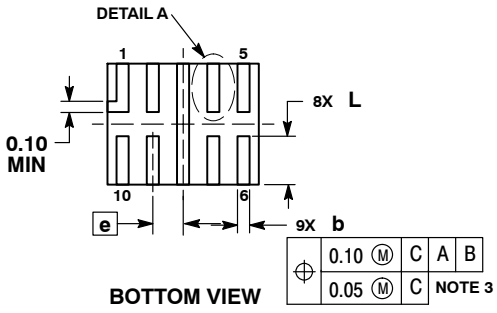
PACKAGE DIMENSIONS

UDFN10 2.5x2, 0.5P
CASE 517CJ
ISSUE O

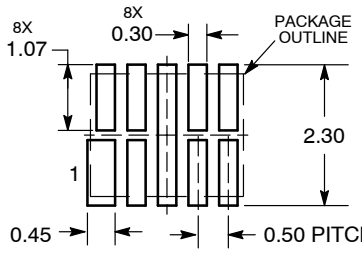


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	2.50 BSC	
E	2.00 BSC	
e	0.50 BSC	
L	0.70	0.90
L1	0.05	0.15



RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Email: orderlit@onsemi.com

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ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

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