Ordering number : EN*A2200

LV71402RA

Advance Information

ON Semiconductor®

http://onsemi.com

Bi-CMOS LSI

1.5A, 2-Cell Li-ion Battery DC-DC USB Charger

3 Current Modes (500 mA / 900 mA / 1.5 A)

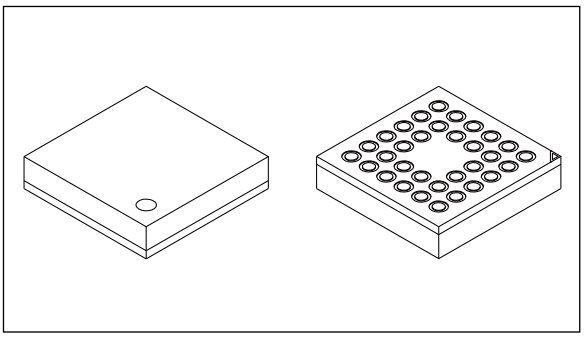
Overview

The LV71402RA is a 1ch DC-DC boost converter which is suitable for charge control usage such as charging 2Cell Li-ion battery (e.g. D-SLR, DVC) from USB port. Since it is corresponding to 3 current modes (500mA/900mA/1.5A) from the port, when it determines that there is no current capability on the port, it will automatically set suppliable current mode. By having a variety of internal protection circuits, inrush current generated by connecting/removing USBs or Li-ion batteries can be controlled – Enables safe charging.

LV71402RA also has an internal mode that is not only used as Li-ion battery charger, but also as a VOUT=8.35V Fixed boost converter which will enable set driving without batteries.

Function

- 1ch Synchronous boost converter (Internal FET)
- LDO Trickle charge at Low voltage
- 3-mode-compatible USB supply current (500mA/900mA/1.5A)
- USB Supply current capability auto-detection
- Internal Soft start function (Current slope : 10msec)
- Automatic recharging function
  (Recharges when VOUT is below 7.8V after judged as fully-charged)
- Switching frequency 1MHz/2MHz Switching function
- Charge/Boost Mode switching function
- LED Pin/CHG_OK Pin for Charging condition check
- Input voltage operation range : 4.0 to 6.0V
- Current at Shutdown < 1uA
- Full-charged voltage : 8.35V±0.5%
- High efficiency charge 93%
- Charging inception Anomaly detection
  (2 hours of LDO Trickle charge will set Standby mode)
- I/O over-voltage protection - OVP
- I/O over-current protection - OCP
- Thermal Shutdown
- Thermistor temperature detection
- Pin control/I^2C bus control selectable



FLGA32(3.5X3.5)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

* I^2C Bus is a trademark of Philips Corporation.

Specifications

Absolute Maximum Ratings at Ta = 25°C

PARAMETER	SYMBOL	CONDITION	RATING	UNIT
Supply voltage	VINmax	VIN	−0.3 to 9.0	V
Pin voltage	VPINmax1	B0,B1,CHG_EN,BST_EN,TH,SDA, SCL,CS,VDD,IREF,OSC,COMP, CHG_OK	−0.3 to 4.0	V
	VPINmax2	EN,LED,INP	−0.3 to 9.0	V
	VPINmax3	SWOUT,VOUT	−0.3 to 10.0	V
	VPINmax4	BOOT	−0.3 to 14.0	V
Allowable power consumption	Pd max	With a designated board *1	1.8	W
Operating temperature	Topr		−20 to +85	°C
Storage temperature	Tstg		−40 to +125	°C
Junction temperature	Tjmax		+150	°C

*1 : Designated board : 60×60×1.6 mm 2S2P_Glass epoxy

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

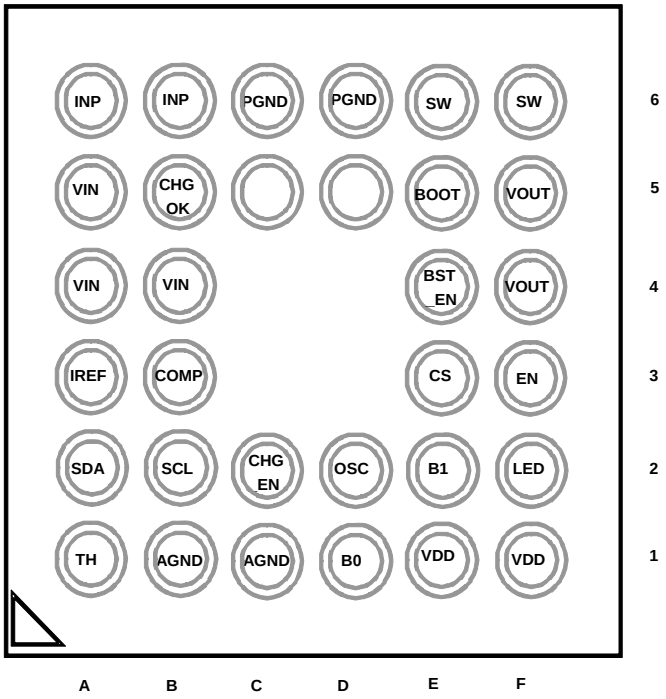
Recommended Operating Conditions at Ta = 25°C

PARAMETER	SYMBOL	CONDITION	RATING	UNIT
Supply-voltage range	VIN		4.0 to 6.0	V

Electrical Characteristics at Ta = 25°C, VIN = 5.0V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	REMARKS
[Supply Current]						
Supply current 1	IVIN1		2	4	mA	EN = ON
Supply current 2	IVIN2			1.0	μA	EN = OFF
[Pin Voltage]						
VOUT Pin voltage	VOUT	8.3	8.35	8.4	V	
VDD Pin voltage	VDD		3.3		V	
TH Pin voltage	VTH		1.65		V	TH Pin = OPEN
[Logic Input/Output Pins]						
EN Pin Input voltage – Level H	VENINH	1		6	V	Pin = EN
EN Pin Input voltage – Level L	VENINL	0		0.5	V	Pin = EN
Input voltage – Level H	VLGINH	2.5		3.6	V	Pin = B0, B1, CHG_EN, BST_EN, SDA, SCL, CS
Input voltage – Level L	VLGINL	0		0.5	V	Pin = B0, B1, CHG_EN, BST_EN, SDA, SCL, CS
Output voltage – Level H	VCHGOKH	3		3.6	V	Pin = CHG_OK
Output voltage – Level L	VCHGOKL	0		0.3	V	Pin = CHG_OK
[Input/Output Current]						
Input current 1	IIN1	80	90	100	mA	VOUT<VIN I^2C_default
Input current 2	IIN2	450	475	500	mA	VOUT>VIN, [B0,B1] = [1,0]
Input current 3	IIN3	810	855	900	mA	VOUT>VIN, [B0,B1] = [0,1] IIN_max = 0.9A
Input current 4	IIN4	1350	1425	1500	mA	VOUT>VIN, [B0,B1] = [1,1] IIN_max = 1.5A
Input Current at End of charge	IEOC		120		mA	VOUT = 8.35V I^2C_default
LED Sink current	ILED		35		mA	VLED = 0.5V
[Limiter Current]						
Input current limit FET(M3) limiter current	IONIN	4			A	
Lo-side switching FET(M2) Limiter current	IONL	4			A	
[ON-Resistance]						
Input current limit FET(M3) ON-resistance	RONIN		110		mΩ	
Hi-side switching FET(M1) ON-resistance	RONH		110		mΩ	
Lo-side switching FET(M2) On-resistance	RONL		110		mΩ	
[Voltage Detection]						
UVLO Lock voltage	VUVLOF	2.6	2.7	2.8	V	VDD Detection system
UVLO Unlock voltage	VUVLON	2.9	3.0	3.1	V	VDD Detection system
OVP Detection level	VOVP	8.7	9	9.3	V	
VIN Current limiter detection level	VINTH	3.7	3.8	3.9	V	
VOUT Recharging voltage	VORECH	7.6	7.8	8	V	I2C_default
[Oscillation Frequency]						
PWM frequency	FPWMOSC		1.0		MHz	I2C_default
Timer frequency	FTIMOSC		32		Hz	COSC = 0.1μF
[PWM Comparator]						
Maximum On duty	DMAX		90		%	
[TH Input Threshold]						
Threshold voltage at Low temperature	VTMIN	2.16	2.4	2.64	V	T = 0°C (B : 3435K = 10kΩ)
Threshold voltage at High temperature	VTMAX	0.7	0.78	0.86	V	T = 60°C (B : 3435K = 10kΩ)

PIN CONFIGURATION (Top view)

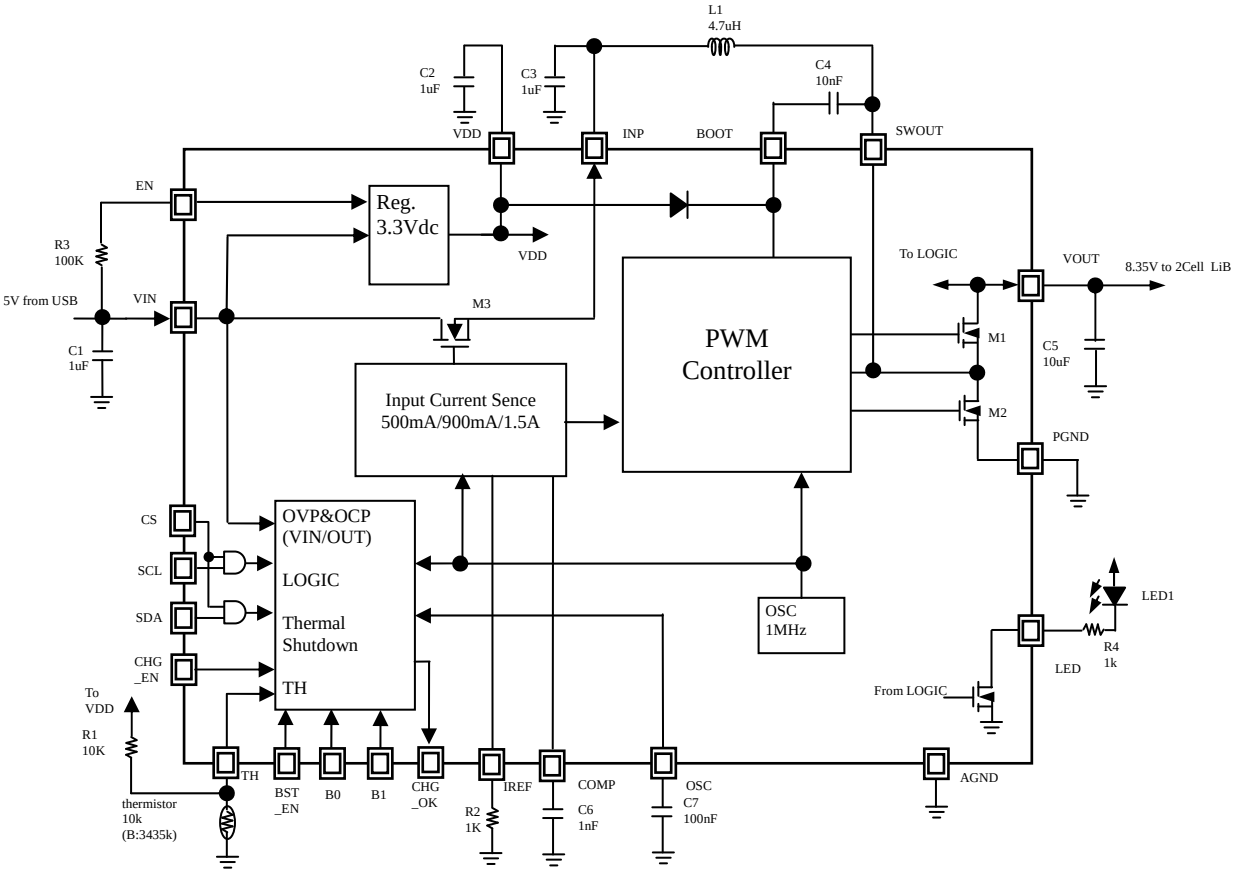


PIN FUNCTIONS

No.	PIN NAME	DESCRIPTION
E1,F1	VDD	Regulator output pin. Provides stable voltage of 3.3V from VIN power supply.
A4,A5,B4	VIN	Pin to provide 5V from USB port.
A6,B6	INP	Converter power supply pin after Input Current Limit FET (M3).
D1	B0	Logic input pin to determine the input current limitation.
E2	B1	Logic input pin to determine the input current limitation.
A3	IREF	Programmed current of the input current limitation. Connect a resistor in between this pin and GND to determine the input current value.
C2	CHG_EN	Charge Enable Input. L = Stop charging operation H = Charging operation
F3	EN	This ICs Enable pin. When EN pin is “H”, VDD powers up and I^2C registers are ready for communication.
F4,F5	VOUT	Boost output pin. Boosted voltage will be generated by the converter operation. Executes charging by connecting a battery in between this pin and PGND. Also Connects 10μF capacitor in parallel with the battery.
E5	BOOT	Hi-side gate voltage driving pin of a converter. Connect capacitor in between SWOUT and BOOT pins.
E6,F6	SWOUT	Switching operation pin of a converter.
D2	OSC	Capacitor connecting pin for timing clock of an internal logic. The clock is set to 32Hz with a 0.1uF ceramic capacitor.
B3	COMP	GM amp phase compensating pin. Phase compensation R embedded. Determines time constant of GM Amp by its external capacity value.
E3	CS	I^2C interface enable input pin. When CS pin is “H”, I^2C_data can be accepted.
F2	LED	Output pin to light up LED while charging the battery.
B1,C1	AGND	Analog Ground
C6,D6	PGND	Power Ground
A1	TH	Thermistor input pin. Connect a NTC Thermistor from TH to GND. Connect a 10kΩ resistor from TH to VDD. Charging is suspended when TH ≥ 2.4V and TH ≤ 0.78V. Set externals OPEN when not using temperature sensing function.
B5	CHG_OK	Logic output pin. This will be “H” when fully-charged.
A2	SDA	I^2C data input pin.
B2	SCL	I^2C clock input pin.
E4	BST_EN	Charging/Boosting mode switching pin. “L” = Charge mode, “H” = Boost mode.

Total : 30PINS

BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

(VIN = 5V, CIN = 1µF, CINP = 1µF, CVDD = 1µF, COUT = 10µF, LOUT = 4.7µH, Ta = +25°C)

LiB=6.8V/980mAh, Charging Characteristic (VOUT)

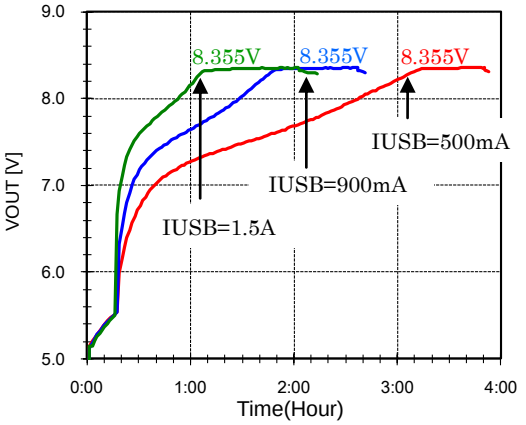


Figure 1.

LiB=6.8V/980mAh, Charging Characteristic (IIN)

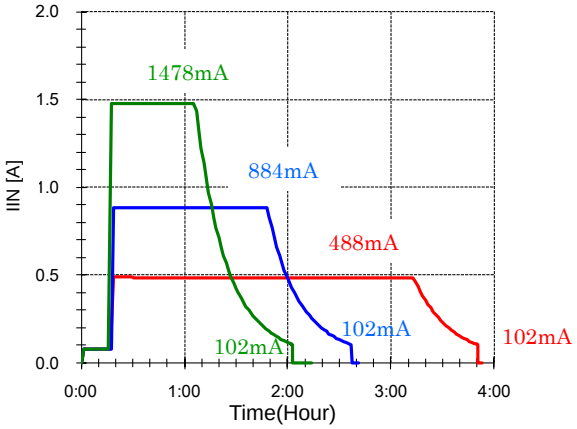


Figure 2.

LiB=6.8V/980mAh, Charging Characteristic (IOUT)

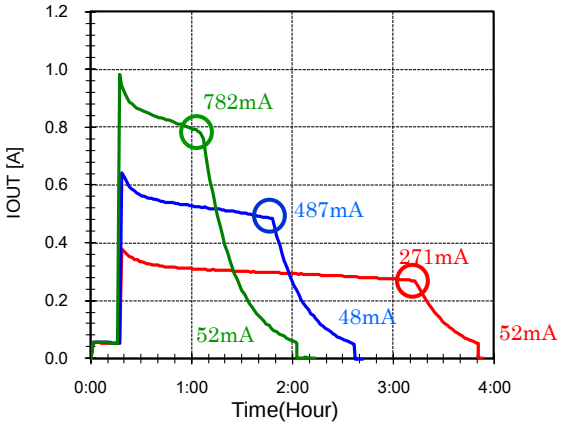


Figure 3.

LiB=6.8V/980mAh, Charging Characteristic (Efficiency)

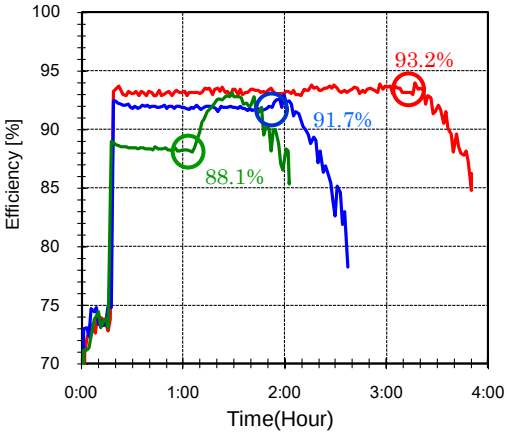


Figure 4.

CC Mode Switching Waveform
(VOUT = 7.4V, IUSB = 1.5A Mode)

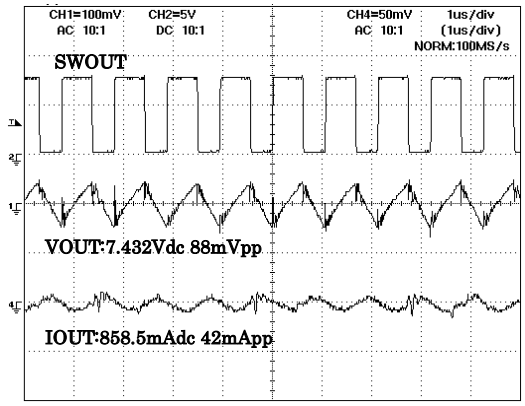


Figure 5.

USB Current Capability Detection Waveform
(USB Supply Current = 0.7A, IUSB = 0.9A Mode)

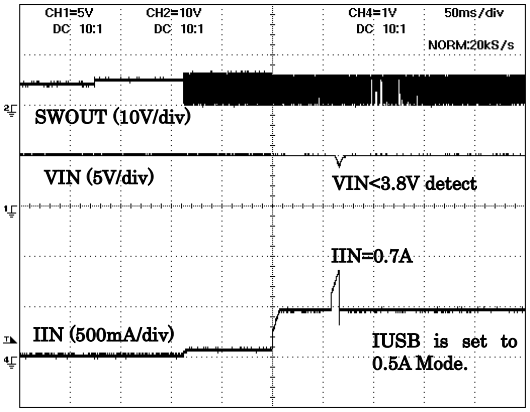
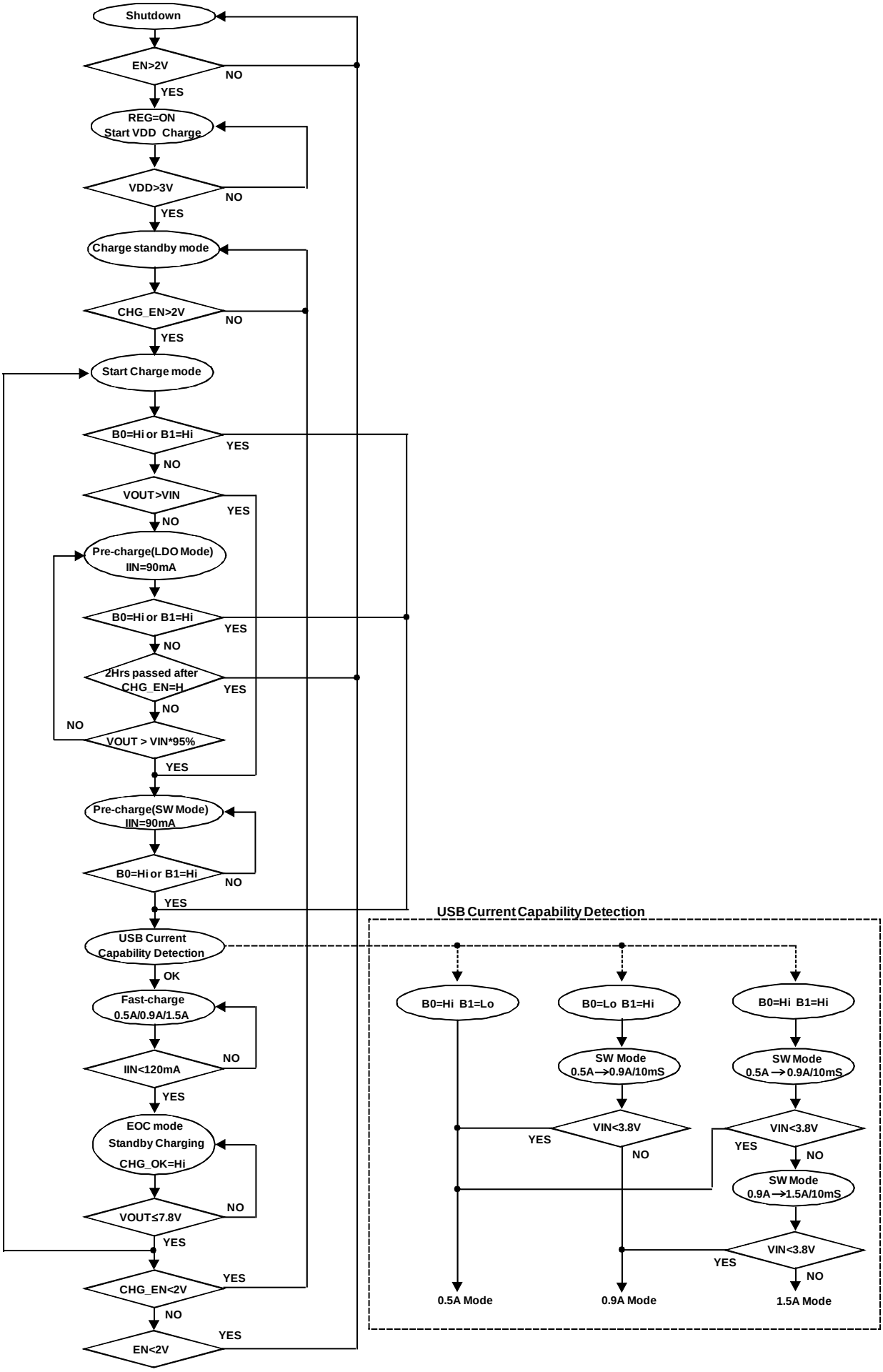


Figure 6.

FLOW CHART


Shutdown
EN>2V
NO
YES
REG=ON
Start VDD Charge
VDD>3V
NO
YES
Charge standby mode
CHG_EN>2V
NO
YES
Start Charge mode
B0=Hi or B1=Hi
YES
NO
VOUT>VIN
YES
NO
Pre-charge(LDO Mode)
IIN=90mA
B0=Hi or B1=Hi
YES
NO
2Hrs passed after
CHG_EN=H
YES
NO
NO
VOUT > VIN*95%
YES
Pre-charge(SW Mode)
IIN=90mA
B0=Hi or B1=Hi
NO
YES
USB Current
Capability Detection
OK
Fast-charge
0.5A/0.9A/1.5A
IIN<120mA
NO
YES
EOC mode
Standby Charging
CHG_OK=Hi
VOUT≤7.8V
NO
YES
CHG_EN<2V
YES
NO
EN<2V
YES
USB Current Capability Detection
B0=Hi B1=Lo
B0=Lo B1=Hi
B0=Hi B1=Hi
SW Mode
0.5A→0.9A/10mS
SW Mode
0.5A→0.9A/10mS
VIN<3.8V
YES
NO
VIN<3.8V
YES
NO
SW Mode
0.9A→1.5A/10mS
VIN<3.8V
YES
NO
0.5A Mode
0.9A Mode
1.5A Mode

ABOUT I²C-BUS

1. A Method of data transfer

This IC has adopted Serial data controlling method (I²C-BUS) and controls with SCL and SDA pins, and CS pin for noise suppression. When CS pin is "H", I²C interface accepts data transfer of SCL and SDA. When CS pin is "L", I²C interface doesn't accept them. If CS pin is not used, it must be pulled up to VDD pin. A Method of data transfer is below. First, set Data transfer start condition (*1) by using these two pins, then input 8-bit data to SDA pin. This 8-bit data needs to be synchronized to SCL pin clock. It is necessary to start transferring from MSB (Most Significant Bit) side. The 9th-bit is going to be the ACK (Data transfer acknowledge) period, and while SCL pin is "H", this IC will "Pull-down" an SDA pin. After transferring necessary data, complete transferring by setting End of data transfer condition (*2) by using two pins.

*1) Define by falling SDA while SCL is in "H" period.
*2) Define by rising SDA while SCL is in "H" period.

2. Data transfer format

After transferring the Start condition, transfer Slave address, followed by sub-address, control data, Ending condition to the SDA pin (See Diagram 1). Since this IC does not have Auto address increment function, Slave address, Sub-address, and Control data must be transferred as a set. The slave-address is configured in 7-bit with having its 8th-bit as a READ/WRITE setting bit. Therefore, set "L" at WRITE mode, and set "H" at READ mode.

• Write Mode

STA	IC-ADD	R/W	A	SUB-ADD	A	DATA	A	STO

STA : Start Condition STO : Stop Condition A [1Bit] : ACK
IC-ADD [7Bit] : Slave address R/W[1Bit] : Read/Write(Read:1/Write:0)
SUB-ADD [8Bit] : Sub address DATA [8Bit] : Data Bits

• Read Mode

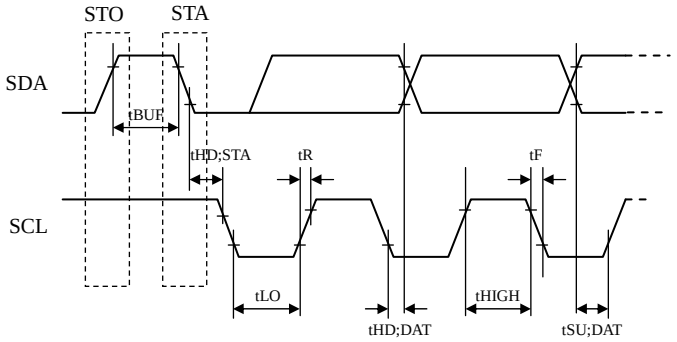
STA	IC-ADD	R/W	A	STATUS1	A	STATUS2	A	STO

STATUS1/2[8Bit] : Status Bits

Diagram 1 : Data configuration diagram

3. Input Timing

Transfer Input data in a timing shown in Diagram 2 (See Table 1).



STA : Start Condition
STO : Stop Condition

Diagram 2 : Input timing

Table 1 : Electrical characteristics at Ta = 25 °C

PARAMETER	SYMBOL	STANDARD		HIGH SPEED		UNIT
		min.	max.	min.	max.	
SCL Frequency	FSCL	0	100	0	400	kHz
BUS free time between stop - start	tBUF	4.7	-	1.3	-	μs
HOLD time of start, restart condition	tHD;STA	4.0	-	0.6	-	μs
L time of SCL	tLOW	4.7	-	1.3	-	μs
H time of SCL	tHIGH	4.0	-	0.6	-	μs
Set-up time of restart condition	tSU;STA	4.7	-	0.6	-	μs
HOLD time of SDA	tHD;DAT	0	-	0	0.9	μs
Set-up time of SDA	tSU;DAT	250	-	100	-	ns
Rising time of SDA, SCL	tR	-	1000	20+0.1Cb(*3)	300	ns
Falling time of SDA, SCL	tF	-	300	20+0.1Cb(*3)	300	ns

*3) Cb : Total capacitance of one BUS line (unit : pF)

I²C-BUS REGISTER MAP

WRITE : IC Address: 10111010

Func.	SUB_ ADDRESS	MSB							LSB
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
CTL1	0	CHG_BUS	CHG_EN	BST_BUS	BST_EN	PWM_FREQ	IUSB_BUS	IUSB[1:0]	
		0	0	0	0	0	0	0	0
CTL2	1	VRECHG[1:0]		EOC[1:0]		SWPCHG[1:0]		LDOPCHG[1:0]	
		1	0	0	0	0	0	0	0
CTL3	2	ERR_LED[1:0]							
		1	0	0	0	0	0	0	0
	3								
		0	0	0	0	0	0	0	0
TEST1	4	TEST MODE (WRITE prohibited)							
TEST2	5	TEST MODE (WRITE prohibited)							
TEST3	6	TEST MODE (WRITE prohibited)							
TEST4	7	TEST MODE (WRITE prohibited)							
TEST5	8	TEST MODE (WRITE prohibited)							
TEST6	9	TEST MODE (WRITE prohibited)							
TEST7	10	TEST MODE (WRITE prohibited)							
TEST8	11	TEST MODE (WRITE prohibited)							
TEST9	12	TEST MODE (WRITE prohibited)							

READ : IC Address: 10111011

Function	MSB							LSB
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
READ1	CHG_OK	ERR	VIN_LO	UVLO	VIN_OVP	VOUT_OVP	VIN_OCP	LDO2H
READ2	TH	TSD	LDO_PG	SW_PG	BST_MODE	CHG_MODE	IUSB_MODE	

I²C-BUS Registers

WRITE : IC Address: 10111010

SUB_ ADDRESS	Bit	Name	Init	DESCRIPTION
0 [CTL1]	[7]	CHG_BUS	0b	Pin/I²C Control : **0b = CHG_EN Pin control,** 1b = I²C control
	[6]	CHG_EN	0b	Charge Enable (When CHG_BUS = 1b) : **0b = Charge disable**, 1b = Charge enable
	[5]	BST_BUS	0b	Pin/I²C Control : **0b = BST_EN Pin control,** 1b = I²C control
	[4]	BST_EN	0b	Boost Mode Enable (When BST_BUS=1b) : **0b = Charge mode,** 1b = Boost mode.
	[3]	PWM_FREQ	0b	PWM Frequency : **0b = 1MHz**, 1b = 2MHz
	[2]	IUSB_BUS	0b	Pin/I²C Control : **0b = B1/B0 Pin control,** 1b = I²C control
	[1]	IUSB[1:0]	00b	USB Input Current Limit (When IUSB_BUS=1b) : **00b = LDOPCHG/SWPCHG Set value** 01b = 500mA, 10b = 900mA, 11b = 1500mA
	[0]			
1 [CTL2]	[7]	VRECHG[1:0]	10b	Battery Recharge Voltage : 00b = 7.0V, 01b = 7.4V, **10b = 7.8V**, 11b = Not Recharging
	[6]			
	[5]	EOC[1:0]	00b	End Of Charge (Input current is detected at IIN) **00b = 120mA**, 01b = 150mA, 10b = 180mA, 11b = 210mA
	[4]			
	[3]	SWPCHG[1:0]	00b	Pre-Charge Current Limit (SW Mode) : **00b = 90mA**, 01b = 120mA, 10b = 150mA, 11b = 180mA
	[2]			
	[1]	LDOPCHG[1:0]	00b	Pre-Charge Current Limit (LDO Mode) : **00b = 90mA**, 01b = 120mA, 10b = 150mA, 11b = 180mA
	[0]			
2 [CTL3]	[7]	ERR_LED[1:0]	10b	LED display at Anomaly detection (Charge suspend) 00b = Lights-out, 01b = blinking at 2Hz, **10b = blinking at 4Hz,** 11b = Lights-on
	[6]			

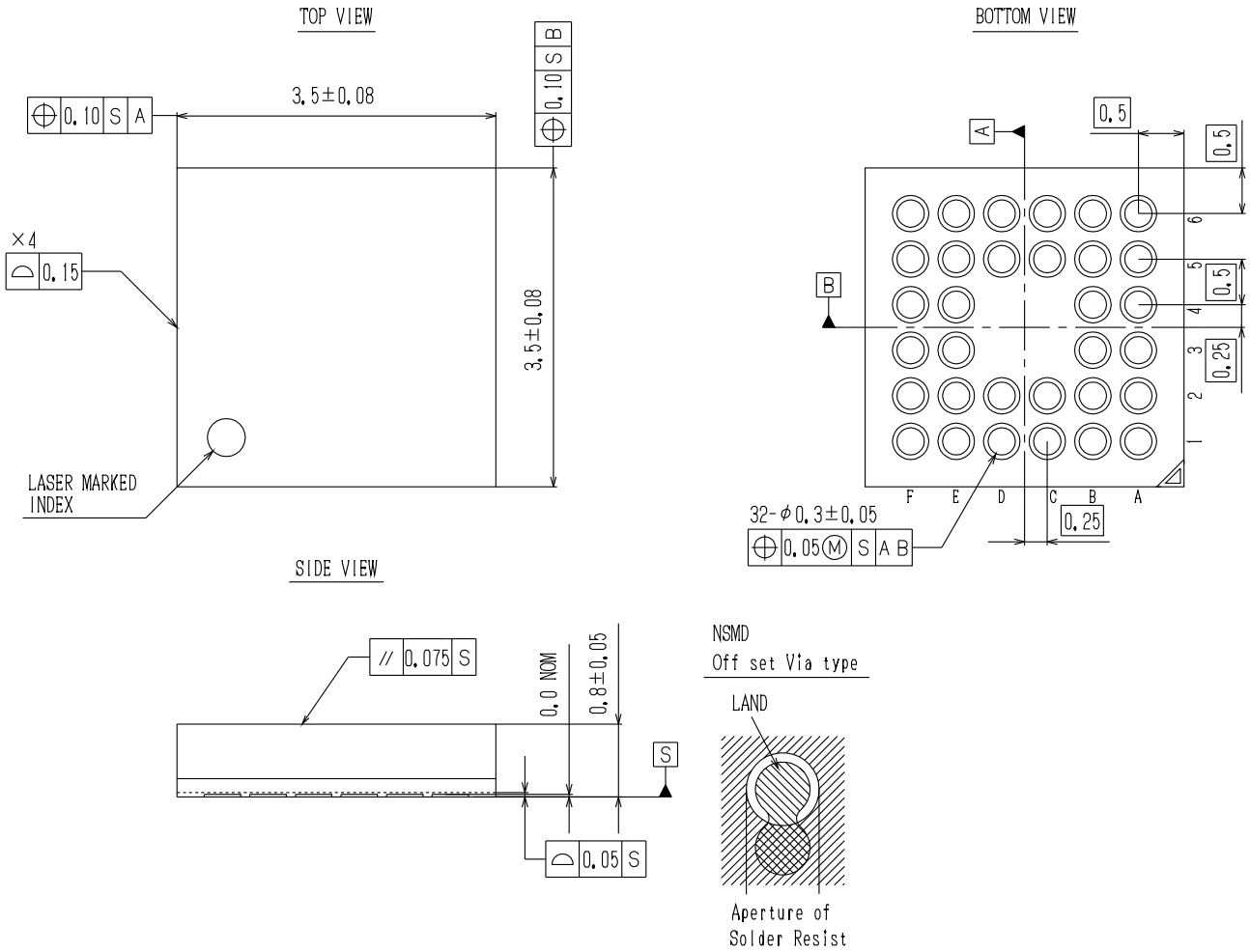
READ : IC Address : 10111011

	Bit	Name	DESCRIPTION
READ1	[7]	CHG_OK	End of charge Detection : 0b = Not End of charge, 1b = End of charge
	[6]	ERR	Charge Error : 0b = Not Error, 1b = Error (When protection circuits work)
	[5]	VIN_LO	VIN Low Voltage Detection : 0b = VIN>3.8V, 1b = VIN<3.8V
	[4]	UVLO	VDD Low Voltage Detection : 0b = VDD>2.8V, 1b = VDD<2.8V
	[3]	VIN_OVP	VIN Over Voltage Detection : 0b = VIN<6.3V, 1b = VIN>6.3V
	[2]	VOUT_OVP	VOUT Over Voltage Detection : 0b = VOUT<9V, 1b = VOUT>9V
	[1]	VIN_OCP	VIN Over Current Detection : 0b = VIN Current< 2A, 1b = VIN Current > 2A
	[0]	LDO2H	LDO Mode Safety Timer Detection : 0b = LDO Mode<2hrs, 1b = LDO Mode>2hrs
READ2	[7]	TH	Thermistor Sense Detection : 0b = Normal Charge, 1b = Thermistor Cold/Hot Temperature
	[6]	TSD	Thermal Shutdown Detection : 0b = Tj <140°C, 1b = Tj >160°C
	[5]	LDO_PG	VOUT Voltage Detection 1 : 0b = VOUT<VIN*95%, 1b = VOUT>VIN*95%
	[4]	SW_PG	VOUT Voltage Detection 2 : 0b = VOUT<7.8V, 1b = VOUT>7.8V
	[3]	BST_MODE	Boost Mode : 0b = Charge Mode, 1b = Boost Mode
	[2]	CHG_MODE	Charge Mode : 0b = LDO Mode, 1b = SW Mode
	[1]	IUSB_MODE	USB Input Current Limit Condition (Internal Logic Condition) : 00b = Pre-Charge, 01b = 500mA, 10b = 900mA, 11b = 1500mA
	[0]		

Package Dimension

FLGA32(3.5X3.5)

unit : mm



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