Ordering number : ENA1868A

LV8414CS

ON Semiconductor®

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Bi-CMOS IC

Microstep Driver Motor Driver IC

Overview

The LV8414CS is a motor driver IC that incorporates two channels of PWM constant-current control micro-step drivers. Miniaturization using the wafer level package (WLP) makes the IC ideally suited for driving the stepping motors used to control the lenses in digital still cameras, cell phone camera modules and other such devices.

Features

- Two channels of 256-division micro-step drivers
- Excitation step proceeds only by step signal input
- Peak excitation current switchable to one of 16 levels
- Serial data control using I^2C interface
- Built-in thermal protection circuit
- Low supply voltage protection circuit incorporated
- On-chip photo sensor drive transistors
- On-chip Schmitt buffer

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage 1	V_M max		6.0	V
Maximum supply voltage 2	V_{CC} max		6.0	V
Output peak current	$I_O$peak	ch1 to 4 t ≤ 10ms, ON-duty ≤ 20%	600	mA
Continuous output current 1	I_O max1	ch1 to 4	400	mA
Continuous output current 2	I_O max2	PI	30	mA
Allowable power dissipation	Pd max	*Mounted on a specified board.	1.0	W
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified circuit board : 40mm×50mm×0.8mm, glass epoxy four-layer board.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Allowable Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage range1	V_M op		2.5 to 5.5	V
Operating supply voltage range2	V_{CC} op		2.5 to 5.5	V
Logic input voltage	V_{IN}		0 to V_{CC}+0.3	V
CLK input frequency	FIN	CLK1 to 2	100	kHz

Electrical Characteristics at Ta = 25°C, V_M = 5.0V, V_{CC} = 3.3V

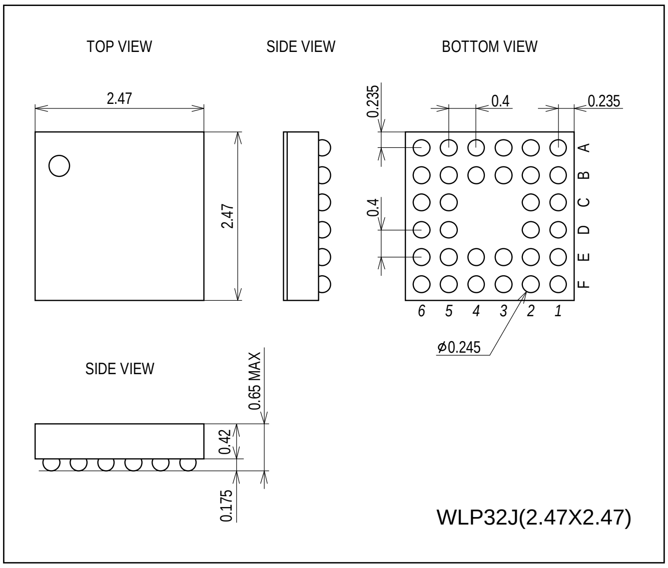
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby mode current drain	Istn	ENA = "L"			1.0	µA
VM current drain	I_M	ENA = "H", IM1 + IM2, with no load	50	100	200	µA
V_{CC} current drain	I_{CC}	ENA = "H"	0.75	1.5	3.0	mA
V_{CC} low-voltage cutoff voltage	$VthV_{CC}$		2.0	2.25	2.5	V
Low-voltage hysteresis voltage	VthHYS		100	150	200	mV
Thermal shutdown temperature	TSD	Design guarantee value *	160	180	200	°C
Thermal hysteresis width	ΔTSD	Design guarantee value *	10	30	50	°C
Micro-step driver						
Logic pin internal pull-down resistance	Rin	ENA, CLK1 to 2, FR1 to 2	50	100	200	kΩ
Logic pin input current	IinL	V_{IN} = 0, ENA, CLK1 to 2, FR1 to 2			1.0	µA
	IinH	V_{IN} = 3.3V, ENA, CLK1 to 2, FR1 to 2	16.5	33	66	µA
Logic high-level voltage	VinH	ENA, SCL, SDA, CLK1 to 2, FR1 to 2	0.6×V_{CC}			V
Logic low-level voltage	VinL	ENA, SCL, SDA, CLK1 to 2, FR1 to 2			0.2×V_{CC}	V
Output on-resistance	Ronu	I_O = 100mA, upper ON resistance		0.38		Ω
	Rond	I_O = 100mA, lower ON resistance		0.22		Ω
	Ron	I_O = 100mA, sum of upper- and lower-side on resistance		0.6	1.0	Ω
Output leakage current	$I_O$leak				1.0	µA
Diode forward voltage	VD	I_D = -100mA	0.45	0.75	1.1	V
Chopping frequency	Fchop00		280	400	520	kHz
	Fchop01		140	200	260	kHz
	Fchop10		420	600	780	kHz
	Fchop11		210	300	390	kHz
Current setting reference voltages	VSEN00		0.185	0.200	0.215	V
	VSEN01		0.175	0.190	0.205	V
	VSEN02		0.165	0.180	0.195	V
	VSEN03		0.155	0.170	0.185	V
	VSEN04		0.145	0.160	0.175	V
	VSEN05		0.135	0.150	0.165	V
	VSEN06		0.125	0.140	0.155	V
	VSEN07		0.115	0.130	0.145	V
	VSEN08		0.105	0.120	0.135	V
	VSEN09		0.095	0.110	0.125	V
	VSEN10		0.085	0.100	0.115	V
	VSEN11		0.075	0.090	0.105	V
	VSEN12		0.065	0.080	0.095	V
	VSEN13		0.055	0.070	0.085	V
	VSEN14		0.045	0.060	0.075	V
	VSEN15		0.035	0.050	0.065	V
PI (Photo sensor driving transistor)						
Output on-resistance	Ron	I_O = 10mA		1.5	2.5	Ω
Output leakage current	$I_O$leak				1.0	µA
Schmitt buffer						
Logic input high-level voltage	VinH	BI1, BI2	0.5×V_{CC}			V
Logic input low-level voltage	VinL	BI1, BI2			0.25×V_{CC}	V

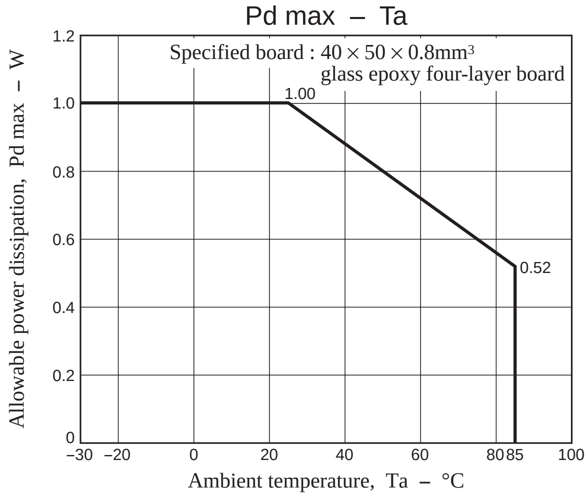
* : Design target value, not to be measured at production test.

Package Dimensions

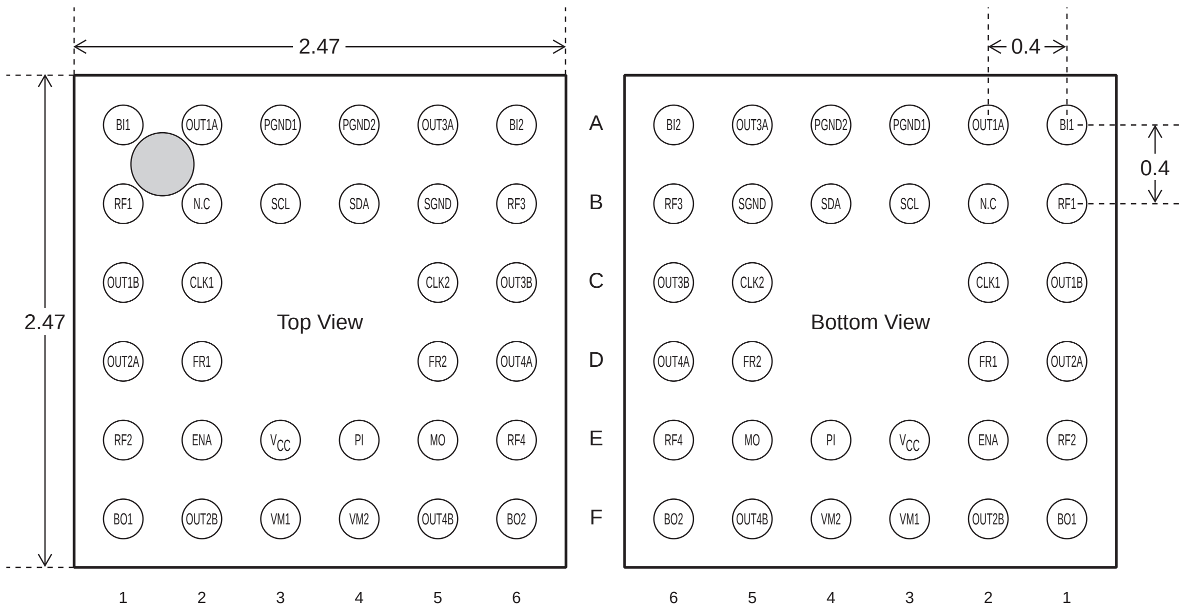
unit : mm (typ)

3406

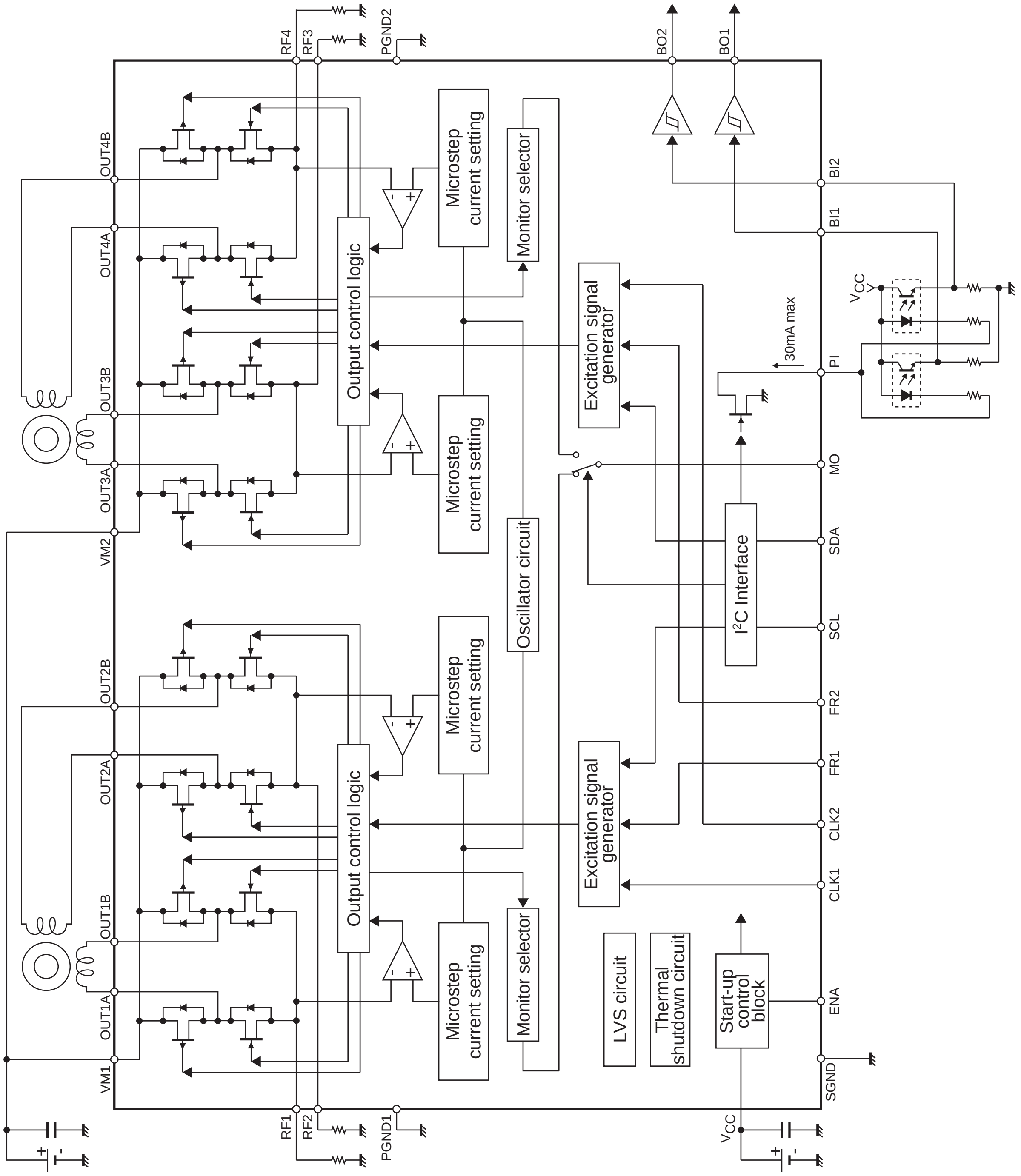




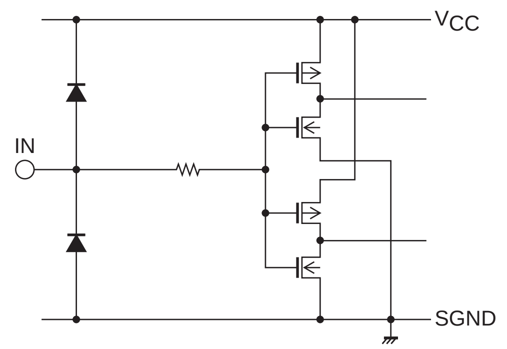
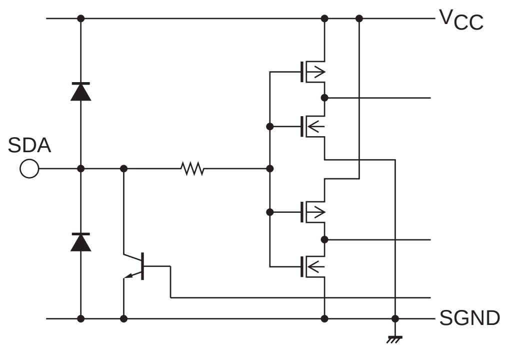
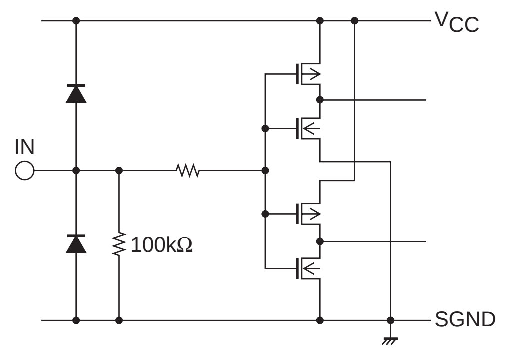
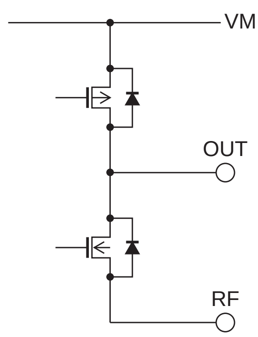
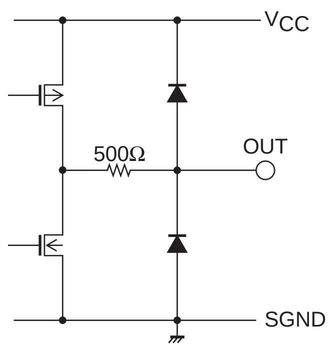
Pin Assignment



Block Diagram



Pin Functions

Pin No.	Pin Name	Function	Equivalent Circuit
A1 A6	BI1 BI2	Schmitt buffer input pin	
B3	SCL	I^2C Interface	
B4	SDA	I^2C Interface	
E2	ENA	Chip enable pin	
C2 C5	CLK1 CLK2	Step signal input pin	
D2 D5	FR1 FR2	Forward/reverse rotation setting signal input pin	
A2 A5 C1 C6 D1 D6 F2 F5	OUT1A OUT3A OUT1B OUT3B OUT2A OUT4A OUT2B OUT4B	H bridge output pin	
B1 B6 E1 E6	RF1 RF3 RF2 RF4	Current-sense resistor connection pins	
E5	MO	Monitor output pin	
F1 F6	BO1 BO2	Schmitt buffer output pin	

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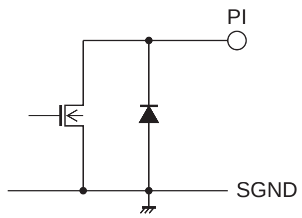
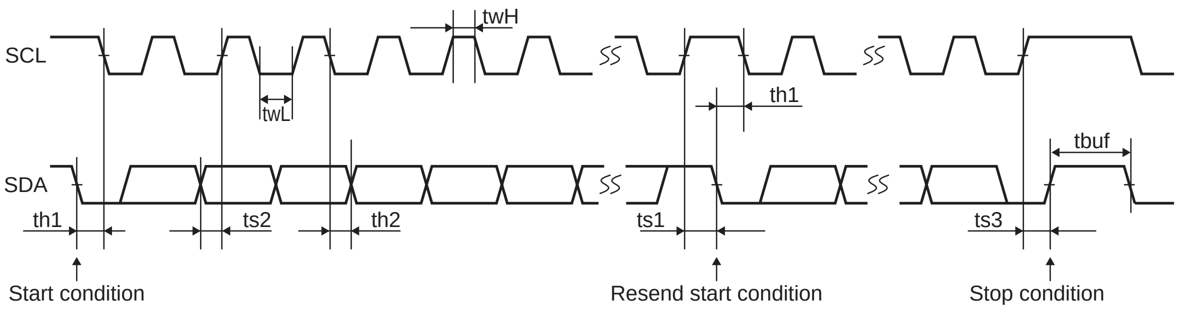
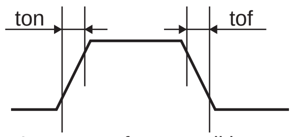
Pin No.	Pin Name	Function	Equivalent Circuit
E4	PI	Photo sensor drive transistor output pin	
E3	V_{CC}	Logic power supply connection pin	
B5	SGND	Signal ground	
F3 F4	VM1 VM2	Motor power supply connection pin	
A3 A4	PGND1 PGND2	Power ground	
B2	N.C.	Unused pin	

Serial Bus Communication Specifications

I²C serial transfer timing conditions





Input waveform condition

Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		100	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	4.7			µs
	ts2	Setup time of SDA with respect to the rising edge of SCL	250			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	4.0			µs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	4.0			µs
	th2	Hold time of SDA with respect to the falling edge of SCL	0.08			µs
Pulse width	twL	SCL low period pulse width	4.7			µs
	twH	SCL high period pulse width	4.0			µs
Input waveform conditions	ton	SCL, SDA (input) rising time			1000	µs
	tof	SCL, SDA (input) falling time			300	µs
Bus free time	tbuf	Interval between stop condition and start condition	4.7			µs

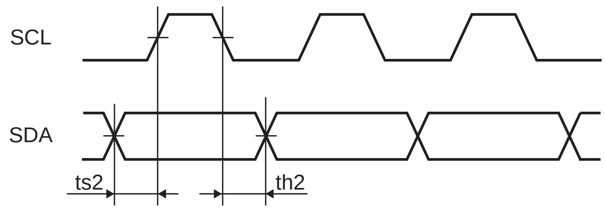
High-speed mode

Parameter	Symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0		400	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	0.6			µs
	ts2	Setup time of SDA with respect to the rising edge of SCL	100			ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	0.6			µs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	0.6			µs
	th2	Hold time of SDA with respect to the falling edge of SCL	0.08			µs
Pulse width	twL	SCL low period pulse width	1.3			µs
	twH	SCL high period pulse width	0.6			µs
Input waveform conditions	ton	SCL, SDA (input) rising time			300	µs
	tof	SCL, SDA (input) falling time			300	µs
Bus free time	tbuf	Interval between stop condition and start condition	1.3			µs

I²C bus transmission method

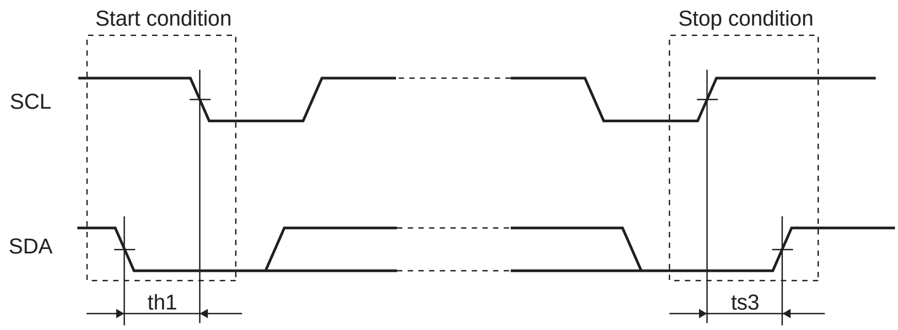
Start and stop conditions

The I²C bus requires that the state of SDA be preserved while SCL is high as shown in the timing diagram below during a data transfer operation.



When data is not being transferred, both SCL and SDA are in the high state. The start condition is generated and access is started when SDA is changed from high to low while SCL and SDA are high.

Conversely, the stop condition is generated and access is ended when SDA is changed from low to high while SCL is high.



Data transfer and acknowledgement response

After the start condition is generated, data is transferred one byte (8 bits) at a time. Any number of data bytes can be transferred consecutively.

An ACK signal is sent to the sending side from the receiving side every time 8 bits of data are transferred. The transmission of an ACK signal is performed by setting the receiving side SDA to low after SDA at the sending side is released immediately after the clock pulse of SCL bit 8 in the data transferred has fallen low.

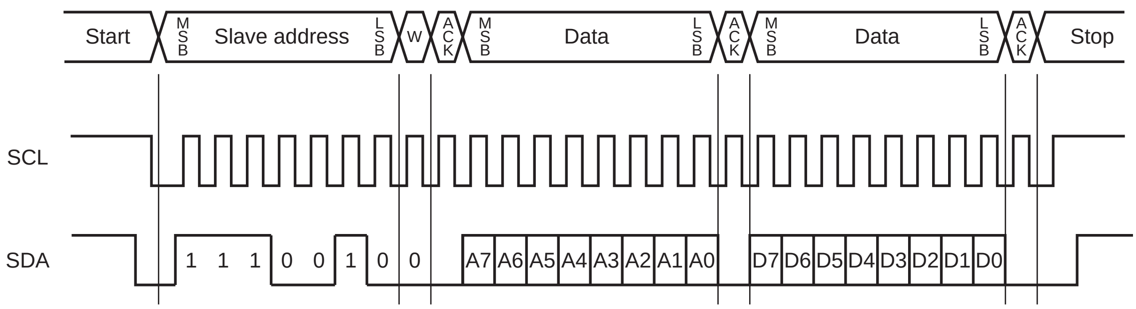
After the receiving side has sent the ACK signal, if the next byte transfer operation is to receive only the byte, the receiving side releases SDA on the falling edge of the 9th clock of SCL.

There are no CE signals in the I²C bus ; instead, a 7-bit slave address is assigned to each device, and the first byte of the transfer data is allocated to the 7-bit slave address and to the command (R/W) which specifies the direction of subsequent data transfer.

The LV8414CS is a drive IC with a dedicated write function and it does not have a read function.

The 7-bit address is transferred in sequence starting with MSB, and the eighth bit is set to low. The second and subsequent bytes are transferred in write mode.

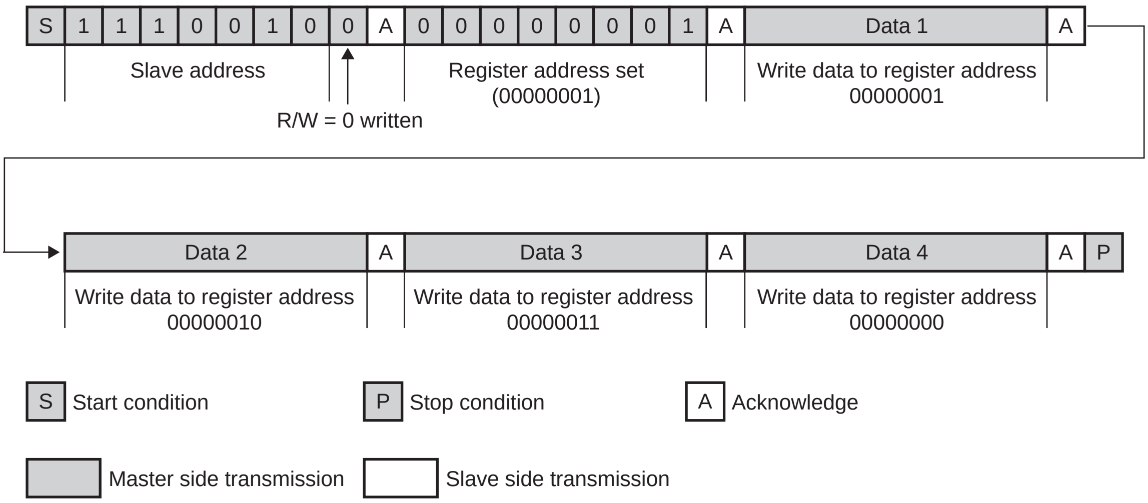
In the LV8414CS, the slave address is stipulated to be “1110010.”.



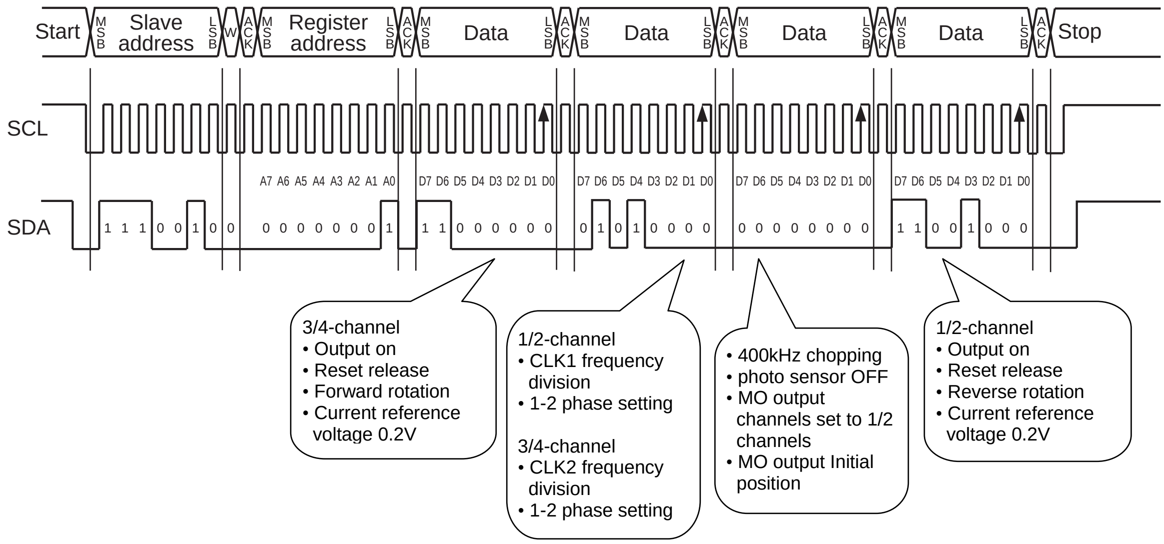
Data transfer write format

The slave address and Write command must be allocated to the first byte (8 bits) and the register address in the “Serial data truth table” must be designated in the second byte.
For the third byte, data transfer is carried out to the address designated by the register address which is written in the second byte. Subsequently, if data continues, the register address value is automatically incremented for the fourth and subsequent bytes.
Thus, continuous data transfer starting at the designated address is made possible.
When the register address is set to “00000011,” the address to which the next byte is transferred wraps around to "00000000."

(1) Data write example



(2) Actual example of continuous data transfer



Based on the “Serial data truth table” on the next page, the following settings are used for the actual example of the continuous data transfer shown in the above figure.
(Data transfer is set at the SCL rising edge of “D0” of each data.)

1/2-channel settings:
Output ON, reset release, reverse (CCW) rotation, current reference voltage setting of 0.2V, no CLK1 frequency division, 1-2 phase setting
3/4-channel settings:
Output ON, reset release, forward (CW) rotation, current reference voltage setting of 0.2V, no CLK2 frequency division, 1-2 phase setting
Other settings:
400kHz chopping frequency, photo sensor OFF, MO output channels set to 1/2 channels, current reference voltage setting of 0.2V

Serial data truth table

Register Address								Data								Setting mode	Set contents
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	*	*	*	*	0	0	0	0	1/2ch Current reference voltage setting	0.200V
								*	*	*	*	0	0	0	1		0.190V
								*	*	*	*	0	0	1	0		0.180V
								*	*	*	*	0	0	1	1		0.170V
								*	*	*	*	0	1	0	0		0.160V
								*	*	*	*	0	1	0	1		0.150V
								*	*	*	*	0	1	1	0		0.140V
								*	*	*	*	0	1	1	1		0.130V
								*	*	*	*	1	0	0	0		0.120V
								*	*	*	*	1	0	0	1		0.110V
								*	*	*	*	1	0	1	0		0.100V
								*	*	*	*	1	0	1	1		0.090V
								*	*	*	*	1	1	0	0		0.080V
								*	*	*	*	1	1	0	1		0.070V
								*	*	*	*	1	1	1	0		0.060V
								*	*	*	*	1	1	1	1		0.050V
								*	*	*	0	*	*	*	*	1/2ch Excitation Direction	CW (forward rotation)
								*	*	*	1	*	*	*	*		CCW (reverse rotation)
								*	*	0	*	*	*	*	*	1/2ch Step/Hold	Clear
								*	*	1	*	*	*	*	*		Hold
								*	0	*	*	*	*	*	*	1/2ch Counter Reset	Reset
								*	1	*	*	*	*	*	*		Clear
								0	*	*	*	*	*	*	*	1/2ch Output Enable	Output OFF
								1	*	*	*	*	*	*	*		Output ON
0	0	0	0	0	0	0	1	*	*	*	*	0	0	0	0	3/4ch Current reference voltage setting	0.200V
								*	*	*	*	0	0	0	1		0.190V
								*	*	*	*	0	0	1	0		0.180V
								*	*	*	*	0	0	1	1		0.170V
								*	*	*	*	0	1	0	0		0.160V
								*	*	*	*	0	1	0	1		0.150V
								*	*	*	*	0	1	1	0		0.140V
								*	*	*	*	0	1	1	1		0.130V
								*	*	*	*	1	0	0	0		0.120V
								*	*	*	*	1	0	0	1		0.110V
								*	*	*	*	1	0	1	0		0.100V
								*	*	*	*	1	0	1	1		0.090V
								*	*	*	*	1	1	0	0		0.080V
								*	*	*	*	1	1	0	1		0.070V
								*	*	*	*	1	1	1	0		0.060V
								*	*	*	*	1	1	1	1		0.050V
								*	*	*	0	*	*	*	*	3/4ch Excitation Direction	CW (forward rotation)
								*	*	*	1	*	*	*	*		CCW (reverse rotation)
								*	*	0	*	*	*	*	*	3/4ch Step/Hold	Clear
								*	*	1	*	*	*	*	*		Hold
								*	0	*	*	*	*	*	*	3/4ch Counter Reset	Reset
								*	1	*	*	*	*	*	*		Clear
								0	*	*	*	*	*	*	*	3/4ch Output Enable	Output OFF
								1	*	*	*	*	*	*	*		Output ON

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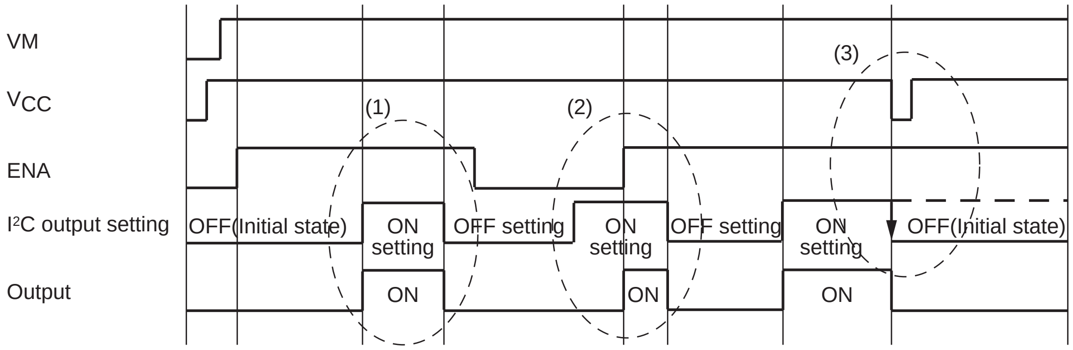
Register Address								Data								Setting mode	Set contents
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	1	0	*	*	*	*	*	*	0	0	1/2ch CLK1 division setting	1 (frequency division)
								*	*	*	*	*	*	0	1		1/2
								*	*	*	*	*	*	1	0		1/4
								*	*	*	*	*	*	1	1		1/8
								*	*	*	*	0	0	*	*	3/4ch CLK2 division setting	1 (frequency division)
								*	*	*	*	0	1	*	*		1/2
								*	*	*	*	1	0	*	*		1/4
								*	*	*	*	1	1	*	*		1/8
								*	*	0	0	*	*	*	*	1/2ch Excitation mode setting	Micro-step
								*	*	0	1	*	*	*	*		1-2 phase
								*	*	1	0	*	*	*	*		1-2 phase (full torque)
								*	*	1	1	*	*	*	*		2 phase
								0	0	*	*	*	*	*	*	3/4ch Excitation mode setting	Micro-step
								0	1	*	*	*	*	*	*		1-2 phase
								1	0	*	*	*	*	*	*		1-2 phase (full torque)
								1	1	*	*	*	*	*	*		2 phase
0	0	0	0	0	0	1	1	*	*	*	*	*	*	0	0	Chopping frequency setting	400kHz
								*	*	*	*	*	*	0	1		200kHz
								*	*	*	*	*	*	1	0		600kHz
								*	*	*	*	*	*	1	1		300kHz
								*	*	*	*	*	0	*	*	Photo sensor driving	OFF
								*	*	*	*	*	1	*	*		ON
								*	*	*	*	0	*	*	*	MO output Channel setting	1/2ch
								*	*	*	*	1	*	*	*		3/4ch
								*	*	*	0	*	*	*	*	MO output position	Initial position
								*	*	*	1	*	*	*	*		1-2 phase position
								*	*	*	*	*	*	*	*	Dummy data	-

Precautions for IC operations

The supply voltage V_{CC}, ENA pin and I^2C output ON setting stand in the following relationship.

- V_{CC}, ENA pin, I^2C output settings, and outputs



(1) No output operations are performed unless the ENA pin is set to high and the I^2C output setting is set to ON.

(2) The I^2C setting is accepted even if the ENA pin is in low state.
(Other I^2C settings are also accepted.)

(3) When the supply voltage V_{CC} is set to low, the internal data is reset.
(The I^2C output setting in the above figure is initialized to OFF state by the fall in the supply voltage V_{CC}.)

ENA pin	I^2C Output Enable setting	Output
L	OFF setting	High-impedance state
H	OFF setting	High-impedance state
L	ON setting	High-impedance state
H	ON setting	Output ON state

Description of stepping motor drive operations

The following state settings related to the control of the stepping motor are established using an I^2C serial data communication.

- Excitation mode : Micro-step (256 divisions), 1-2 phase, 1-2 phase (full torque), or 2-phase
- Excitation direction : CW (clockwise) or CCW (counterclockwise)
- Step/Hold : Clear or Hold
- Counter reset : Clear or Reset
- Output enable : Output Off or Output On
- Current setting reference voltages : Selects one of 16 values
- Chopping frequency : Selects one of 4 values

1. CLK pin function

CLK input		Operating mode
ENA	CLK	
Low	*	Standby mode
High		Excitation step proceeds
High		Excitation step is kept

The excitation steps are advanced by setting the CLK1 (2) from low to high when the ENA is in high state.

2. Initial position

The excitation mode is set to the initial position when the IC is set to the initial state at power-on or when the counter is reset.

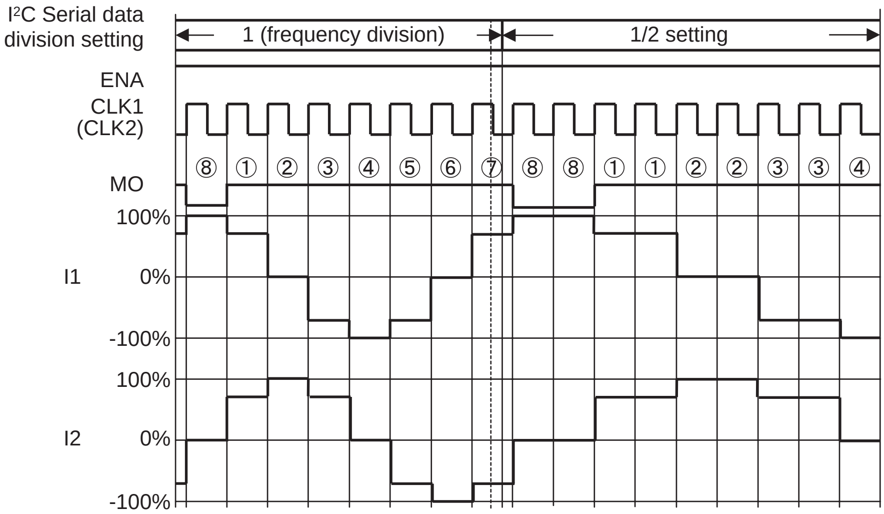
Excitation mode	Initial position	
	1ch (3ch)	2ch (4ch)
256 divisions (16W1-2 phase) Micro-step	100%	0%
1-2 phase	100%	0%
1-2 phase (full torque)	100%	0%
2 phase	100%	-100%

3. MO pin function

By setting the MO output channel and MO output position using the I^2C serial data, the MO pin is set to low at the initial position in each excitation mode or at the 1-2 phase position in the micro-step drive mode.

* It is assumed that the 1-2 phase setting for the MO output is used in the micro-step drive mode. Even if the MO output position is set to 1-2 phase in the 1-2 phase or 2-phase mode, MO is set to low at the initial position and remains unchanged after it is initialized.

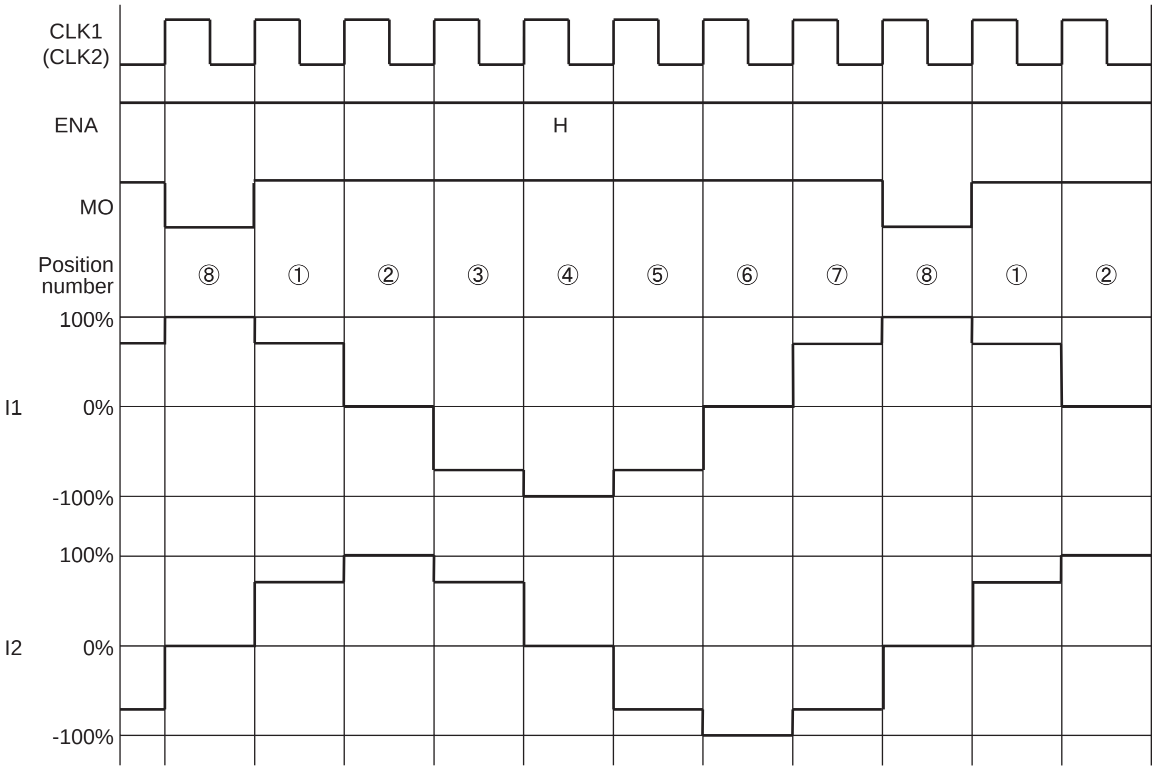
* Since the period during which MO is set to low extends from the rising edge of the CLK which is the setting position, to the rising edge of the CLK which moves to the next phase, care must be taken when a frequency division setting has been established.

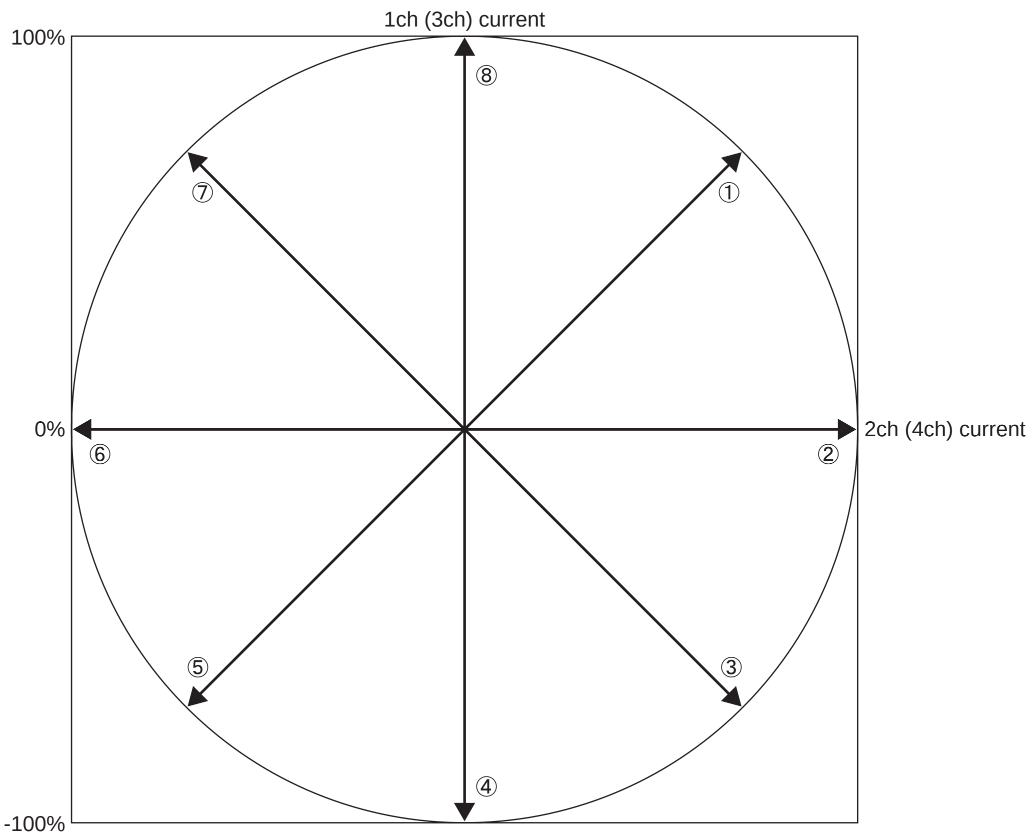


4. Excitation Mode Setting

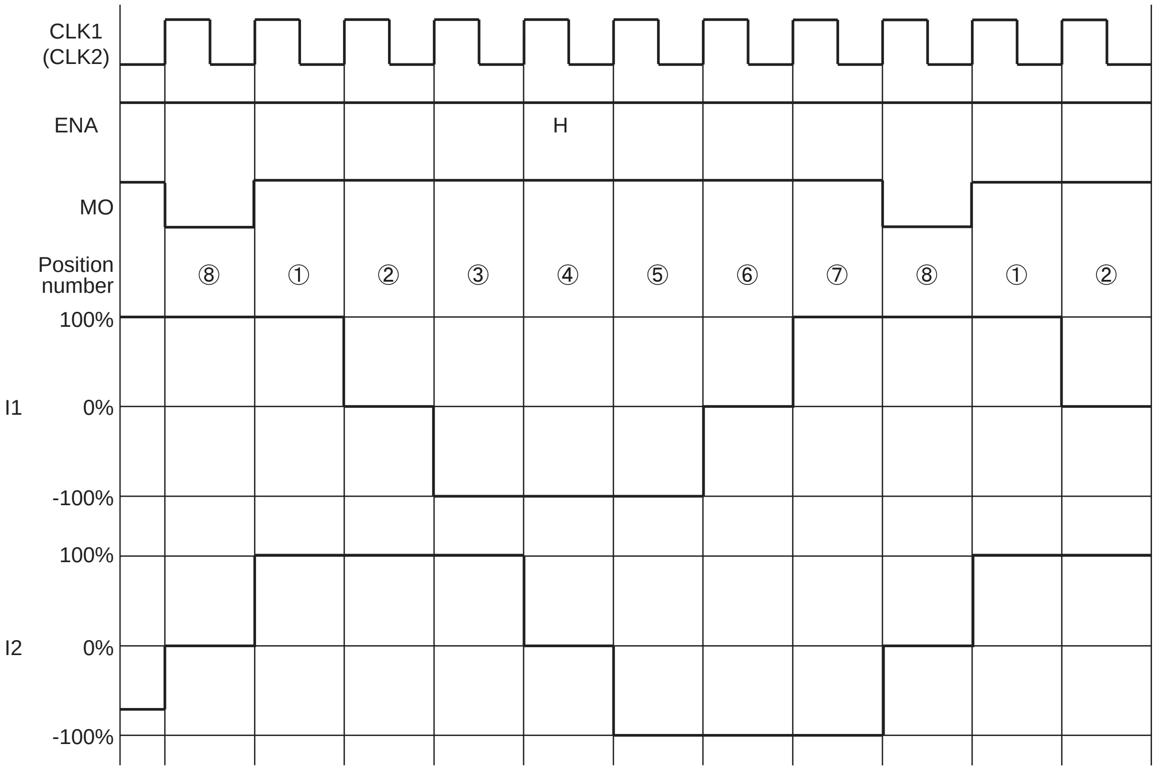
Given below and in the following pages are the timing charts and monitor output pin MO signal in each excitation mode.

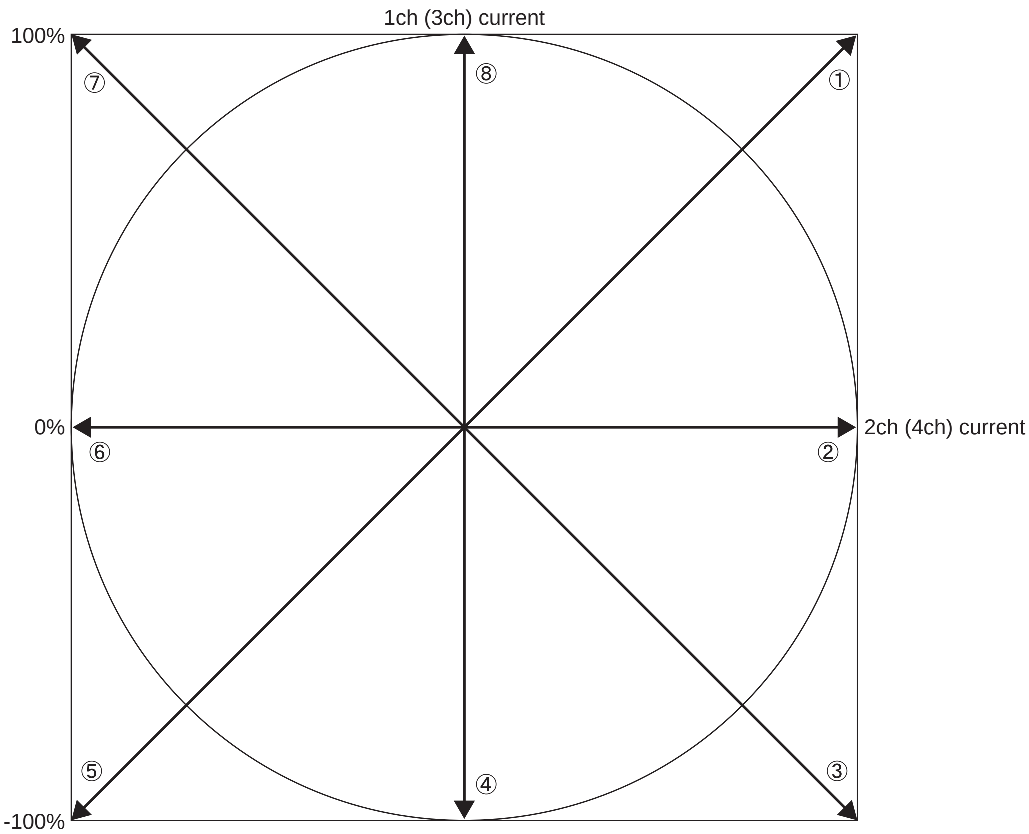
[1-2 Phase Excitation Timing Chart]



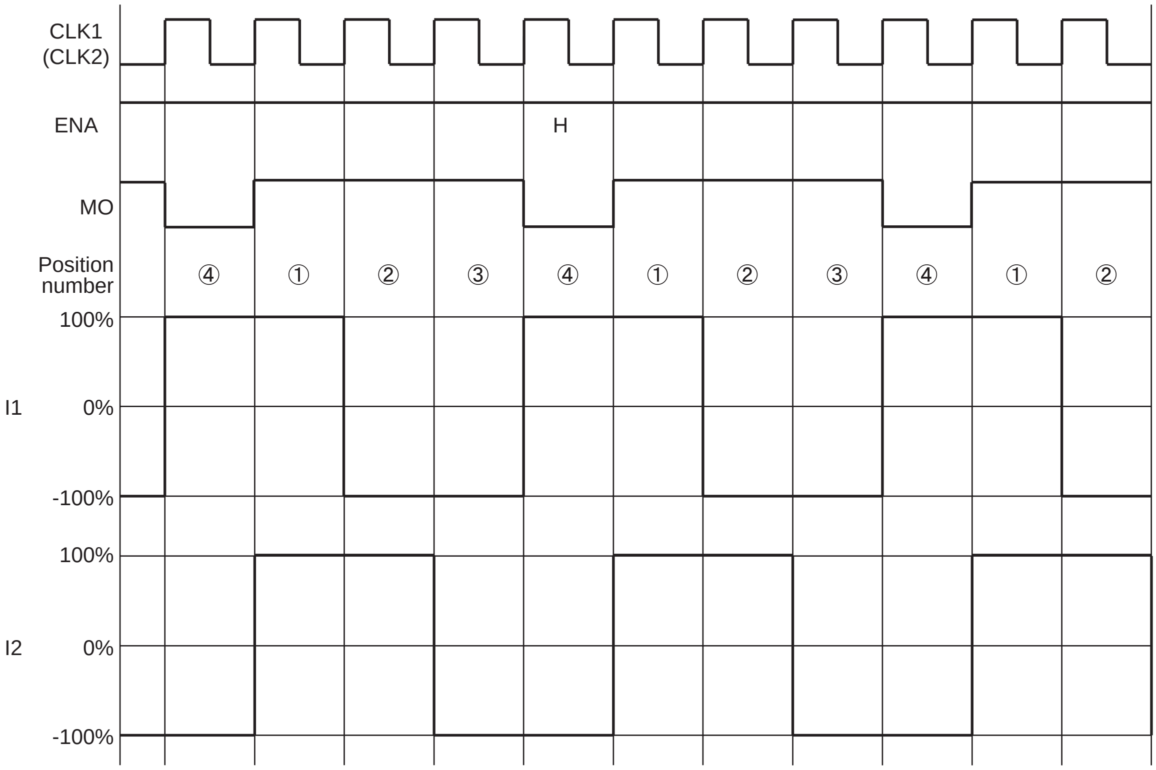


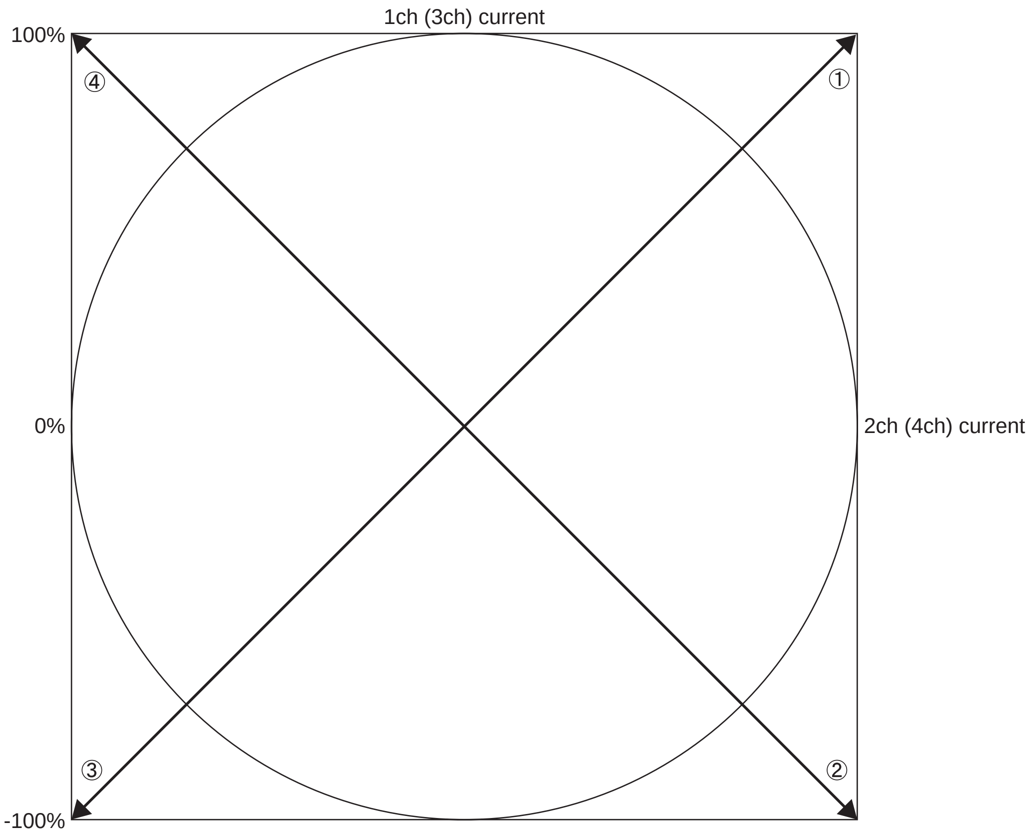
[1-2 Phase Excitation (full torque) Timing Chart]



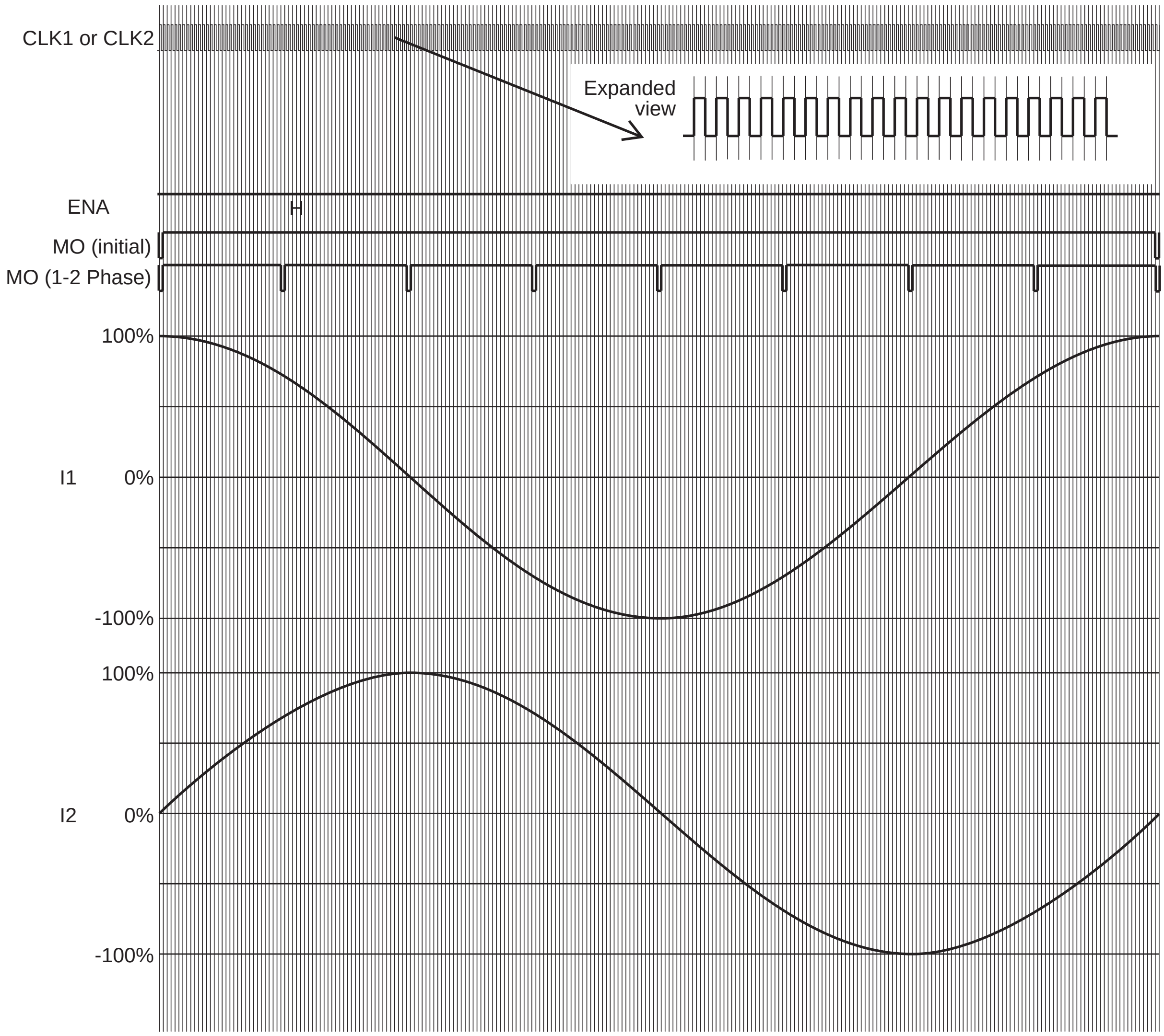


[2 Phase Excitation Timing Chart]





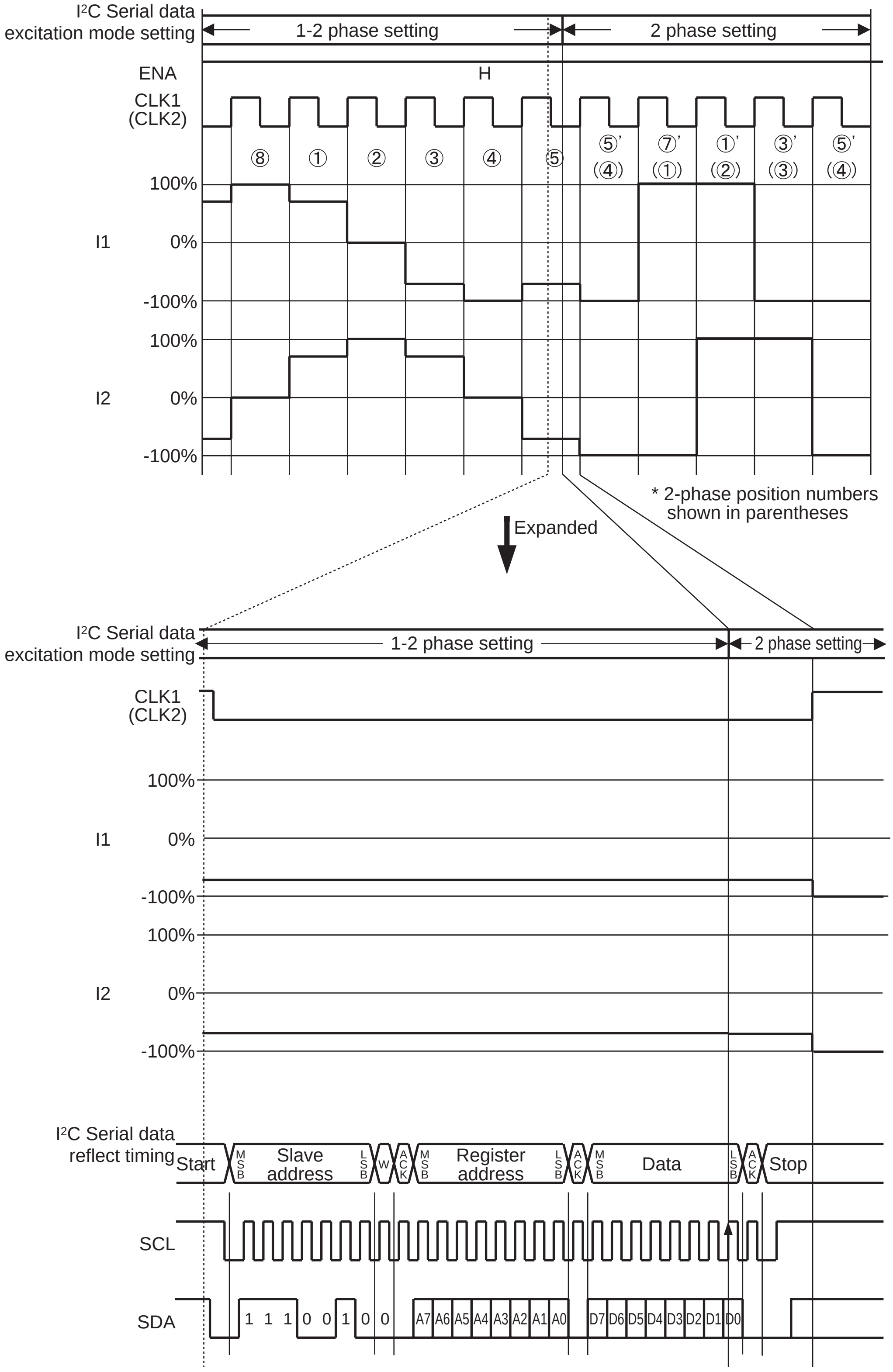
[Micro-step (16W1-2 Phase Excitation) Timing Chart]



5. Switching the excitation mode during operation

The timing at which the results of switching the excitation mode during operation are reflected and the position established after each excitation mode has been switched are as shown below.

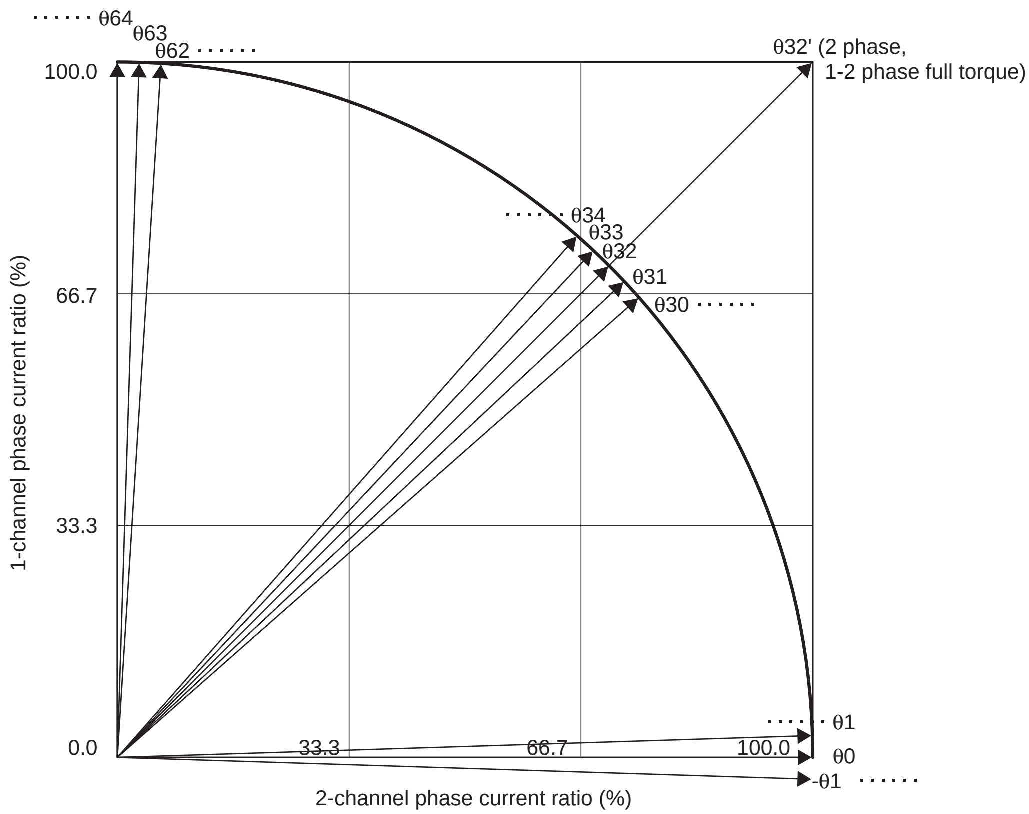
[Timing at which the results of switching the excitation mode setting are reflected (from 1-2 phase to 2-phase)]
The excitation mode switching is set at the rising edge of SCLK (8th bit of SCLK) of "D0" and the setting is reflected starting with the next CLK.



[Positions when switching the excitation mode setting]

(1) Switching to the micro-step mode

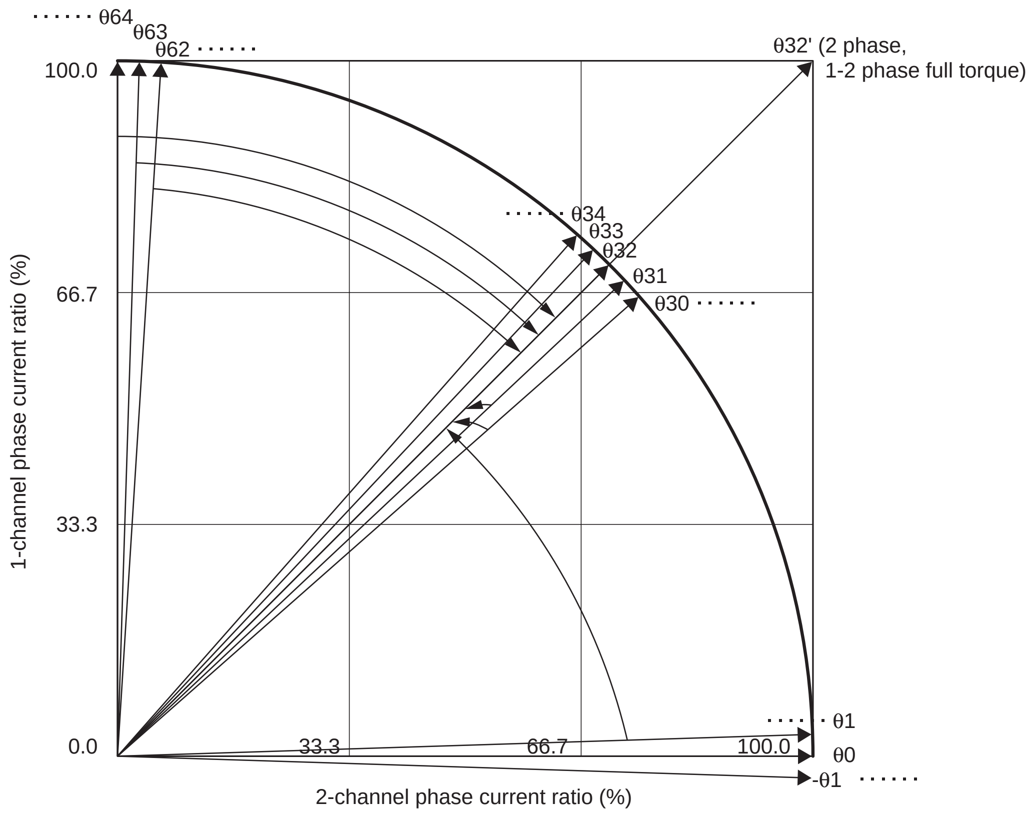
When operation has been switched from each excitation mode to the micro-step mode, excitation position proceeds to the next micro step position by the first pulse generated after the switching.



Before switching the excitation mode		Step position after the excitation mode is switched
Excitation mode	Position	256 divisions Micro-step
Micro-step	θ64	
	θ63 to θ33	
	θ32	
	θ31 to θ1	
	θ0	
1-2 phase	θ64	θ63
	θ32	θ31
	θ0	-θ1
1-2 phase full torque	θ64	θ63
	θ32’	θ31
	θ0	-θ1
2 phase	θ32’	θ31

(2) Switching to the 1-2 phase excitation (1-2 phase excitation full torque) mode
When operation has been switched from excitation mode to the 1-2 phase excitation (1-2 phase excitation full torque) mode, excitation position proceeds to position θ32 (θ32’) by the first pulse generated after the switching, and then operation transfers to the 1-2 phase excitation (1-2 phase excitation full torque) mode.
However, if the position established before the excitation mode switching is θ32 (θ32’), excitation position proceeds to the next position in the 1-2 phase excitation (1-2 phase excitation full torque) mode by the first pulse generated after the switching.

(3) Switching to the 2-phase excitation mode
If, in the case of channel 1 to channel 4, operation has been switched from each excitation mode to the 2-phase excitation mode, excitation position proceeds to position θ32’ by the first pulse generated after the switching, and then to the next position in the 2-phase excitation mode.



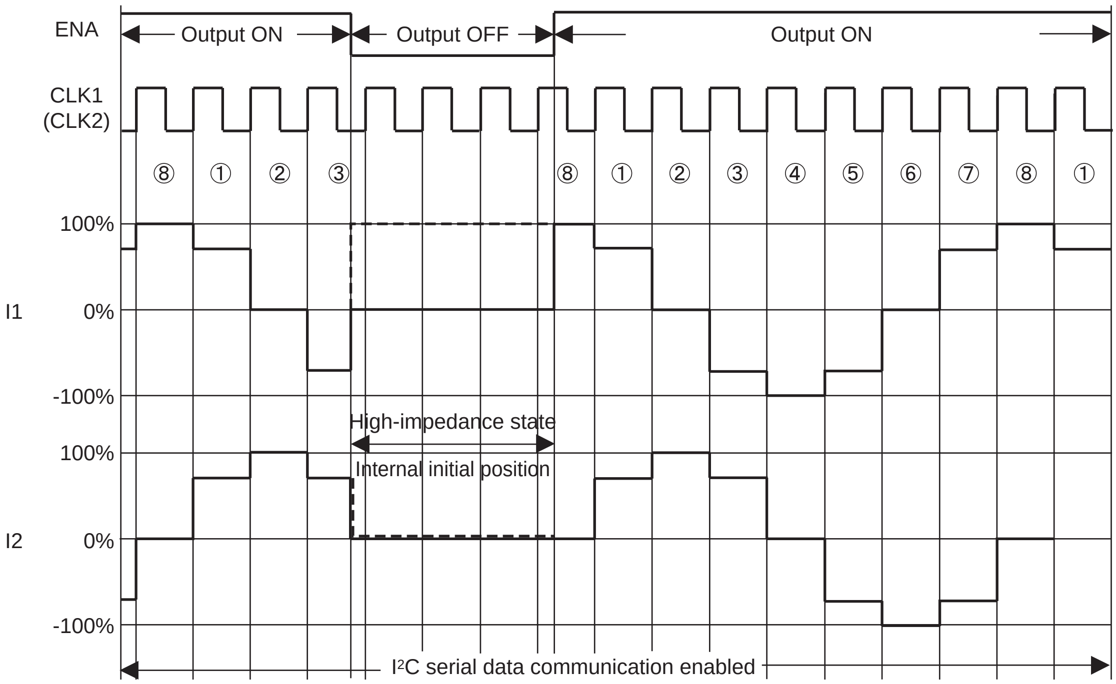
Before switching the excitation mode		Step position after the excitation mode is switched		
Excitation mode	Position	1-2 phase	1-2 phase full torque	2 phase
Micro-step	θ64	θ32	θ32’	θ32’
	θ63 to θ33	θ32	θ32’	θ32’
	θ32	θ0	θ0	θ32’
	θ31 to θ1	θ32	θ32’	θ32’
	θ0	-θ32’	-θ32’	-θ32’
1-2 phase	θ64		θ32’	θ32’
	θ32		θ0	θ32’
	θ0		-θ32’	-θ32’
1-2 phase full torque	θ64	θ32		θ32’
	θ32’	θ0		θ32’
	θ0	-θ32		-θ32’
2 phase	θ32’	θ0	θ0(θ0)	

6. ENA pin function and I^{2}C serial data output enable setting

[ENA pin]

V_{CC} consumption current during standby can be reduced to virtually zero by setting the ENA input pin to low. Furthermore, when this pin is set to low, the output becomes OFF state (high-impedance), and the state of the internal logic circuit is set to the initial excitation position (initial position).

By setting the ENA pin to high, the output becomes ON state, and the circuit operates from the initial excitation position.



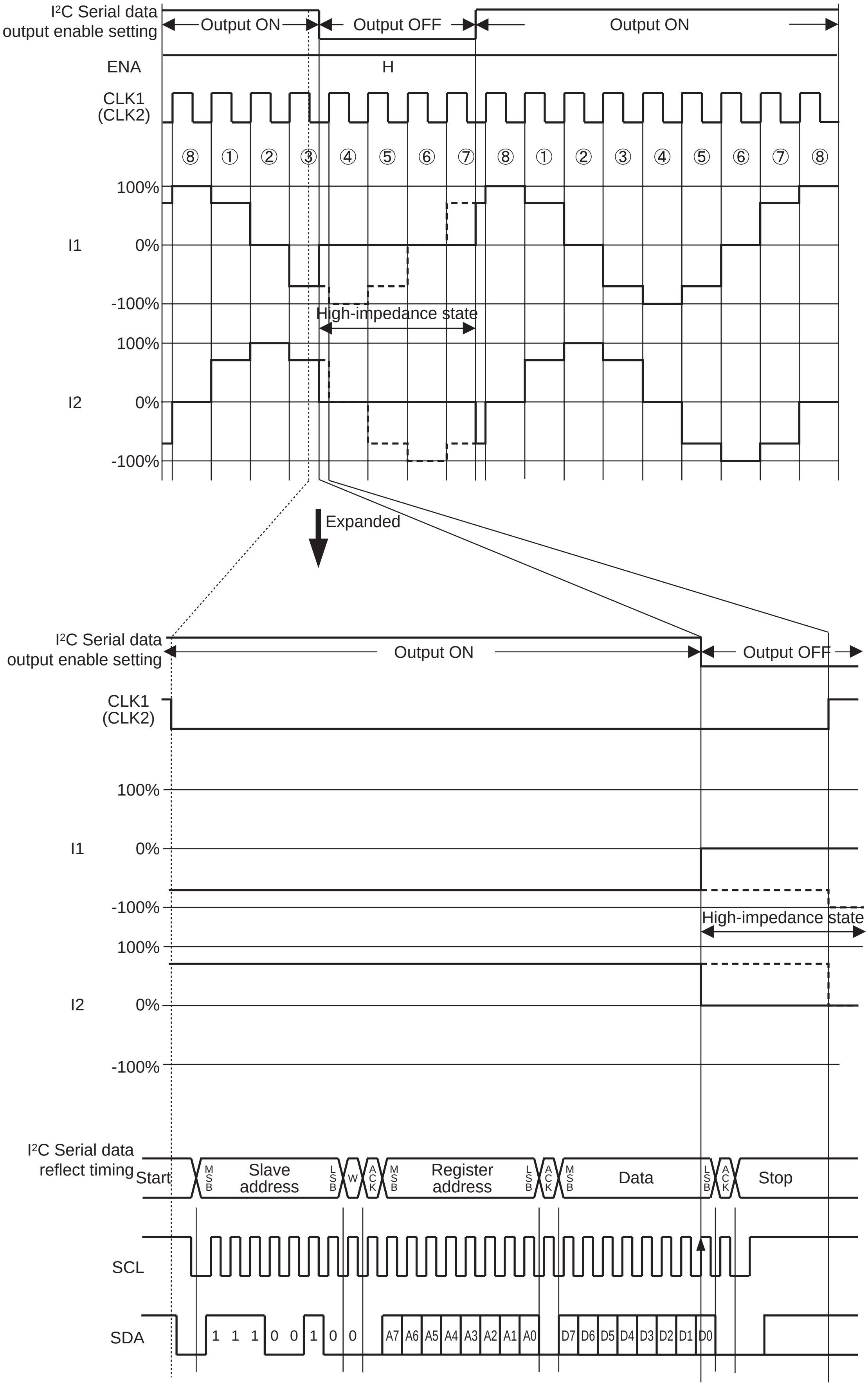
* The output does not operate unless “output enable” is set to the “output ON” state using an I^{2}C serial data communication.

[I^{2}C serial data output enable setting]

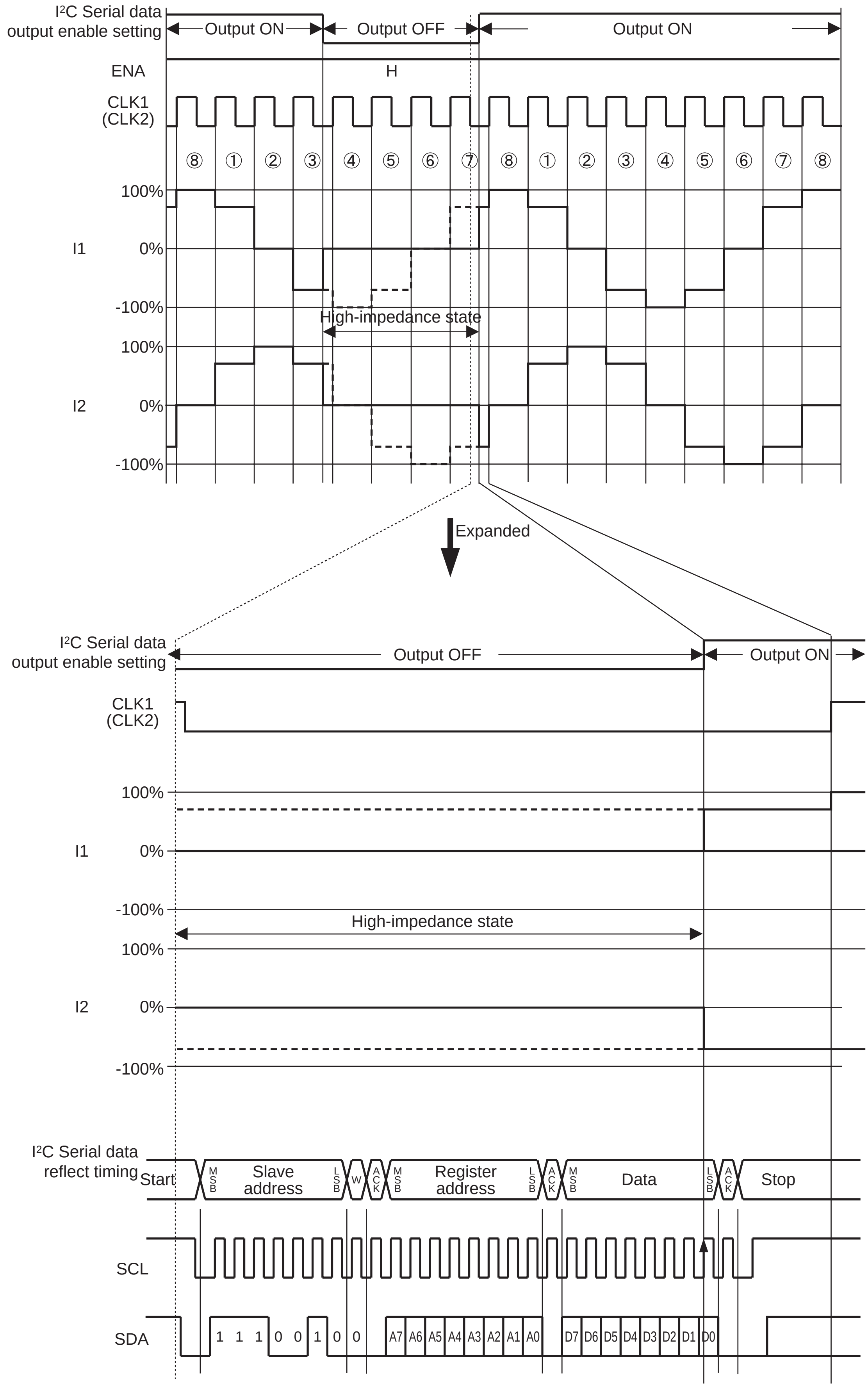
When “output enable” is set to the “output OFF” state, the output is placed in the high-impedance state at the rising edge of the 8th SCL bit in the data transmission.

However, since the internal logic circuit is activated, the position number advances if CLK has been input. This means that when “output enable” is set to the “output ON” state after this, the output is set to ON at the rising edge of the 8th SCL bit in the data transmission, and that the output level at this time will be the level at the number to which the position has advanced by the CLK input.

[Timing at which the output enable setting is reflected (output OFF)]
The output enable setting is reflected at the rising edge of SCLK (8th bit of SCLK) of “D0”



[Timing at which the output enable setting is reflected (output ON)]



7. FR pin function and I^{2}C serial data excitation direction setting

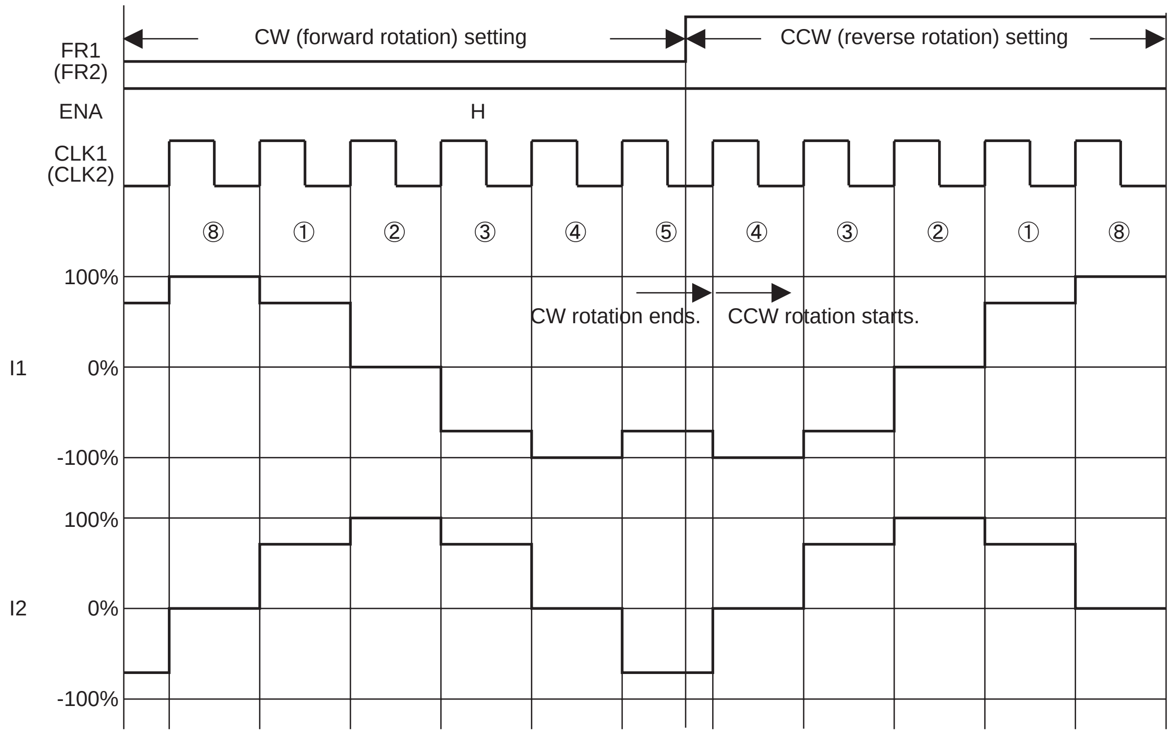
[FR pin]

Using the FR1 (FR2) forward/reverse rotation setting signal input pin, it is possible to switch the excitation direction between forward and reverse rotation.

When FR is set to low, the clockwise (CW: forward rotation) direction is set; conversely, when it is set to high, the counterclockwise (CCW: reverse rotation) direction is set.

In CW (forward rotation) mode, the channel 2 (channel 4) current phase is delayed by 90° relative to the channel 1 (channel 3) current.

In CCW (reverse rotation) mode, the channel 2 (channel 4) current phase is advanced by 90° relative to the channel 1 (channel 3) current.



[I^{2}C serial data excitation direction setting]

When the excitation (rotation) direction of the stepping motor is determined using the “excitation direction” setting, the output is switched to forward or reverse rotation at the rising edge of the 8th bit of SCL in the data transmission.

In CW (forward rotation) mode, the channel 2 (channel 4) current phase is delayed by 90° relative to the channel 1 (channel 3) current.

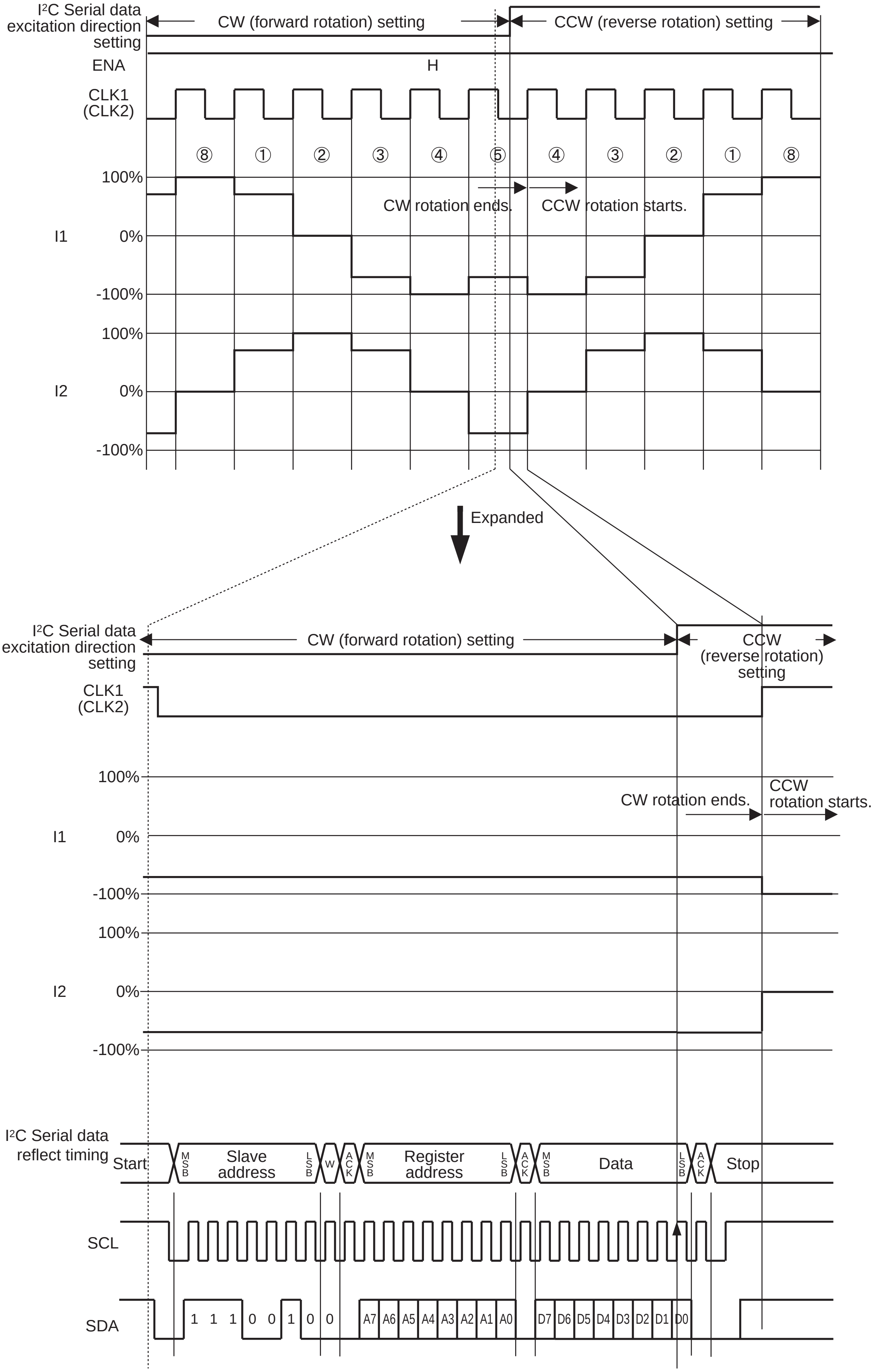
In CCW (reverse rotation) mode, the channel 2 (channel 4) current phase is advanced by 90° relative to the channel 1 (channel 3) current.

* Since the FR1 (FR2) forward/reverse signal input pins are provided with an internal pull-down resistor, these pins are set to the low state when they are open. Furthermore, when these pins are set to low, the excitation direction setting established using an I^{2}C serial data communication takes priority. Conversely, when they are set to high, the excitation direction is always set to “reverse rotation” regardless of the I^{2}C communication setting.

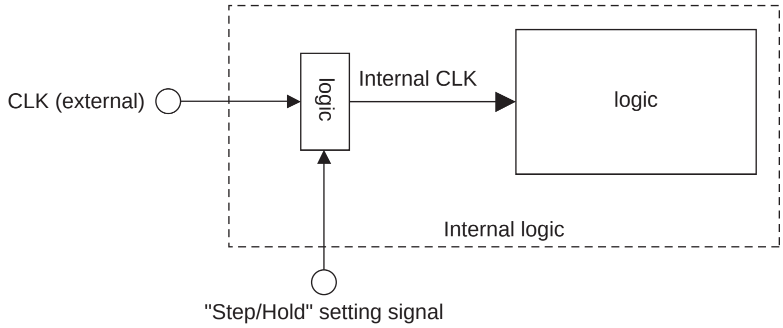
FR pin	I^{2}C excitation direction setting	Output
L	CCW (reverse rotation)	reverse rotation direction
H	CCW (reverse rotation)	reverse rotation direction
L	CW (forward rotation)	forward rotation direction
H	CW (forward rotation)	reverse rotation direction

[Timing at which excitation direction setting is reflected (CW to CCW)]

The excitation direction is set at the rising edge of SCLK (8th bit of SCLK) of “D0” and the setting is reflected starting with the next CLK.



8. I²C serial data Step/Hold setting

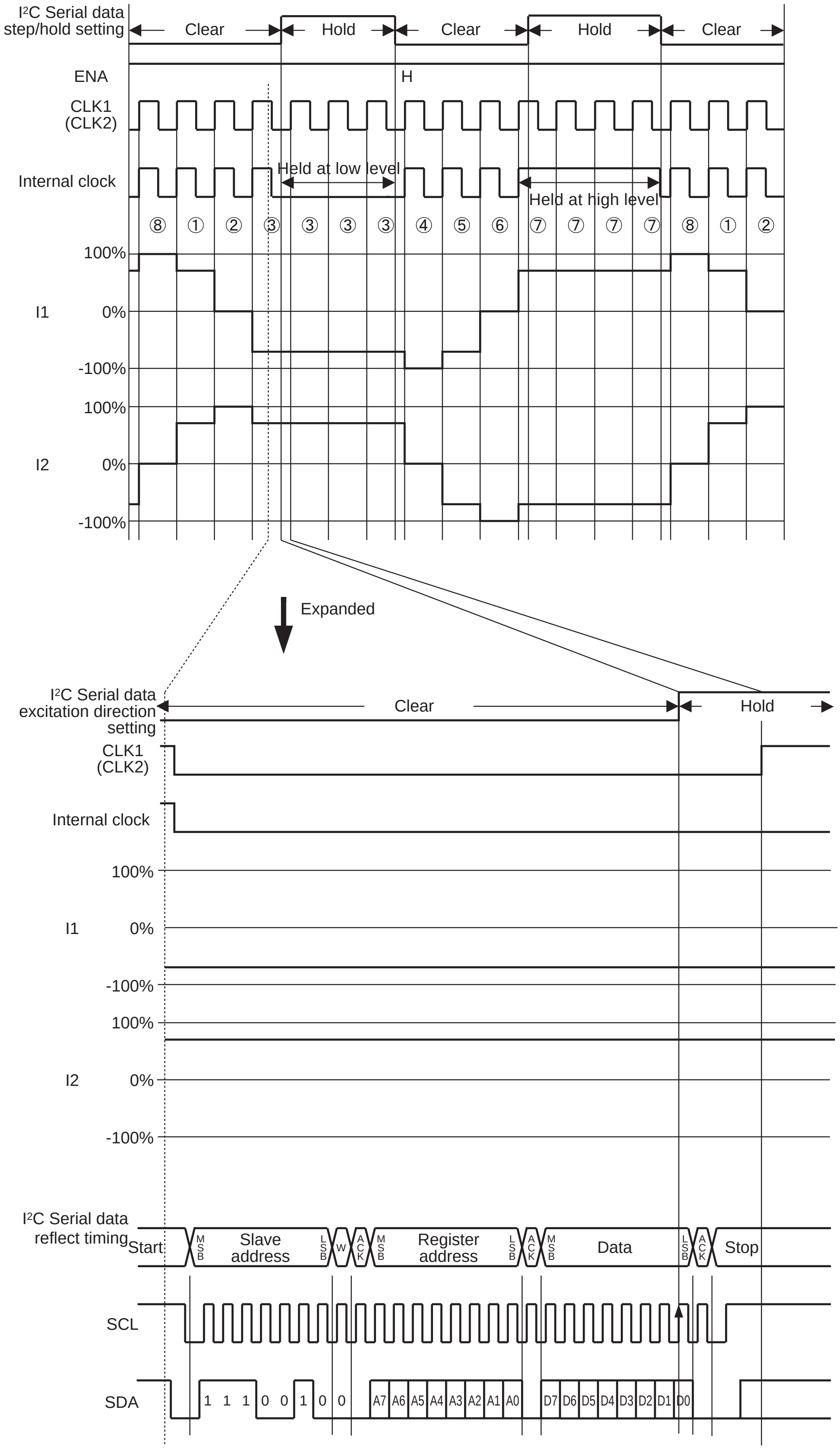


When the Step/Hold data is set to the Hold state, the state of the external clock signal (CLK) at that time is latched and held as the internal clock signal.

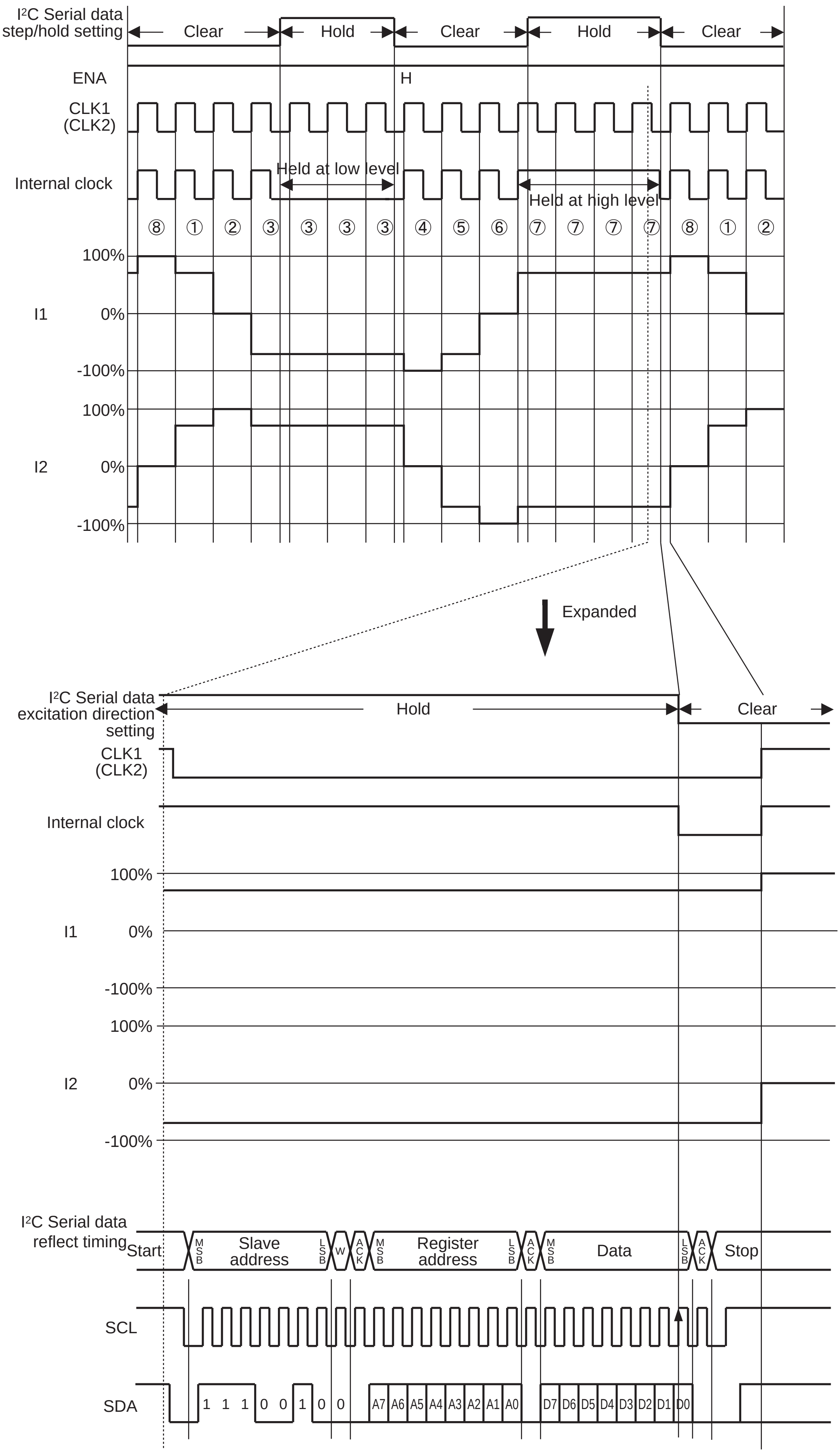
Since the state of CLK (external) is low at the timing when step/hold is set for the first time as shown in the figure on the next page, the internal CLK is held in the low state. In contrast, at the timing with which Step/Hold is set to the Hold state for the second time, the internal clock signal will be held at the high level because the external clock (CLK) was at the high level.

When Step/Hold is set to the Clear state, the internal clock is synchronized with the external clock (CLK). The output holds the state it was in at the point Step/Hold is set to the Hold state, and advances on the next clock signal rising edge after Step/Hold is set to the Clear state.
As long as Step/Hold is in the Hold state, the position number does not advance even if an external clock (CLK) signal is applied.

[Timing at which the step/hold setting is reflected (Clear to Hold)]
The step/hold setting is reflected at the rising edge of SCLK (8th bit of SCLK) of “D0”



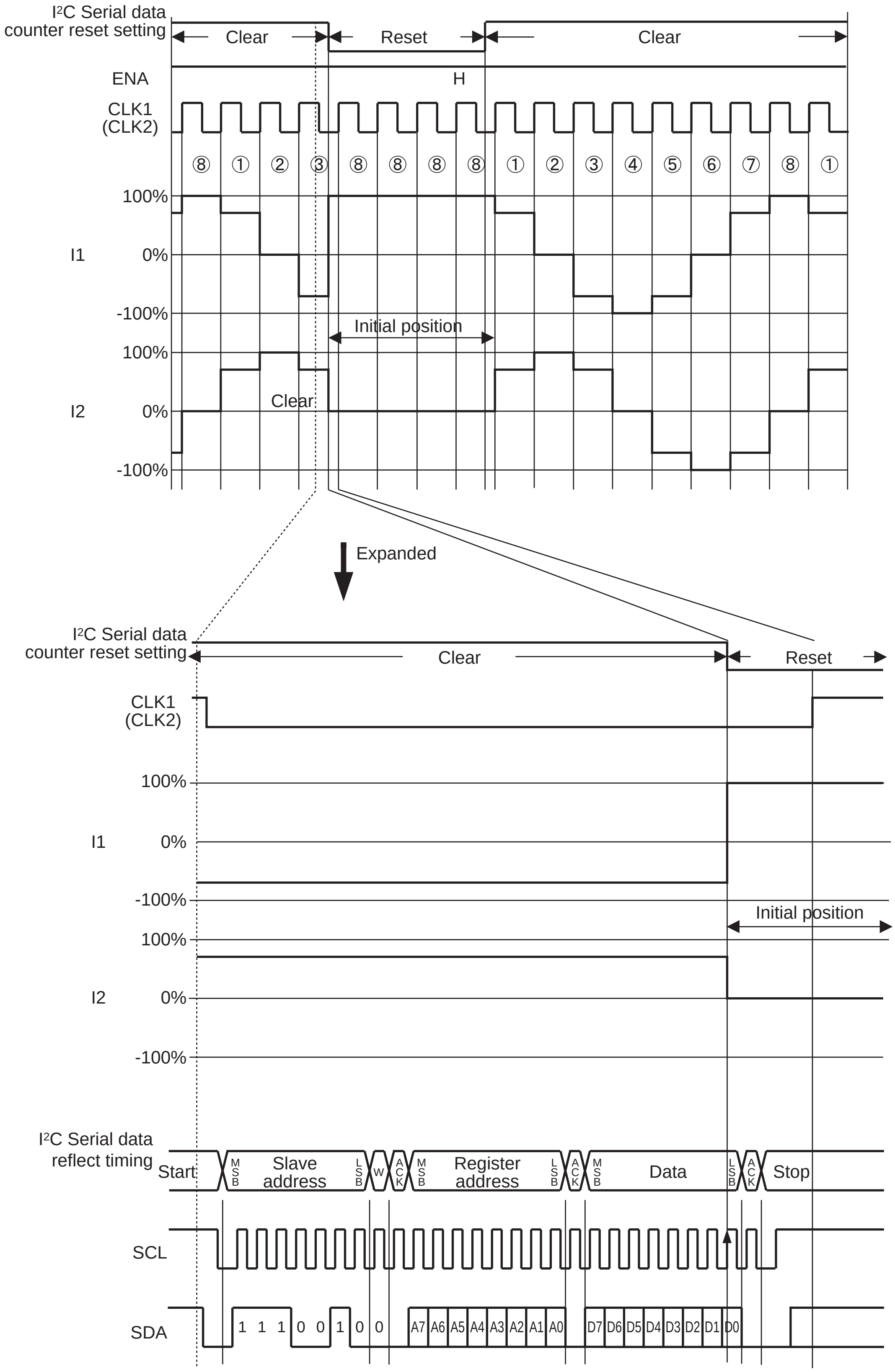
[Timing at which the step/hold setting is reflected (Hold to Clear)]



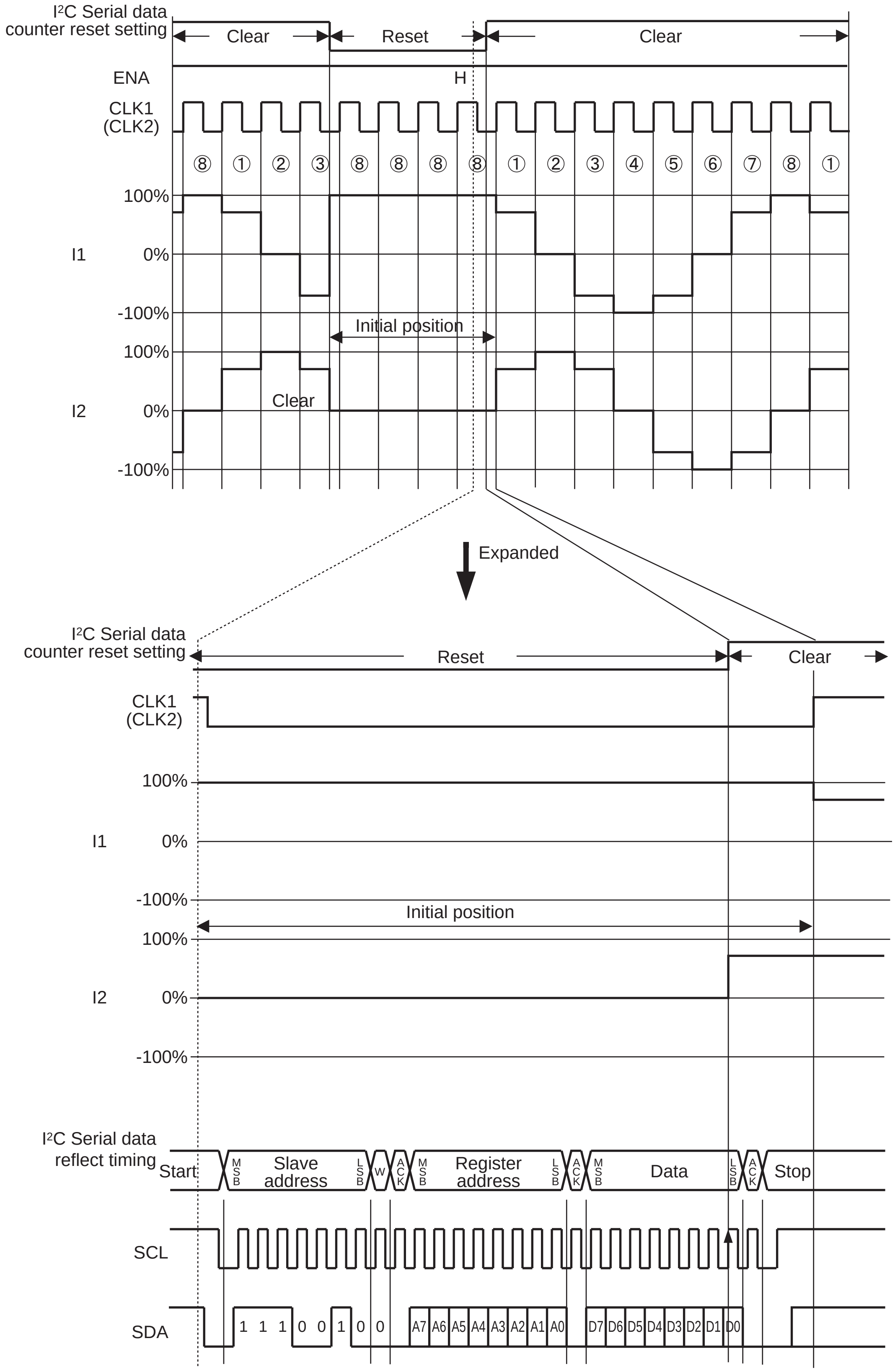
9. I²C serial data counter reset setting

When “counter reset” setting is set to the “reset” state, the output is set to the default state (initial position) at the rising edge of the 8th SCL bit in the data transmission. When “counter reset” setting is then set to the “release” state, the position number of the output advances from the rising edge of the CLK signal following the rising edge of the 8th SCL bit in the data transmission.

[Timing at which the counter reset setting is reflected (Clear to Reset)]
The counter reset setting is reflected at the rising edge of SCLK (8th bit of SCLK) of “D0”



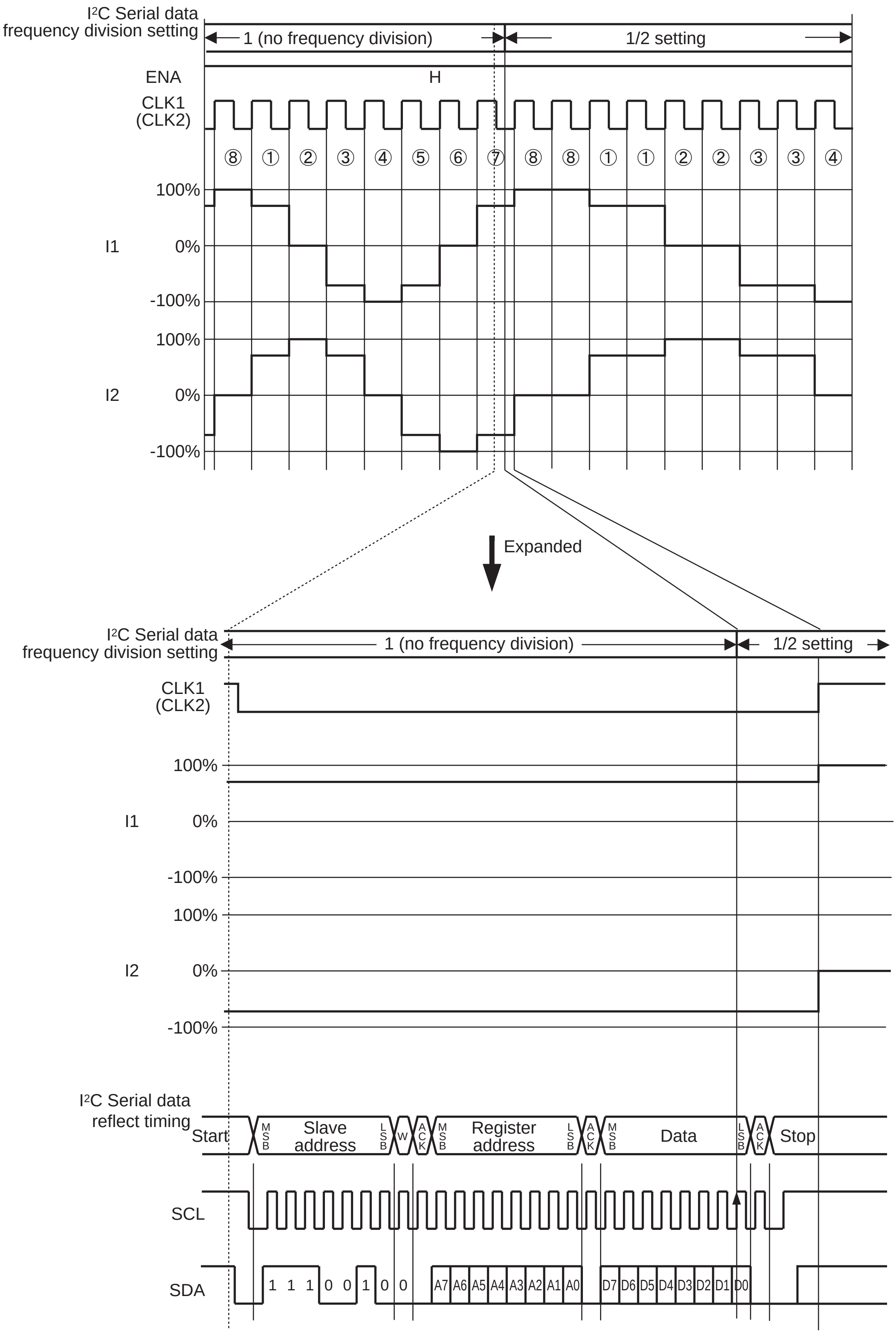
[Timing at which the counter reset setting is reflected (Reset to Clear)]



10. Number of divisions (I²C serial data frequency division setting)

Since this IC provides 256-division (16W1-2 phase) micro-step drive, a 32kHz excitation step signal is required when driving a stepping motor at 1kHz if 1-2 phase excitation is to be used.
I²C communication allows one of four ratios, namely, 1 (no frequency division), 1/2, 1/4, or 1/8 to be selected as the CLK frequency division ratio, so the motor speed can be set.

[Timing at which CLK frequency division setting is reflected]
The CLK frequency division is set at the rising edge of SCLK (8th bit of SCLK) of "D0" and the setting is reflected starting with the next CLK.



11. Output current reference voltage

I^2C communication allows the voltage to be switched to one of 16 steps from 0.200V to 0.050V. This is effective for reducing power consumption when stepping motor holding current is supplied.
The output current is determined from the internal reference voltage and the resistance value connected between the current-sense resistor connection pin (RF) and GND.
The formula used to calculate the output current is given below.

(Output constant current) = (Constant current reference voltage) ÷ (RF resistance value)

Example: With a 0.200V internal reference voltage, 1.0Ω RF resistance and 100% current ratio
Iout = 0.2V × 100% ÷ 1.0Ω = 200mA

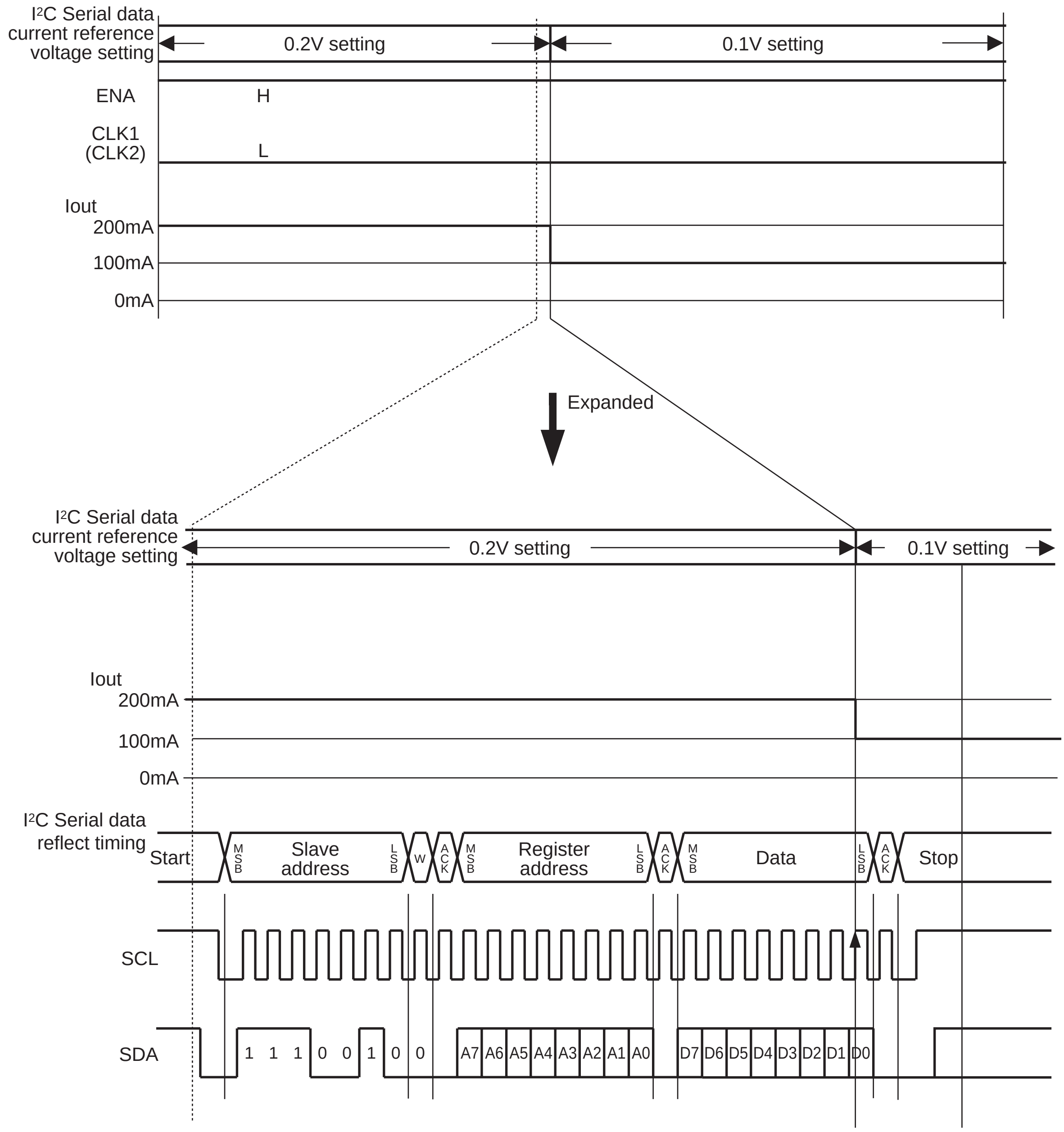
Output current reference voltage values for 1/2 channels and 3/4 channels are set as shown below.

1/2 channels setting
Register address (A7 = “0”, A6 = “0”, A5 = “0”, A4 = “0”, A3 = “0”, A2 = “0”, A1 = “0”, A0 = “0”)
3/4 channels setting
Register address (A7 = “0”, A6 = “0”, A5 = “0”, A4 = “0”, A3 = “0”, A2 = “0”, A1 = “0”, A0 = “1”)

D3	D2	D1	D0	Current setting reference voltage
0	0	0	0	0.200V
0	0	0	1	0.190V
0	0	1	0	0.180V
0	0	1	1	0.170V
0	1	0	0	0.160V
0	1	0	1	0.150V
0	1	1	0	0.140V
0	1	1	1	0.130V
1	0	0	0	0.120V
1	0	0	1	0.110V
1	0	1	0	0.100V
1	0	1	1	0.090V
1	1	0	0	0.080V
1	1	0	1	0.070V
1	1	1	0	0.060V
1	1	1	1	0.050V

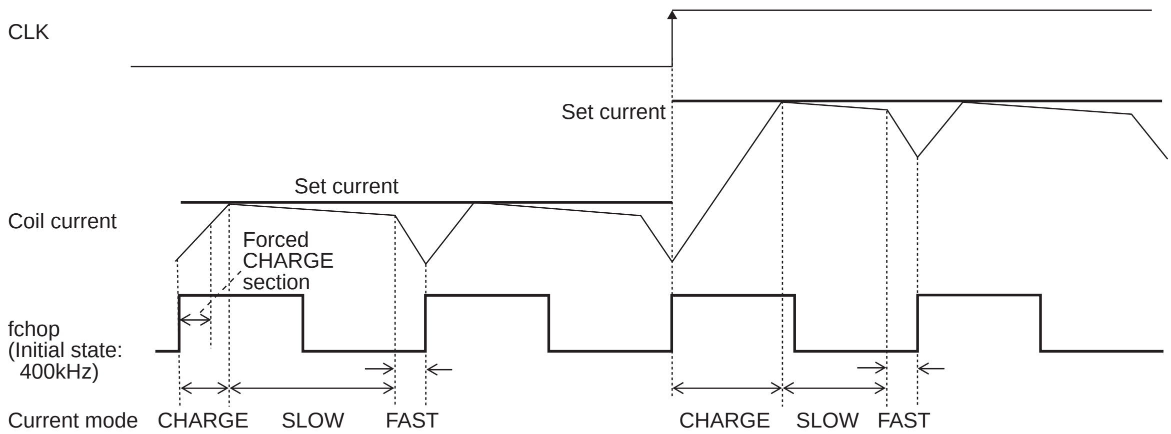
[Timing at which current setting reference voltage is reflected]
The current setting reference voltage is reflected at the rising edge of SCLK (8th bit of SCLK) of “D0”

Example: With 1.0Ω for RF and 100% current ratio

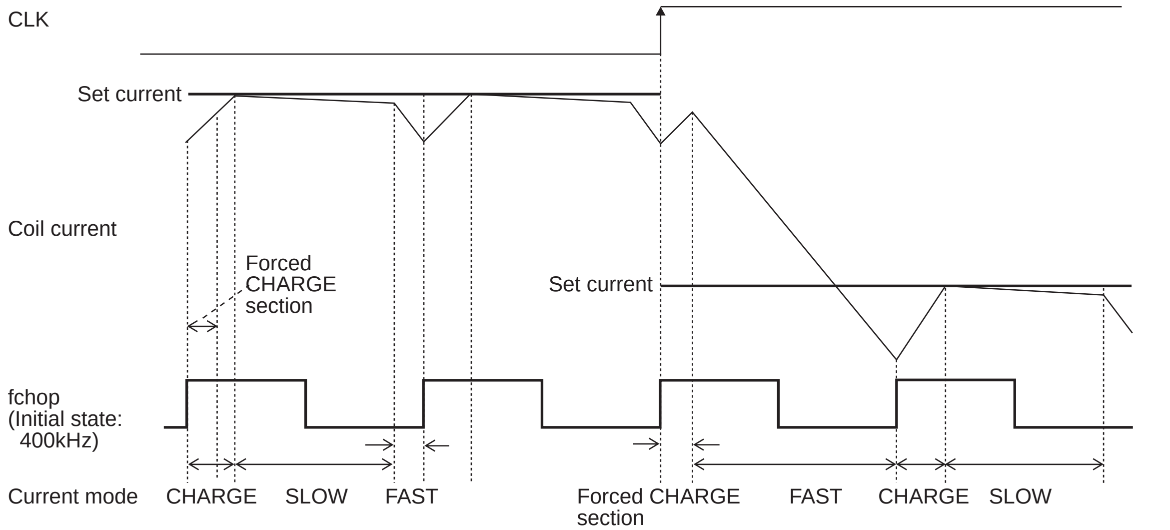


12. Current control operation specification

[Sine wave increasing direction]



[Sine wave increasing direction]



[Description of current limiting operation]
In each current mode, the operation sequence is as described below :

At rise of chopping frequency, the CHARGE mode begins.

- The coil current (ICOIL) and setting current (IREF) are compared in the forced CHARGE section.

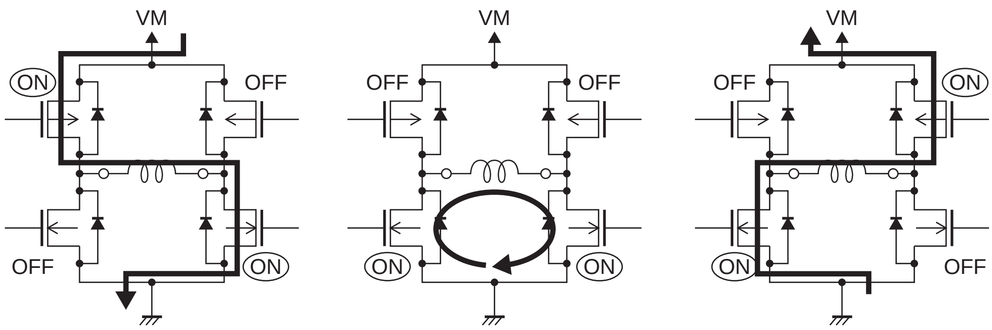
When (ICOIL < IREF) existed in the forced CHARGE section:

The CHARGE mode is established until ICOIL ≥ IREF. Then it is switched to the SLOW DECAY mode, and finally it is switched to the FAST DECAY mode.

When (ICOIL < IREF) did not exist in the forced CHARGE section:

The FAST DECAY mode begins. The coil current is attenuated in the FAST DECAY mode till one cycle of chopping is over.

Above operations are repeated. Normally, the SLOW (+FAST) DECAY mode continues in the sine wave increasing direction, then entering the FAST DECAY mode till the current is attenuated to the set level and followed by the SLOW DECAY mode.



(Charge mode) (Slow decay mode) (Fast decay mode)

[Timing at which the chopping frequency setting is reflected (400kHz to 200kHz)]
The frequency setting is reflected at the rising edge of SCLK (8th bit of SCLK) of “D0”