

MC100LVE222

3.3 V/5.0 V ECL 1:15 Differential $\div 1/\div 2$ Clock Driver

The MC100LVE222 is a low skew 1:15 differential $\div 1/\div 2$ ECL fanout buffer designed with clock distribution in mind. The LVECL/LVPECL input signal pairs can be differential or used single-ended (with V_{BB} output reference bypassed and connected to the unused input of a pair). Either of two fully differential clock inputs may be selected. Each of the four output banks of 2, 3, 4, and 6 differential pairs may be independently configured to fanout 1X or 1/2X of the input frequency. The LVE222 specifically guarantees low output to output skew. Optimal design, layout, and processing minimize skew within a device and from lot to lot.

The fsel pins and CLK_Sel pin are asynchronous control inputs. Any changes may cause indeterminate output states requiring an MR pulse to resynchronize any 1/2X outputs.

The device tpd is affected by the quantity of output pairs terminated with a minimum occurring with only one output pair and increasing about 10–20 ps for all output pairs. Relative skew distribution is not affected as more pairs are terminated, but the increased tpd does shift the entire distribution. Unused output pairs should be left unterminated (open) to reduce power and switching noise.

The MC100LVE222, as with most ECL devices, can be operated from a positive V_{CC}/V_{CCO} supply in PECL mode. This allows the LVE222 to be used for high performance clock distribution in +3.3 V systems. Operation with >3.8 V (V_{CC} or V_{CCO}) will require special thermal handling considerations. Designers can take advantage of the LVE222's performance to distribute low skew clocks across the backplane or the board. In a PECL environment series or Thevenin line terminations are typically used as they require no additional power supplies. All power supply pins must be connected. For more information on using PECL, designers should refer to Application Note AN1406/D. For a SPICE model, refer to Application Note AN1560/D.

Features

- 200 ps Part-to-Part Skew
- 50 ps Output-to-Output Skew
- Selectable 1x or 1/2x Frequency Outputs
- ESD Protection: >2 kV HBM, >200 V MM
- The 100 Series Contains Temperature Compensation
- PECL Mode Operating Range: $V_{CC}/V_{CCO} = 3.0$ V to 5.25 V with $V_{EE} = 0$ V
- NECL Mode Operating Range: $V_{CC}/V_{CCO} = 0$ V with $V_{EE} = -3.0$ V to -5.25 V
- Internal Input Pulldown Resistors
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 2
- For Additional Information, refer to Application Note AND8003/D
- Flammability Rating: UL 94 V-0 @ 0.125 in, Oxygen Index: 28 to 34
- Transistor Count = 684 devices
- Pb-Free Packages are Available*

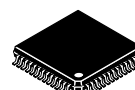
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



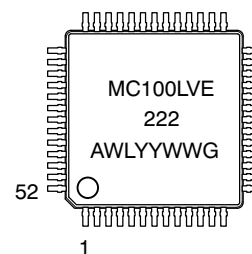
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MARKING DIAGRAM*



LQFP
FA SUFFIX
CASE 848D



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free

*For additional information, see Application Note AN1080/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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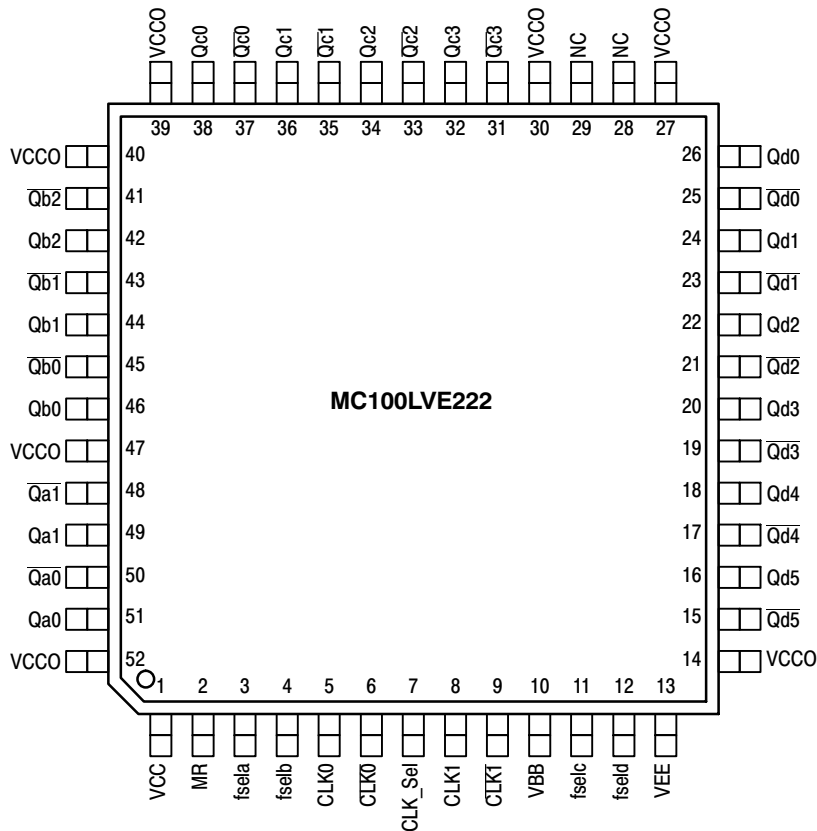


Figure 1. Pinout Assignment (Top View)

Table 1. PIN DESCRIPTION

| PIN | FUNCTION |
|----------------------------------|--|
| CLK0, $\overline{\text{CLK0}}$ | ECL Differential Input Clock |
| CLK1, $\overline{\text{CLK1}}$ | ECL Differential Input Clock |
| CLK_Sel | ECL Clock Select |
| MR | ECL Master Reset |
| Qa0:1, $\overline{\text{Qa0:1}}$ | ECL Differential Outputs |
| Qb0:2, $\overline{\text{Qb0:2}}$ | ECL Differential Outputs |
| Qc0:3, $\overline{\text{Qc0:3}}$ | ECL Differential Outputs |
| Qd0:5, $\overline{\text{Qd0:5}}$ | ECL Differential Outputs |
| fseln | ECL $\div 1$ or $\div 2$ Select |
| VBB | Reference Voltage Output |
| VCC/VCCO | Positive Supply ($V_{\text{CC}} = V_{\text{CCO}}$) |
| VEE | Negative Supply |
| NC | No Connect |

Note: All VCC/VCCO, and VEE pins must be externally connected to Power Supply to guarantee proper operation. All VCC/VCCO pins are internally interconnected.

Table 2. FUNCTION TABLE

| Input | Function | |
|---------|----------|----------|
| | L | H |
| MR | Active | Reset |
| CLK_Sel | CLK0 | CLK1 |
| fseln | $\div 1$ | $\div 2$ |

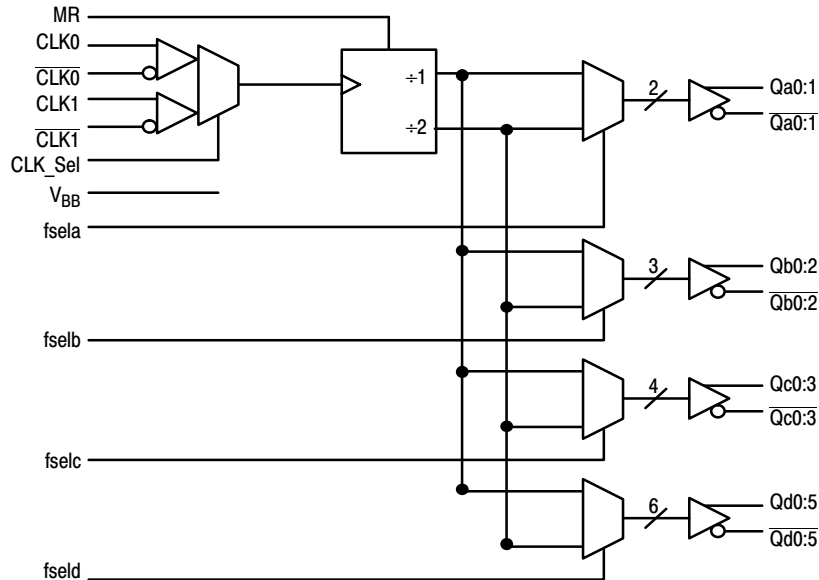


Figure 2. Logic Diagram

MC100LVE222

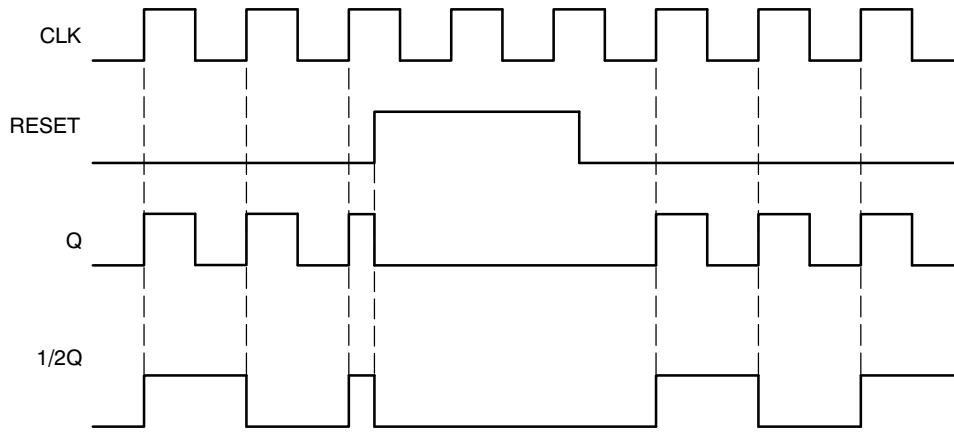


Figure 3. Timing Diagram

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|------------------|--|--|--|-------------------|--------------|
| V_{CC}/V_{CCO} | PECL Mode Power Supply | $V_{EE} = 0 \text{ V}$ | | 8 to 0 | V |
| V_{EE} | NECL Mode Power Supply | $V_{CC} \text{ or } V_{CCO} = 0 \text{ V}$ | | -8 to 0 | V |
| V_I | PECL Mode Input Voltage NECL Mode Input Voltage | $V_{EE} = 0 \text{ V}$ $V_{CC} \text{ or } V_{CCO} = 0 \text{ V}$ | $V_I \leq (V_{CC} \text{ or } V_{CCO})$ $V_I \geq V_{EE}$ | 6 to 0 -6 to 0 | V V |
| I_{out} | Output Current | Continuous Surge | | 50 100 | mA mA |
| I_{BB} | V_{BB} Sink/Source | | | ± 0.5 | mA |
| T_A | Operating Temperature Range | | | -40 to +85 | °C |
| T_{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ_{JA} | Thermal Resistance (Junction-to-Ambient) | 0 lfpm 500 lfpm | 52 LQFP 52 LQFP | 35.6 30 | °C/W °C/W |
| θ_{JC} | Thermal Resistance (Junction-to-Case) | Standard Board | 52 LQFP | 21 | °C/W |
| T_{sol} | Wave Solder | <2 to 3 sec @ 248°C | | 265 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Table 4. LVPECL DC CHARACTERISTICS V_{CC} or $V_{CCO} = 3.3$ V; $V_{EE} = 0.0$ V (Note 1)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------------|------|------|-------------|------|------|-------------|------|------|--------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 122 | 136 | | 122 | 136 | | 125 | 139 | mA |
| V_{OH} | Output HIGH Voltage (Note 2) | 2215 | 2295 | 2420 | 2275 | 2345 | 2420 | 2275 | 2345 | 2420 | mV |
| V_{OL} | Output LOW Voltage (Note 2) | 1470 | 1605 | 1745 | 1490 | 1595 | 1680 | 1490 | 1595 | 1680 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 2135 | | 2420 | 2135 | | 2420 | 2135 | | 2420 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 1490 | | 1825 | 1490 | | 1825 | 1490 | | 1825 | mV |
| V_{BB} | Output Voltage Reference | 1.92 | | 2.04 | 1.92 | | 2.04 | 1.92 | | 2.04 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6) | | | | | | | | | | |
| | $V_{PP} < 500$ mV | 1.3 | | 2.9 | 1.2 | | 2.9 | 1.2 | | 2.9 | V |
| | $V_{PP} \geq 500$ mV | 1.6 | | 2.9 | 1.5 | | 2.9 | 1.5 | | 2.9 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μ A |
| I_{IL} | Input LOW Current | | | | | | | | | | |
| | Others CLK0, CLK1 | 0.5 -300 | | | 0.5 -300 | | | 0.5 -300 | | | μ A μ A |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Input and output parameters vary 1:1 with V_{CC}/V_{CCO} . V_{EE} can vary +0.3 V to -1.95 V. Operation with $|V_{CC} \text{ or } V_{CCO} - V_{EE}| \geq 3.8$ V span will require special thermal handling considerations.
2. Outputs are terminated through a 50 Ω resistor to (V_{CC} or V_{CCO}) - 2.0 V.
3. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC}/V_{CCO} . V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to $V_{PP}(\text{min})$.

Table 5. LVNECL DC CHARACTERISTICS V_{CC} or $V_{CCO} = 0.0$ V; $V_{EE} = -3.3$ V (Note 4)

| Symbol | Characteristic | -40°C | | | 25°C | | | 85°C | | | Unit |
|-------------|--|-------------|-------|-------|-------------|-------|-------|-------------|-------|-------|--------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| I_{EE} | Power Supply Current | | 122 | 136 | | 122 | 136 | | 125 | 139 | mA |
| V_{OH} | Output HIGH Voltage (Note 5) | -1085 | -1005 | -880 | -1025 | -955 | -880 | -1025 | -955 | -880 | mV |
| V_{OL} | Output LOW Voltage (Note 5) | -1830 | -1695 | -1555 | -1810 | -1705 | -1620 | -1810 | -1705 | -1620 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1165 | | -880 | -1165 | | -880 | -1165 | | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1810 | | -1475 | -1810 | | -1475 | -1810 | | -1475 | mV |
| V_{BB} | Output Voltage Reference | -1.38 | | -1.26 | -1.38 | | -1.26 | -1.38 | | -1.26 | V |
| V_{IHCMR} | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 6) | | | | | | | | | | |
| | $V_{PP} < 500$ mV | -2.0 | | -0.4 | -2.1 | | -0.4 | -2.1 | | -0.4 | V |
| | $V_{PP} \geq 500$ mV | -1.7 | | -0.4 | -1.8 | | -0.4 | -1.8 | | -0.4 | V |
| I_{IH} | Input HIGH Current | | | 150 | | | 150 | | | 150 | μ A |
| I_{IL} | Input LOW Current | | | | | | | | | | |
| | Others CLK0, CLK1 | 0.5 -300 | | | 0.5 -300 | | | 0.5 -300 | | | μ A μ A |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input and output parameters vary 1:1 with V_{CC}/V_{CCO} . V_{EE} can vary +0.3 V to -1.95 V. Operation with $|V_{CC} \text{ or } V_{CCO} - V_{EE}| \geq 3.8$ V span will require special thermal handling considerations.
5. Outputs are terminated through a 50 Ω resistor to (V_{CC} or V_{CCO}) - 2.0 V.
6. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC}/V_{CCO} . V_{IHCMR} is defined as the range within which the V_{IH} level may vary, with the device still meeting the propagation delay specification. The V_{IL} level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to $V_{PP}(\text{min})$.

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Table 6. AC CHARACTERISTICS V_{CC} or $V_{CCO} = 3.3$ V; $V_{EE} = 0.0$ V or $V_{CC}/V_{CCO} = 0.0$ V; $V_{EE} = -3.3$ V (Note 7)

| Symbol | Characteristic | -40°C | | | 25°C | | | 70°C | | | Unit |
|------------------------|---|---------------------|----------------------|----------------------|---------------------|----------------------|----------------------|----------------------|----------------------|----------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f_{max} | Maximum Toggle Frequency | 1.2 | > 1.5 | | 1.2 | > 1.5 | | 1.2 | > 1.5 | | GHz |
| t_{PLH} t_{PHL} | Propagation Delay to Output IN (differential) (Note 8) IN (single-ended) (Note 9) MR | 1040 940 1100 | 1140 1140 1250 | 1240 1290 1400 | 1080 980 1170 | 1180 1180 1320 | 1280 1330 1470 | 1120 1020 1220 | 1220 1220 1370 | 1320 1370 1520 | ps |
| t_{skew} | Within-Device Skew (Note 10) Part-to-Part Skew (Differential Configuration) | | | 50 200 | | | 50 200 | | | 50 200 | ps |
| t_{JITTER} | Random CLOCK Jitter (RMS) | | < 1.0 | | | < 1.0 | | | < 1.0 | | ps |
| V_{PP} | Input Swing (Differential) (Note 11) | 400 | | 1000 | 400 | | 1000 | 400 | | 1000 | mV |
| t_r/t_f | Output Rise/Fall Time 20%-80% | 200 | | 600 | 200 | | 600 | 200 | | 600 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. V_{EE} can vary +0.3 V to -1.95 V. Operation with $|V_{CC}$ or $pV_{CCO}-V_{EE}| \geq 3.8$ V span will require special thermal handling considerations.
8. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals.
9. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal.
10. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
11. $V_{PP}(\min)$ is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The $V_{PP}(\min)$ is AC limited for the LVE222. A differential input as low as 50 mV will still produce full ECL levels at the output.

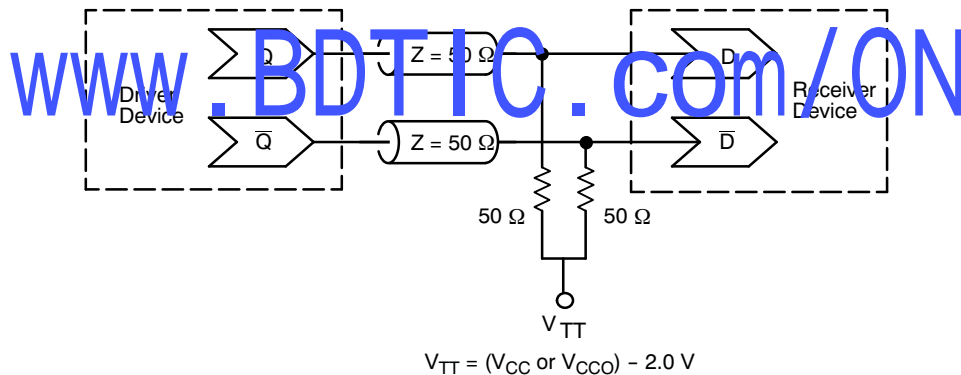


Figure 4. Typical Termination for Output Driver and Device Evaluation
(Refer to Application Note AND8020 – Termination of ECL Logic Devices)

MC100LVE222

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|------------------|----------------------|-----------------------|
| MC100LVE222FA | LQFP-52 | 160 Units / Rail |
| MC100LVE222FAG | LQFP-52 (Pb-Free) | 160 Units / Rail |
| MC100LVE222FAR2 | LQFP-52 | 1500 / Tape & Reel |
| MC100LVE222FAR2G | LQFP-52 (Pb-Free) | 1500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

- AN1404** - ECLinPS™ Circuit Performance at Non-Standard V_{IH} Levels
- AN1405** - ECL Clock Distribution Techniques
- AN1406** - Designing with PECL (ECL at +5.0 V)
- AN1503** - ECLinPS I/O SPICE Modeling Kit
- AN1504** - Metastability and the ECLinPS Family
- AN1560** - Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** - Interfacing Between LVDS and ECL
- AN1596** - ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** - Using Wire-OR Ties in ECLinPS Designs
- AN1672** - The ECL Translator Guide
- AN18001** - Odd Number Counters Design
- AN18002** - Marking and Date Codes
- AND8020** - Termination of ECL Logic Devices
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