Programmable Divide-By-N Dual 4-Bit Binary/BCD Down Counter

The MC14569B is a programmable divide-by-N dual 4-bit binary or BCD down counter constructed with MOS P-Channel and N-Channel enhancement mode devices (complementary MOS) in a monolithic structure.

This device has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

Features

- Speed-up Circuitry for Zero Detection
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Can be Cascaded With MC14526B for Frequency Synthesizer Applications
- All Outputs are Buffered
- Schmitt Triggered Clock Conditioning
- Pb–Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	–0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
PD	Power Dissipation, per Package (Note 1)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
ΤL	Lead Temperature (8–Second Soldering)	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Temperature Derating:

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Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, Vin and Vout should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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http://onsemi.com

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		MARKING DIAGRAMS
	PDIP-16 P SUFFIX CASE 648	¹⁶ ኹኹኹኹኹኹኹኸ MC14569BCP ୦ AWLYYWW 1 ₽₽₽₽₽₽₽₽
and the second	TSSOP-16 DT SUFFIX CASE 948F	16 14 569B o ALYW 1
STATE OF	SOIC-16 DW SUFFIX CASE 751G	16 A A A A A A A A A A A A A A A A A A A
A WL, YY, Y	L = Wafer I	bly Location Lot

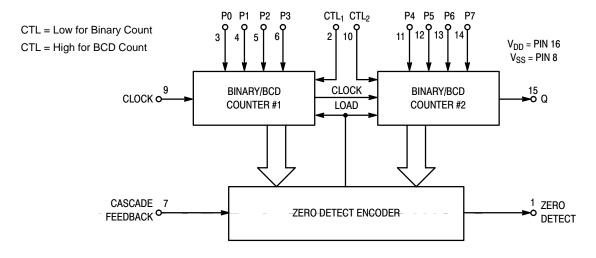
ORDERING INFORMATION

WW, W = Work Week

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

PIN	ASSI	GNME	ENT
	1•	16] V _{DD}
CTL1 [2	15]Q
P0 [3	14] P7
P1 [4	13] P6
P2 [5	12] P5
P3 [6	11] P4
	7	10] CTL ₂
v _{ss} [8	9	СГОСК

BLOCK DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping [†]
MC14569BCP	PDIP-16	500 Units / Rail
MC14569BCPG	PDIP–16 (Pb–Free)	500 Units / Rail
MC14569BDW	SOIC-16 WB	47 Units / Rail
MC14569BDWG	SOIC-16 WB (Pb-Free)	47 Units / Rail
MC14569BDWR2	SOIC-16 WB	1000 Units / Tape & Reel
MC14569BDWR2G	SOIC-16 WB (Pb-Free)	1000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS	(Voltages Referenced to V _{SS})
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				- 5	5°C		25°C		12	5°C	
Characterist	Symbol	V _{DD} Vdc	Min	Мах	Min	Typ (Note 2)	Max	Min	Мах	Unit	
Output Voltage V _{in} = V _{DD} or 0	"0" Level	V _{OL}	5.0 10 15	- - -	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
$V_{in} = 0 \text{ or } V_{DD}$	"1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15	- -	4.95 9.95 14.95	- - -	Vdc
Input Voltage $(V_O = 4.5 \text{ or } 0.5 \text{ Vdc})$ $(V_O = 9.0 \text{ or } 1.0 \text{ Vdc})$ $(V_O = 13.5 \text{ or } 1.5 \text{ Vdc})$)	V _{IL}	5.0 10 15	- - -	1.5 3.0 4.0	_ _ _	2.25 4.50 6.75	1.5 3.0 4.0	_ _ _	1.5 3.0 4.0	Vdc
$(V_O = 0.5 \text{ or } 4.5 \text{ Vdc})$ $(V_O = 1.0 \text{ or } 9.0 \text{ Vdc})$ $(V_O = 1.5 \text{ or } 13.5 \text{ Vdc})$)	V _{IH}	5.0 10 15	3.5 7.0 11	- - -	3.5 7.0 11	2.75 5.50 8.25	- -	3.5 7.0 11	- - -	Vdc
$\begin{array}{l} \text{Output Drive Current} \\ (\text{V}_{\text{OH}} = 2.5 \text{ Vdc}) \\ (\text{V}_{\text{OH}} = 4.6 \text{ Vdc}) \\ (\text{V}_{\text{OH}} = 9.5 \text{ Vdc}) \\ (\text{V}_{\text{OH}} = 13.5 \text{ Vdc}) \end{array}$	Source	Іон	5.0 5.0 10 15	- 3.0 - 0.64 - 1.6 - 4.2	- - -	- 2.4 - 0.51 - 1.3 - 3.4	- 4.2 - 0.88 - 2.25 - 8.8	- - -	- 1.7 - 0.36 - 0.9 - 2.4		mAdc
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink	I _{OL}	5.0 10 15	0.64 1.6 4.2	- - -	0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4	_ _ _	mAdc
Input Current		l _{in}	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Capacitance (V _{in} = 0)		C _{in}	_	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package)		I _{DD}	5.0 10 15	 	5.0 _10 _20		0.005 	5.0 10– 20	- - -	150 300 600	μAdc
Total Supply Current (N (Dynamic plus Quies Per Package) (C _L = 50 pF on all ou buffers switching)	scent,	Ι _Τ	5.0 10 15			$I_{T} = (1$.58 μA/kHz) .20 μA/kHz) .95 μA/kHz)	f + I _{DD} f + I _{DD}			μAdc

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at 25°C.
 To calculate total supply current at loads other than 50 pF:

 $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

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All Types V_{DD} Characteristic Symbol Unit Min Тур Max Vdc (Note 5) **Output Rise Time** 5.0 100 200 t_{TLH} _ ns 10 50 100 _ 15 40 80 _ **Output Fall Time** 5.0 100 200 ns t_{THL} _ 100 10 50 _ 15 _ 40 80 Turn-On Delay Time t_{PLH} ns Zero Detect Output 5.0 420 700 10 175 300 _ 125 250 15 _ Q Output 5.0 675 1200 ns _ 10 _ 285 500 200 400 15 _ Turn-Off Delay Time t_{PHL} ns Zero Detect Output 5.0 380 600 _ 300 10 150 _ 100 200 15 _ Q Output 5.0 530 1000 ns _ 10 _ 225 400 300 15 155 _ Clock Pulse Width 5.0 300 100 _ ns t_{WH} 10 150 45 _ 15 30 115 _ **Clock Pulse Frequency** \mathbf{f}_{cl} 5.0 _ 3.5 2.1 MHz 10 9.5 5.1 _ 15 _ 13.0 7.8 Clock Pulse Rise and Fall Time 5.0 NO LIMIT ttlh, tthl μs 10 15

SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}, T_A = 25^{\circ}C$)

5. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING WAVEFORMS

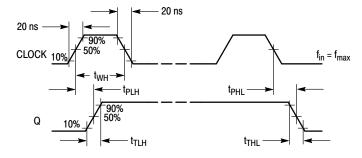
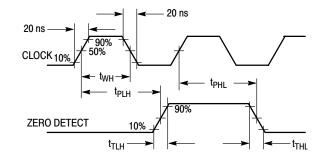


Figure 1.





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PIN DESCRIPTIONS

INPUTS

P0, P1, P2, P3 (Pins 3, 4, 5, 6) – Preset Inputs. Programmable inputs for the least significant counter. May be binary or BCD depending on the control input.

P4, P5, P6, P7 (Pins 11, 12, 13, 14) – Preset Inputs. Programmable inputs for the most significant counter. May be binary or BCD depending on the control input.

Clock (Pin 9) – Preset data is decremented by one on each positive transition of this signal.

OUTPUTS

Zero Detect (Pin 1) – This output is normally low and goes high for one clock cycle when the counter has decremented to zero.

Q (Pin 15) – Output of the last stage of the most significant counter. This output will be inactive unless the preset input P7 has been set high.

CONTROLS

Cascade Feedback (Pin 7) – This pin is normally set high. When low, loading of the preset inputs (P0 through P7) is inhibited, i.e., P0 through P7 are "don't cares." Refer to Table 1 for output characteristics.

 CTL_1 (Pin 2) – This pin controls the counting mode of the least significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

 CTL_2 (Pin 10) – This pin controls the counting mode of the most significant counter. When set high, counting mode is BCD. When set low, counting mode is binary.

SUPPLY PINS

 V_{SS} (Pin 18) – Negative Supply Voltage. This pin is usually connected to ground.

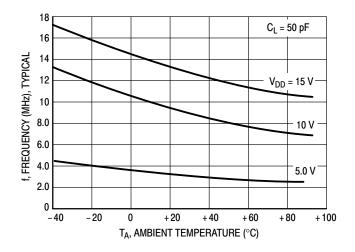
 V_{DD} (Pin 16) – Positive Supply Voltage. This pin is connected to a positive supply voltage ranging from 3.0 V to 18 V.

OPERATING CHARACTERISTICS

The MC14569B is a programmable divide–by–N dual 4–bit down counter. This counter may be programmed (i.e., preset) in BCD or binary code through inputs P0 to P7. For each counter, the counting sequence may be chosen independently by applying a high (for BCD count) or a low (for binary count) to the control inputs CTL_1 and CTL_2 .

The divide ratio N (N being the value programmed on the preset inputs P0 to P7)_is_automatically_loaded into thecounter as soon as the count 1 is detected. Therefore, a division ratio of one is not possible. After N clock cycles, one pulse appears on the Zero Detect output. (See Timing Diagram.) The Q output is the output of the last stage of the most significant counter (See Tables 1 through 5, Mode Controls.)

When cascading the MC14569B to the MC14526B, the Cascade Feedback input, Q, and Zero Detect outputs must be respectively connected to "0", Clock, and Load of the following counter. If the MC14569B is used alone, Cascade Feedback must be connected to $V_{\rm DD}$.



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Counter Co	ntrol Values	Divide Ratio			
CTL ₁	CTL ₂	Zero Detect	Q		
0	0	256	256		
0	1	160	160		
1	0	160	160		
1	1	100	100		

NOTE: Data Preset Inputs (P0–P7) are "Don't Cares" while Cascade Feedback is Low.

Table 2Mode Controls (CTL₁ = Low, CTL₂ = Low, Cascade Feedback = High)

	Preset Inputs Divid							Divide	e Ratio	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	256	256	Max Count
0	0	0	0	0	0	0	1	Х	Х	Illegal State
0	0	0	0	0	0	1	0	2	Х	Min Count
0	0	0	0	0	0	1	1	3	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
0	0	0	0	1	1	1	1	15	Х	
0	0	0	1	0	0	0	0	16	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
0	0	1	0	0	0	0	0	32	Х	
•	•	•	•	•	•	•	•	•	х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	х	
0	1	_ 0	0	_0	0	0	_ 0	_ 64	X	_
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
0	1	1	1	1	1	1	1	127	Х	
1	0	0	0	0	0	0	0	128	128	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	0	1	0	0	0	136	136	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	Ļ
1	1	1	1	1	1	1	1	255	255	Ť
27	2 ⁶	2 ⁵	24	2 ³	2 ²	2 ¹	20			
128	64	32	16	8	4	2	1			Bit Value
	Coun Bin	ter #2 ary			Count Bin					Counting Sequence

X = No Output (Always Low)

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X = No Output (Always Low)

			Preset	Inputs				Divide	Ratio	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	160	160	Max Count
0	0	0	0	0	0	0	1	х	Х	Illegal State
0	0	0	0	0	0	1	0	2	Х	Min Count
0	0	0	0	0	0	1	1	3	х	
•	•	•	•	•	•	•	•	•	Х	
				•		•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	0	0	0	1	0	0	1	9	X	
0	0	0	1	0	0	0	0	10	X	
•	•	•		•	•	•	•	•	X	
•		•	•	•	•	•	•	•	X	
									X	
•	•	•	•	•	•	•	•	• 19	X	
0	0	1	0	0	0	0	0	20	X	
-									X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•		
•	•	•	•	•	•	•	•	•	X	
0	0	1	1	0	0	0	0	30	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
0	1	0	0	0	0	0	0	40	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
0	1	0	1	0	0	0	0	50	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	- •	- •	-•	- •	-•	- •	- •	X	—
0	1	1	0	0	0	0	0	60	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
0	1	1	1	0	0	0	0	70	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
1	0	0	0	0	0	0	0	80	80	Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
•		•		•	•	•	•	•	•	
•			•			•		•	•	
					•	•				
•	1	1	•	0	0	•	•	• 150	• 150	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•		•	•	•	•	•	•	•	•	↓
1	1	1	1	1	0	0	1	159	159	•
80	40	20	10	8	4	2	1			Bit Value
	Coun	ter #2		1	Coun	ter #1				Counting
		ary			BC					Sequence
1				1	50			1		004-01100

 Table 3Mode Controls (CTL1 = High, CTL2 = Low, Cascade Feedback = High)

	Ratio	Divide				Values	Preset					
Comments	Q	Zero Detect	P0	P1	P2	P3	P4	P5	P6	P7		
Max Count	160	160	0	0	0	0	0	0	0	0		
Illegal State	Х	Х	1	0	0	0	0	0	0	0		
Min Count	х	2	0	1	0	0	0	0	0	0		
	Х	3	1	1	0	0	0	0	0	0		
	Х	•	•	•	•	•	•	•	•	•		
	Х	•	•	•	•	•	•	•	•	•		
	Х	•	•	•	•	•	•	•	•	•		
	Х	15	1	1	1	1	0	0	0	0		
	Х	16	0	0	0	0	1	0	0	0		
	Х	•	•	•	•	•	•	•	•	•		
	Х	•	•	•	•	•	•	•	•	•		
	Х	•	•	•	•	•	•	•	•	•		
	Х	31	1	1	1	1	1	0	0	0		
	Х	32	0	0	0	0	0	1	0	0		
	Х	•	•	•	•	•	•	•	•	•		
	Х	•	•	•	•	•	•	•	•	•		
	Х	•	•	•	•	•	•	•	•	•		
	Х	48	0	0	0	0	1	1	0	0		
	•	•	•	•	•	•	•	•	•	•		
	•	•	•	•	•	•	•	•	•	•		
	•	•	•	•	•	•	•	•	•	•		
	Х	64	0	0	0	0	0	0	1	0		
	•	•	•	•	•	•	•	•	•	•		
	•	•	•	•	•	•	•	•	•	•		
	•	•	•	•	•	•	•	•	•	•		
	Х	80	0	0	0	0	1	0	1	0		
	•	•	•	•	•	•	•	•	•	•		
	•	•	•	•	•	•	•	•	•	•		
	— - • X	-•	- • — 0	-• 0	•	-• 0	- • 1	-•	• 1	• 0		
										0		
	•	•	•	•	•	•	•	•	•	•		
	•		•	•	•	•	•	•		•		
Q Output Active	128	128	0	0	0	0	0	0	0	•		
	.20	.20	•	•	•	•	•	•	•			
	•	•	•	•	•	•	•	•	•	•		
	•	•	•	•	•	•	•	•	•	•		
	144	144	0	0	0	0	1	0	0	1		
	•	•	•	•	•	•	•	•	•	•		
	•	•	•	•	•	•	•	•	•	•		
	•	•	•	•	•	•	•	•	•	•		
↓	159	159	1	1	1	1	1	0	0	1		
			2 ⁰	2 ¹	2 ²	2 ³	24	2 ⁵	2 ⁶	27		
Bit Value			1	2	4	8	_ 16	32	_ 64	128		
Counting					Count				Count			
Sequence					Bin				BC			

X = No Output (Always Low)

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			Preset	Values				Divide	Ratio	
P7	P6	P5	P4	P3	P2	P1	P0	Zero Detect	Q	Comments
0	0	0	0	0	0	0	0	100	100	Max Count
0	0	0	0	0	0	0	1	Х	Х	illegal state
0	0	0	0	0	0	1	0	2	Х	Min Count
0	0	0	0	0	0	1	1	3	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
0	0	0	0	1	0	0	1	9	Х	
0	0	0	1	0	0	0	0	10	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
0	0	1	1	0	0	0	0	30	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
0	1	0	0	0	0	0	0	40	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
0	1	0	1	0	0	0	0	50	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	Х	
0	1	1	1	0	0	0	0	70	X	
•	•	•	•	•	•	•	•	•	Х	
•	•	•	•	•	•	•	•	•	X	
•	•	•	•	•	•	•	•	•	X	
1	0	- 0	- 0	-0	- 0	-0	_ 0	– 80 –		— Q Output Active
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
1	0	0	1	0	0	0	0	90	90	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	•	•	
•	•	•	•	•	•	•	•	• 99	• 99	↓
-		-						33	33	Dit Malua
80	40	20	10	8	4	2	1			Bit Value
		ter #2			Count					Counting
	BC	CD			BC	D				Sequence

TIMING DIAGRAM MC14569B

7

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8

6

9

10

11

15

13

16

CLOCK

DIVIDE BY 2 DIVIDE

BY 3

DIVIDE BY 4 DIVIDE BY 12

ZERO

DETECT OUTPUT

5

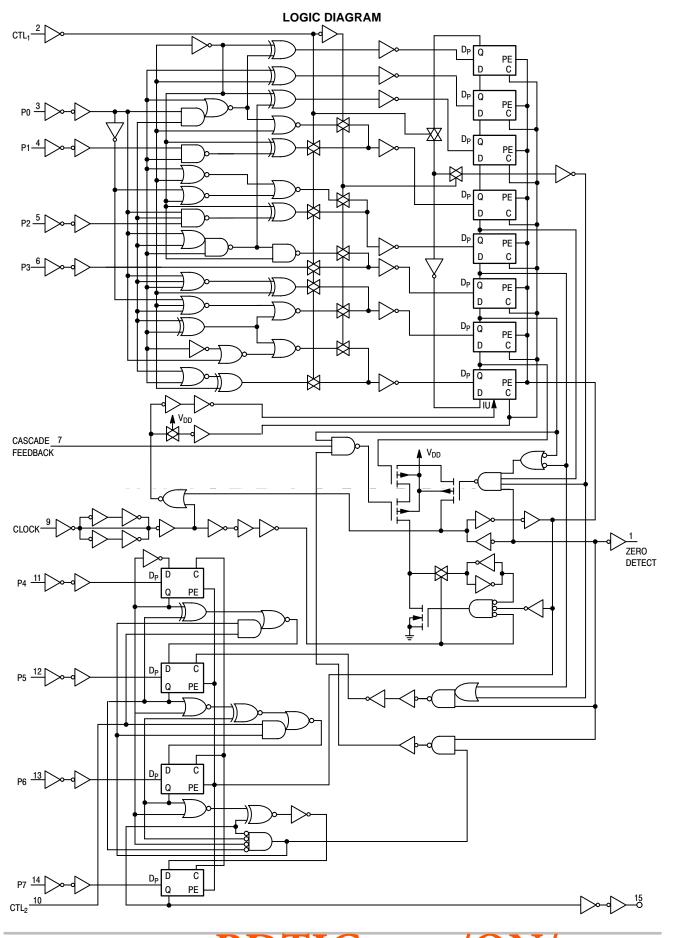
X = No Output (Always Low)

2

WWW.

B

3



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TYPICAL APPLICATIONS

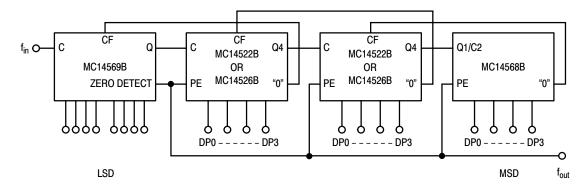


Figure 3. Cascading MC14568B and MC14522B or MC14526B with MC14569B

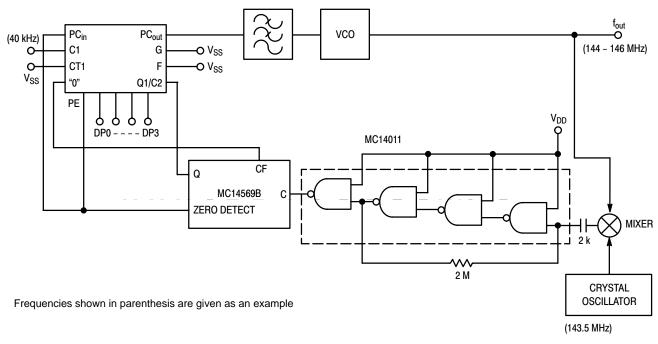
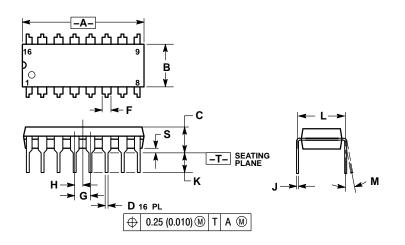


Figure 4. Frequency Synthesizer with MC14568B and MC14569B Using a Mixer (Channel Spacing 10 kHz)

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PACKAGE DIMENSIONS

PDIP-16 **P SUFFIX** PLASTIC DIP PACKAGE CASE 648-08 ISSUE T

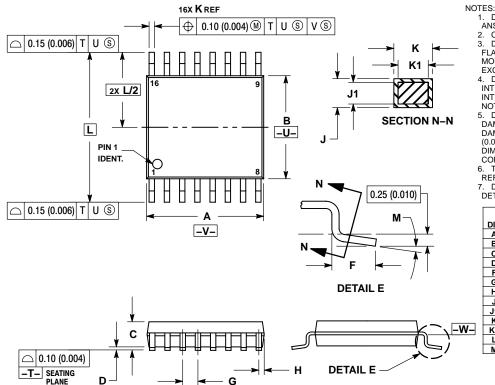


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 1.
- CONTROLLING DIMENSION: INCH. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL. 2.
- 3.
- 4. DIMENSION B DOES NOT INCLUDE
- MOLD FLASH. 5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.740	0.770	18.80	19.55
В	0.250	0.270	6.35	6.85
С	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
н	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
κ	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
М	0 °	10 °	0 °	10 °
S	0.020	0.040	0.51	1.01

TSSOP-16 DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948F-01 **ISSUE A**



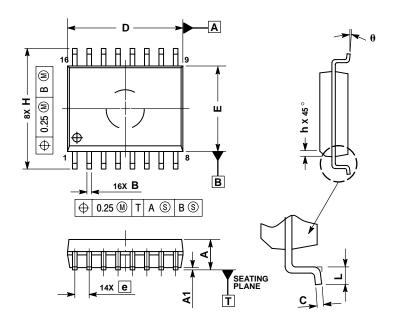
- DIESC
 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EVOLUTION AND REPORTS SHALL NOT
- MOLD FLASH OK GATE BOKKS SHALL NOT EXCEED 0.15 (0.006) PER SIDE. 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL
- CONDITION. CONDITION.
 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INCHES	
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
в	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
Н	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
 κ	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
М	0 °	8 °	0 °	8 °

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PACKAGE DIMENSIONS

SOIC-16 WB **DW SUFFIX** PLASTIC SOIC PACKAGE CASE 751G-03 **ISSUE C**



NOTES:

- NOTES: 1. DIMENSIONS ARE IN MILLIMETERS. 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994. 3. DIMENSIONS D AND E DO NOT INLCUDE MOLD PROTRUSION. 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE. 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		
DIM	MIN	MAX	
Α	2.35	2.65	
A1	0.10	0.25	
в	0.35	0.49	
С	0.23	0.32	
D	10.15	10.45	
E	7.40	7.60	
е	1.27 BSC		
Н	10.05	10.55	
h	0.25	0.75	
L	0.50	0.90	
q	0 °	7 °	

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