Octal D-Type Latch with 3-State Outputs

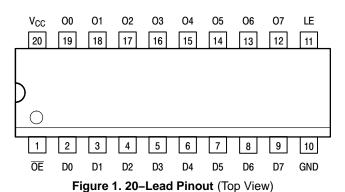
With 5 V-Tolerant Inputs

The MC74LVX573 is an advanced high speed CMOS octal latch with 3-state outputs. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

This 8-bit D-type latch is controlled by a latch enable input and an output enable input. When the output enable input is high, the eight outputs are in a high impedance state.

Features

- High Speed: $t_{PD} = 6.4 \text{ ns}$ (Typ) at $V_{CC} = 3.3 \text{ V}$
- Low Power Dissipation: $I_{CC} = 4 \mu A$ (Max) at $T_A = 25^{\circ}C$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: $V_{OLP} = 0.8 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model > 2000 V; Machine Model > 200 V
- Pb-Free Packages are Available*



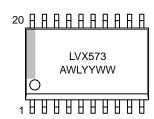


http://onsemi.com

MARKING DIAGRAMS



SOIC-20 DW SUFFIX CASE 751D





TSSOP-20 DT SUFFIX CASE 948E





SOEIAJ-20 M SUFFIX CASE 967



A = Assembly Location

WL, L = Wafer Lot Y, YY = Year

W, WW = Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

^{*}For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

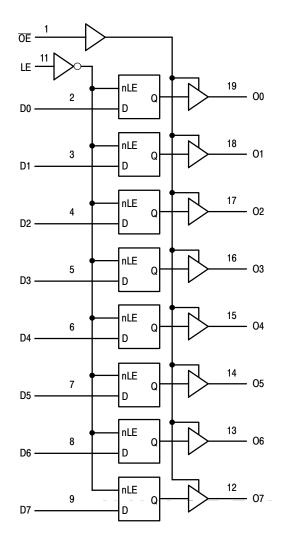


Table 1. PIN NAMES

Pins	Function
OE	Output Enable Input
LE	Latch Enable Input
D0-D7	Data Inputs
O0-O7	3–State Latch Outputs

I	INPUTS		INPUTS OUTPUTS		OUTPUTS	
OE	LE	Dn	On	OPERATING MODE		
L	H	H L	H L	Transparent (Latch Disabled); Read Latch		
L	L L	h I	H L	Latched (Latch Enabled) Read Latch		
L	L	Х	NC	Hold; Read Latch		
Н	L	Х	Z	Hold; Disabled Outputs		
H H	H	H L	Z Z	Transparent (Latch Disabled); Disabled Outputs		
H	L L	h I	Z Z	Latched (Latch Enabled); Disabled Outputs		

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Latch Enable High—to—Low Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Latch Enable High—to—Low Transition; NC = No Change, State Prior to the Latch Enable High—to—Low Transition; X = High or Low Voltage Level or Transitions are Acceptable; Z = High Impedance State; For I_{CC} Reasons DO NOT FLOAT Inputs.

Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{in}	DC Input Voltage	-0.5 to +7.0	V
V _{out}	DC Output Voltage	-0.5 to V _{CC} +0.5	V
I _{IK}	Input Diode Current	-20	mA
I _{OK}	Output Diode Current	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±75	mA
P _D	Power Dissipation	180	mW
T _{stg}	Storage Temperature	-65 to +150	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	3.6	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-40	+85	°C
Δt/ΔV	Input Rise and Fall Time	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

			v _{cc}	Т	A = 25°	С	T _A = - 40 to 85°C		
Symbol	Parameter	Test Conditions	v	Min	Тур	Max	Min	Max	Unit
V _{IH}	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V _{IL}	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V _{OH}	High-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	$I_{OH} = -50 \mu A$ $I_{OH} = -50 \mu A$ $I_{OH} = -4 \text{ mA}$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V _{OL}	Low-Level Output Voltage (V _{in} = V _{IH} or V _{IL})	$I_{OL} = 50 \mu A$ $I_{OL} = 50 \mu A$ $I_{OL} = 4 \text{ mA}$	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I _{in}	Input Leakage Current	V _{in} = 5.5 V or GND	3.6			±0.1		±1.0	μΑ
l _{OZ}	Maximum 3–State Leakage Current	$V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or GND}$	3.6			±0.2 5		±2.5	μΑ
Icc	Quiescent Supply Current	$V_{in} = V_{CC} \text{ or } GND$	3.6	_		4.0		40.0	μΑ

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ns}$)

				Т	A = 25°	С	T _A = - 40 to 85°C		
Symbol	Parameter	Test Condit	tions	Min	Тур	Max	Min	Max	Unit
t _{PLH} ,	Propagation Delay LE to O	V _{CC} = 2.7 V	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		8.2 10.7	15.6 19.1	1.0 1.0	18.5 22.0	ns
		$V_{CC} = 3.3 \pm 0.3 \text{ V}$	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		6.4 8.9	10.1 13.6	1.0 1.0	12.0 15.5	
t _{PLH} ,	Propagation Delay D to O	V _{CC} = 2.7 V	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		7.6 10.1	14.5 18.0	1.0 1.0	17.5 21.0	ns
		$V_{CC} = 3.3 \pm 0.3 \text{ V}$	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		5.9 8.4	9.3 12.8	1.0 1.0	11.0 14.5	
t _{PZL} , t _{PZH}	Output Enable Time OE to O	$V_{CC} = 2.7 \text{ V}$ $R_L = 1 \text{ k}\Omega$	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		7.8 10.3	15.0 18.5	1.0 1.0	18.5 22.0	ns
		$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $R_L = 1 \text{ k}\Omega$	$C_L = 15 \text{ pF}$ $C_L = 50 \text{ pF}$		6.1 8.6	9.7 13.2	1.0 1.0	12.0 15.5	
t _{PLZ} , t _{PHZ}	Output Disable Time OE to O	$V_{CC} = 2.7 \text{ V}$ $R_L = 1 \text{ k}\Omega$	C _L = 50 pF		12.1	19.1	1.0	22.0	ns
		$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $R_L = 1 \text{ k}\Omega$	C _L = 50 pF		10.1	13.6	1.0	15.5	
toshl toslh	Output-to-Output Skew (Note 1)	$V_{CC} = 2.7 \text{ V}$ $V_{CC} = 3.3 \pm 0.3 \text{ V}$	$C_L = 50 \text{ pF}$ $C_L = 50 \text{ pF}$			1.5 1.5		1.5 1.5	ns

^{1.} Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

		T _A = 25°C		T _A = - 40 to 85°C			
Symbol	Parameter	Min	Тур	Max	Min	Max	Unit
C _{in}	Input Capacitance		4	10		10	pF
C _{out}	Maximum 3-State Output Capacitance		6				pF
C _{PD}	Power Dissipation Capacitance (Note 2)		29				pF

C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
 Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/8 (per latch). C_{PD} is used to determine the no–load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V, Measured in SOIC Package)

		T _A = 25°C		
Symbol	Characteristic	Тур	Max	Unit
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.5	0.8	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.5	-0.8	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V

TIMING REQUIREMENTS (Input $t_r = t_f = 3.0 \text{ ns}$)

			T _A = 25°C		T _A = - 40 to 85°C	
Symbol	Parameter	Test Conditions	Тур	Limit	Limit	Unit
t _{w(h)}	Minimum Pulse Width, LE	V _{CC} = 2.7 V V _{CC} = 3.3 ± 0.3 V		6.5 5.0	7.5 5.0	ns
t _{su}	Minimum Setup Time, D to LE	$V_{CC} = 2.7 \text{ V}$ $V_{CC} = 3.3 \pm 0.3 \text{ V}$		5.0 3.5	5.0 3.5	ns
t _h	Minimum Hold Time, D to LE	V _{CC} = 2.7 V V _{CC} = 3.3 ± 0.3 V		1.5 1.5	1.5 1.5	ns

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LVX573DWR2	SOIC-20	1000 / Tape & Reel
MC74LVX573DWR2G	SOIC-20 (Pb-Free)	1000 / Tape & Reel
MC74LVX573DT	TSSOP-20*	75 Units / Rail
MC74LVX573DTR2	TSSOP-20*	2500 / Tape & Reel
MC74LVX573M	SOEIAJ-20	50 Units / Rail
MC74LVX573MG	SOEIAJ-20 (Pb-Free)	50 Units / Rail
MC74LVX573MEL	SOEIAJ-20	2000 / Tape & Reel
MC74LVX573MELG	SOEIAJ-20 (Pb-Free)	2000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*This package is inherently Pb–Free.

SWITCHING WAVEFORMS

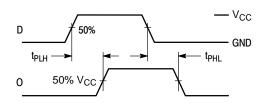


Figure 3.

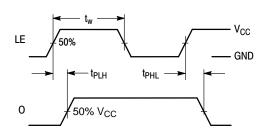


Figure 4.

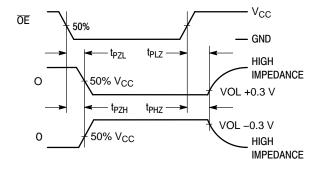


Figure 5.

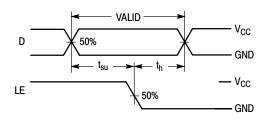
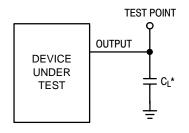


Figure 6.

TEST CIRCUITS



*Includes all probe and jig capacitance

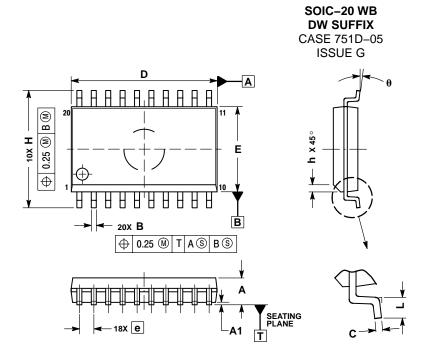
 $\begin{array}{c|c} & \text{TEST POINT} \\ \hline \\ \text{DEVICE} \\ \text{UNDER} \\ \text{TEST} \end{array} \begin{array}{c} \text{OUTPUT} & \text{1 k$}\Omega \\ \\ \text{$I$ L}\Omega \\ \\ \text{C_L}^{\star} \end{array} \begin{array}{c} \text{CONNECT TO V_{CC} WHEN TESTING t_{PLZ} AND t_{PZL}.} \\ \text{CONNECT TO GND WHEN TESTING t_{PHZ} AND t_{PZH}.} \\ \hline \\ \end{array}$

*Includes all probe and jig capacitance

Figure 7. Propagation Delay Test Circuit

Figure 8. 3-State Test Circuit

PACKAGE DIMENSIONS

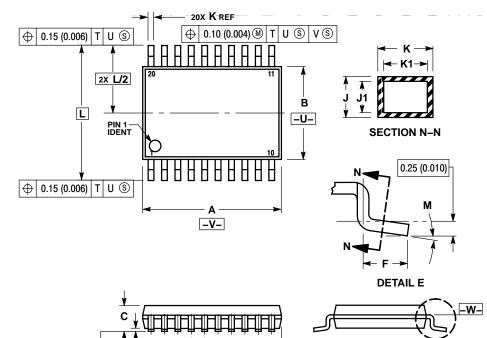


NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS. 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD
 - PROTRUSION.
 MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
- DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS					
DIM	MIN MAX					
Α	2.35	2.65				
A1	0.10	0.25				
В	0.35	0.49				
С	0.23	0.32				
D	12.65	12.95				
Ε	7.40	7.60				
е	1.27	BSC				
Н	10.05	10.55				
h	0.25	0.75				
L	0.50	0.90				
A	0 °	7 °				





<u>0.100 (0.004)</u> -T- SEATING PLANE

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION:
 MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE
 MOLD FLASH, PROTRUSIONS OR GATE
 BURRS. MOLD FLASH OR GATE BURRS
 SHALL NOT EXCEED 0.15 (0.006) PER
- 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER
- SIDE.

 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K
 DIMENSION AT MAXIMUM MATERIAL
- CONDITION.

 5. TERMINAL NUMBERS ARE SHOWN
- FOR REFERENCE ONLY.

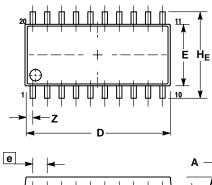
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	6.40	6.60	0.252	0.260	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
Н	0.27	0.37	0.011	0.015	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BSC		
M	0°	8°	0°	8°	

DETAIL E

PACKAGE DIMENSIONS

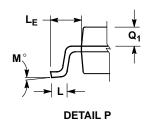
SOEIAJ-20 **M SUFFIX** CASE 967-01 **ISSUE O**

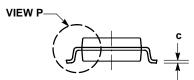


⊕ 0.13 (0.005) M



0.10 (0.004)





NOTES:

- OTES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.

 4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

()				
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
С	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
Е	5.10	5.45	0.201	0.215
е	1.27 BSC		0.050 BSC	
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0 °	10°	0 °	10°
Q_1	0.70	0.90	0.028	0.035
Z		0.81		0.032

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