Quad Bus Buffer

with 3-State Control Inputs

The MC74VHC125 is a high speed CMOS quad bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC125 requires the 3-state control input (\overline{OE}) to be set High to place the output into the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.

- High Speed: $t_{PD} = 3.8$ ns (Typ) at $V_{CC} = 5$ V
- Low Power Dissipation: $I_{CC} = 4 \mu A$ (Max) at $T_A = 25$ °C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 5.5 V Operating Range
- Low Noise: $V_{OLP} = 0.8 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: Human Body Model; > 2000 V, Machine Model; > 200 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- These devices are available in Pb-free package(s). Specifications herein
 apply to both standard and Pb-free devices. Please see our website at
 www.onsemi.com for specific Pb-free orderable part numbers, or
 contact your local ON Semiconductor sales office or representative.



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14-LEAD SOIC D SUFFIX CASE 751A 14-LEAD TSSOP DT SUFFIX CASE 948G



14-LEAD SOIC EIAJ M SUFFIX CASE 965

PIN CONNECTION AND MARKING DIAGRAM

(Top View)

OE1	1 ●	14	v _{cc}
A1 [2	13	OE4
Y1 🛭	3	12	A4
<u> </u>	4	11] Y4
A2 [5	10	0E3
Y2 [6	9] A3
GND [7	8] Y3
			J

DEVICE MARKING INFORMATION

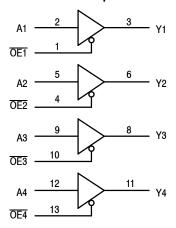
See general marking information in the device marking section on page 6 of this data sheet.

ORDERING INFORMATION

Device	Package	Shipping	
MC74VHC125D	SOIC	55 Units/Rail	
MC74VHC125DT	TSSOP	96 Units/Rail	
MC74VHC125M	SOIC EIAJ	50 Units/Rail	

LOGIC DIAGRAM

Active-Low Output Enables



FUNCTION TABLE

VHC125						
Inp	outs	Output				
Α	ΟE	Υ				
Н	L	Н				
L	L	L				
Х	Н	Z				

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _{in}	DC Input Voltage	_0.5 to_+7.0_	V
V _{out}	DC Output Voltage	-0.5 to V _{CC} +0.5	V
I _{IK}	Input Diode Current	- 20	mA
lok	Output Diode Current	± 20	mA
l _{out}	DC Output Current, per Pin	± 25	mA
Icc	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T _{stg}	Storage Temperature	-65 to +150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq $(V_{in}$ or $V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{in}	DC Input Voltage	0	5.5	V
V _{out}	DC Output Voltage	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time $ V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V} $ $ V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V} $	0	100 20	ns/V

^{**} Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

[†]Derating - SOIC Packages: - 7 mW/°C from 65° to 125°C TSSOP Package: - 6.1 mW/°C from 65° to 125°C

DC ELECTRICAL CHARACTERISTICS

			Vcc	1	T _A = 25°C		T _A ≤	85°C	T _A ≤	125°C	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V _{IH}	Minimum High-Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V _{IL}	Maximum Low-Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	V
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} = V_{IH}$ or V_{IL} $I_{OH} = -4$ mA $I_{OH} = -8$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		V
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50 \mu\text{A}$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	V
I _{OZ}	Maximum 3-State Leakage Current	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{OUT} = V_{CC} \text{ or GND}$	5.5			± 0.2 5		±2.5		±2.5	μΑ
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5V or GND	0 to 5.5			± 0.1		±1.0		±1.0	μΑ
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			4.0		40		40	μΑ

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ ns}$)

				т	A = 25°	С	T _A = s	≤ 85°C		= ≤ 5°C	
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Min	Max	Unit
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to Y	$V_{CC} = 3.3 \pm 0.3V$	C _L = 15 pF C _L = 50 pF		5.6 8.1	8.0 11.5	1.0 1.0	9.5 13.0	1.0 1.0	12.0 16.0	ns
		$V_{CC} = 5.0 \pm 0.5V$	C _L = 15 pF C _L = 50 pF		3.8 5.3	5.5 7.5	1.0 1.0	6.5 8.5	1.0 1.0	8.5 10.5	
t _{PZL} , t _{PZH}	Maximum Output Enable TIme, OE to Y	$V_{CC} = 3.3 \pm 0.3V$ $R_L = 1 \text{ k}\Omega$	C _L = 15 pF C _L = 50 pF		5.4 7.9	8.0 11.5	1.0 1.0	9.5 13.0	1.0 1.0	11.5 15.0	ns
		V_{CC} = 5.0 \pm 0.5V R_L = 1 $k\Omega$			3.6 5.1	5.1 7.1	1.0 1.0	6.0 8.0	1.0 1.0	7.5 9.5	
t _{PLZ} , t _{PHZ}	Maximum Output Disable Time, OE to Y	$V_{CC} = 3.3 \pm 0.3V$ $R_L = 1 \text{ k}\Omega$	C _L = 50 pF		9.5	13.2	1.0	15.0	1.0	18.0	ns
		$V_{CC} = 5.0 \pm 0.5V$ $R_L = 1 \text{ k}\Omega$	C _L = 50 pF		6.1	8.8	1.0	10.0	1.0	12.0	
t _{OSLH} , t _{OSHL}	Output-to-Output Skew	V _{CC} = 3.3 ± 0.3V (Note 1)	C _L = 50 pF			1.5		1.5		1.5	ns
		V _{CC} = 5.0 ± 0.5V (Note 1)	C _L = 50 pF			1.0		1.0		1.0	
C _{in}	Maximum Input Capacitance				4	10		10		10	pF
C _{out}	Maximum Three-State Output Capacitance (Output in High Impedance State)				6						pF

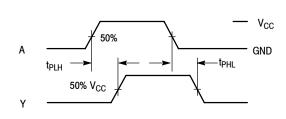
		Typical @ 25°C, V _{CC} = 5.0 V	
C _{PD}	Power Dissipation Capacitance (Note 2)	14	pF

NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

		T _A = 25°C		
Symbol	Characteristic	Тур	Max	Unit
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	0.3	0.8	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	-0.3	-0.8	V
V _{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V _{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHn}|, t_{OSHL} = |t_{PHLm} - t_{PHLn}|.
 C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/4 (per buffer). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

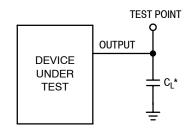
SWITCHING WAVEFORMS



 ν_{CC} 0E 50% GND - t_{PZL} t_{PLZ} HIGH **IMPEDANCE** 50% V_{CC} Υ $V_{OL} + 0.3V$ t_{PZH} t_{PHZ} V_{OH} - 0.3V Υ 50% V_{CC} HIGH **IMPEDANCE**

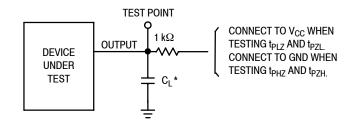
Figure 1.

Figure 2.



*Includes all probe and jig capacitance

Figure 3. Test Circuit



*Includes all probe and jig capacitance

Figure 4. Test Circuit

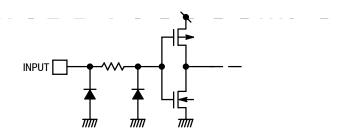
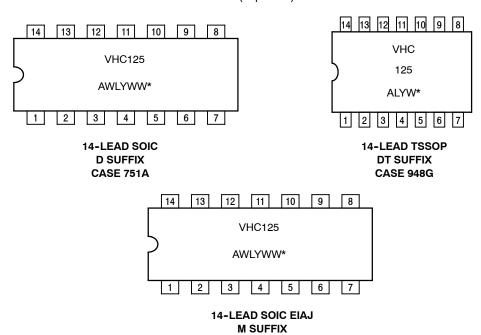


Figure 5. Input Equivalent Circuit

MARKING DIAGRAMS

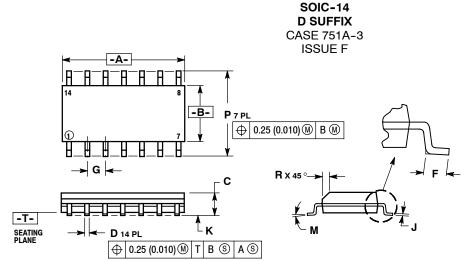
(Top View)



CASE 965

*See Applications Note AND8004/D for date code and traceability information.

PACKAGE DIMENSIONS



NOTES:

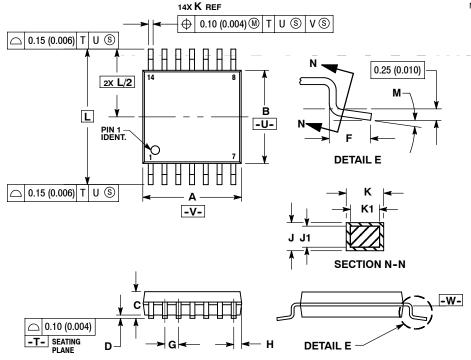
- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER. 3. DIMENSIONS A AND B DO NOT INCLUDE

- MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- PER SIDE.

 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS INCHES			HES
DIM	MIN	MAX	MIN	MAX
Α	8.55	8.75	0.337	0.344
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	BSC	0.050	BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
Р	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

TSSOP DT SUFFIX CASE 948G-01 **ISSUE O**



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH,
- PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- (LUVO) PEN SIDE.

 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- 0.25 (U.11) PER SIDE.
 DIMENSION K DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
 EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.

 6. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.

 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026	BSC
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252 BSC	
М	0°	8°	0°	8°

PACKAGE DIMENSIONS

SO-14 M SUFFIX CASE 965-01 ISSUE O LE Q1 Q1 DETAIL P VIEW P 0.13 (0.005) (0.004)

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS D AND E DO NOT INCLUDE
 MOLD FLASH OR PROTRUSIONS AND ARE
 MEASURED AT THE PARTING LINE. MOLD FLASH
 OR PROTRUSIONS SHALL NOT EXCEED 0.15
 (0.006) PER SIDE.
- 4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018)

	MILLIN	MILLIMETERS INCHES		
DIM	MIN	MAX	MIN	MAX
Α		2.05		0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
C	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
Е	5.10	5.45	0.201	0.215
е	1.27 BSC		0.050	BSC
HE	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10 °	0°	10°
Q_1	0.70	0.90	0.028	0.035
Z		1.42		0.056

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