# **Quad Bus Buffer**

# with 3-State Control Inputs

The MC74VHC126 is a high speed CMOS quad bus buffer fabricated with silicon gate CMOS technology. It achieves noninverting high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC126 requires the 3-state control input (OE) to be set Low to place the output into high impedance.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

- High Speed:  $t_{PD} = 3.8 \text{ ns}$  (Typ) at  $V_{CC} = 5.0 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 4.0 \mu A$  (Max) at  $T_A = 25^{\circ}C$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise:  $V_{OLP} = 0.8 \text{ V (Max)}$
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
- Chip Complexity: 72 FETs or 18 Equivalent Gates
- These devices are available in Pb-free package(s). Specifications herein
  apply to both standard and Pb-free devices. Please see our website at
  www.onsemi.com for specific Pb-free orderable part numbers, or
  contact your local ON Semiconductor sales office or representative.

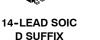


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CASE 751A





14-LEAD TSSOP DT SUFFIX CASE 948G



14-LEAD SOIC EIAJ M SUFFIX CASE 965

#### **PIN CONNECTIONS**

			L					
OE1	1 ●	14	] v <sub>cc</sub>					
A1 [	2	13	OE4					
Y1 [	3	12	] A4					
OE2	4	11	] Y4					
A2 [	5	10	OE3					
Y2 [	6	9	] A3					
GND [	7	8	] Y3					
(Top View)								

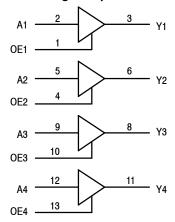
### **ORDERING INFORMATION**

Device	Package	Shipping
MC74VHC126D	SOIC	55 Units/Rail
MC74VHC126DT	TSSOP	96 Units/Rail
MC74VHC126M	SOIC EIAJ	50 Units/Rail

#### **DEVICE MARKING INFORMATION**

See general marking information in the device marking section on page 7 of this data sheet.

# **Active-High Output Enables**



# **FUNCTION TABLE**

VHC126							
Inp	outs	Output					
Α	OE	Υ					
Н	Н	Н					
L	Н	L					
Х	L	Z					

Figure 1. Logic Diagram

#### MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage	-0.5 to +7.0	V
V <sub>out</sub>	DC Output Voltage	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input Diode Current	-20	mA
lok	Output Diode Current	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air (Note 2) SOIC Packages TSSOP Package	500 450	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C

<sup>1.</sup> Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.

2. Derating - SOIC Packages: - 7.0 mW/°C from 65° to 125°C

TSSOP Package: - 6.1 mW/°C from 65° to 125°C

#### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	5.5	V
V <sub>in</sub>	DC Input Voltage	0	5.5	V
V <sub>out</sub>	DC Output Voltage	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time	_ 0 _ 0	100 20	ns/V

## DC ELECTRICAL CHARACTERISTICS

			V <sub>CC</sub>	1	A = 25°0	С	T <sub>A</sub> ≤	85°C	T <sub>A</sub> ≤	125°C	
Symbol	Parameter	Test Conditions	(V)	Min	Тур	Max	Min	Max	Min	Max	Unit
V <sub>IH</sub>	Minimum High-Level Input Voltage		2.0 3.0 4.5 5.5	1.5 2.1 3.15 3.85			1.5 2.1 3.15 3.85		1.5 2.1 3.15 3.85		V
V <sub>IL</sub>	Maximum Low-Level Input Voltage		2.0 3.0 4.5 5.5			0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65		0.5 0.9 1.35 1.65	٧
V <sub>OH</sub>	Minimum High-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OH} = -50 \mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		٧
		$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -4.0$ mA $I_{OH} = -8.0$ mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		٧
V <sub>OL</sub>	Maximum Low-Level Output Voltage V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 50  \mu\text{A}$	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	<b>V</b>
		$V_{IN} = V_{IH} \text{ or } V_{IL}$ $I_{OL} = 4.0 \text{ mA}$ $I_{OL} = 8.0 \text{ mA}$	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	٧
l <sub>OZ</sub>	Maximum 3-State Leakage Current	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND	5.5			±0.25		±2.5		±2.5	μΑ
I <sub>IN</sub>	Maximum Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μΑ
Icc	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5		_	4.0		40	_	40	μΑ

#### AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0 \text{ ns}$ )

				7	Γ <sub>A</sub> = 25°(	<b>C</b>	T <sub>A</sub> = ≤	85°C	T <sub>A</sub> = ≤ 125°C		
Symbol	Parameter	Test Condi	tions	Min	Тур	Max	Min	Max	Min	Max	Unit
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay,	$V_{CC} = 3.3 \pm 0.3 \text{ V}$	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		5.6 8.1	8.0 11.5	1.0 1.0	9.5 13.0	1.0 1.0	12.0 15.0	ns
	A to Y	$V_{CC} = 5.0 \pm 0.5 \text{ V}$	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		3.8 5.3	5.5 7.5	1.0 1.0	6.5 8.5	1.0 1.0	8.5 10.5	
t <sub>PZL</sub> , t <sub>PZH</sub>	Maximum Output Enable Time,	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $R_L = 1.0 \text{ k}\Omega$			5.4 7.9	8.0 11.5	1.0 1.0	9.5 13.0	1.0 1.0	11.5 15.0	ns
	OE to Y	$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $R_L = 1.0 \text{ k}\Omega$	C <sub>L</sub> = 15 pF C <sub>L</sub> = 50 pF		3.6 5.1	5.1 7.1	1.0 1.0	6.0 8.0	1.0 1.0	7.5 9.5	
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Maximum Output Disable Time,	$V_{CC} = 3.3 \pm 0.3 \text{ V}$ $R_L = 1.0 \text{ k}\Omega$	C <sub>L</sub> = 50 pF		9.5	13.2	1.0	15.0	1.0	18.0	ns
	OE to Y	$V_{CC} = 5.0 \pm 0.5 \text{ V}$ $R_L = 1.0 \text{ k}\Omega$	C <sub>L</sub> = 50 pF		6.1	8.8	1.0	10.0	1.0	12.0	
t <sub>OSLH</sub> , t <sub>OSHL</sub>	Output-to-Output Skew	V <sub>CC</sub> = 3.3 ± 0.3 V (Note 3)	C <sub>L</sub> = 50 pF			1.5		1.5		1.5	ns
		V <sub>CC</sub> = 5.0 ± 0.5 V (Note 3)	C <sub>L</sub> = 50 pF			1.0		1.0		1.0	
C <sub>in</sub>	Maximum Input Capacitance				4.0	10		10		10	pF
C <sub>out</sub>	Maximum Three-State Output Capacitance (Output in High Impedance State)				6.0						pF

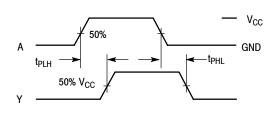
							Typical @ 25°C, V <sub>CC</sub> = 5.0V	
$C_{PD}$	Power Dissipation Capacitance (Note 4)	_	_	_	_	_	15	pF

# **NOISE CHARACTERISTICS** (Input $t_{f} = t_{f} = 3.0$ ns, $C_{L} = 50$ pF, $V_{CC} = 5.0$ V)

		T <sub>A</sub> = 25°C		
Symbol	Characteristic	Тур	Max	Unit
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	0.3	0.8	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	- 0.3	- 0.8	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		3.5	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		1.5	V

Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PLHn</sub>|.
 C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC(OPR)</sub> = C<sub>PD</sub> • V<sub>CC</sub> • f<sub>in</sub> + I<sub>CC</sub>/4 (per buffer). C<sub>PD</sub> is used to determine the no-load dynamic power consumption; P<sub>D</sub> = C<sub>PD</sub> • V<sub>CC</sub><sup>2</sup> • f<sub>in</sub> + I<sub>CC</sub> • V<sub>CC</sub>.

## **SWITCHING WAVEFORMS**



 $V_{CC}$ 0E 50% GND  $t_{PLZ}$  $t_{PZL}$ HIGH **IMPEDANCE** 50% V<sub>CC</sub> Υ  $V_{OL} + 0.3V$  $t_{PHZ}$  $t_{PZH}$ V<sub>OH</sub> - 0.3V 50% V<sub>CC</sub> HIGH **IMPEDANCE** 

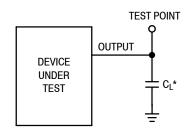
Figure 2.

Figure 3.

CONNECT TO  $V_{CC}$  WHEN TESTING  $t_{PLZ}$  AND  $t_{PZL}$  CONNECT TO GND WHEN

TESTING t<sub>PHZ</sub> AND t<sub>PZH</sub>.

TEST POINT



\*Includes all probe and jig capacitance

DEVICE UNDER TEST  $\begin{array}{c|c} \text{DEVICE} & \text{OUTPUT} & \text{$1$ k}\Omega \\ \text{$\emptyset$} & \text{$\emptyset$} & \text{$C_L$}^{\star} \\ \end{array}$ 

\*Includes all probe and jig capacitance

Figure 4. Test Circuit

Figure 5. Test Circuit

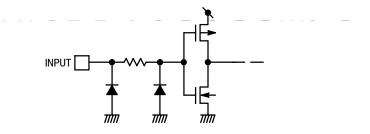
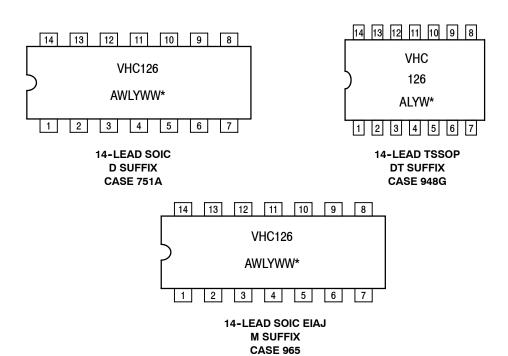


Figure 6. Input Equivalent Circuit

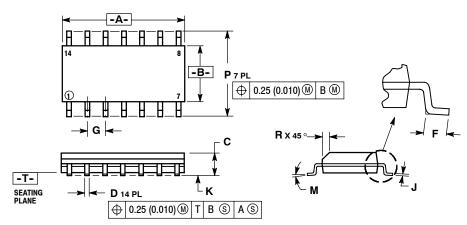
#### **MARKING DIAGRAMS**



\*See Applications Note #AND8004/D for date code and traceability information.

#### PACKAGE DIMENSIONS

## **D SUFFIX** SOIC-14 **CASE 751A-03 ISSUE F**

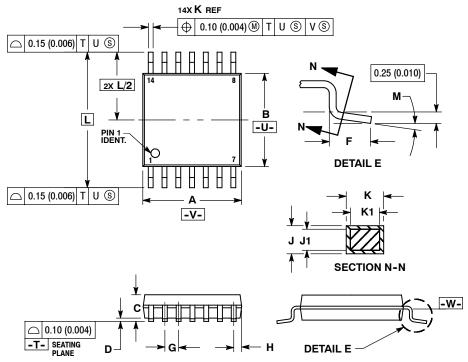


#### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. 2. CONTROLLING DIMENSION: MILLIMETER.
- 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
- 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	8.55	8.75	0.337	0.344	
В	3.80	4.00	0.150	0.157	
C	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050	BSC	
_	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
M	0°	7°	0°	7°	
Р	5.80	6.20	0.228 0.244		
R	0.25	0.50	0.010 0.019		

### **DT SUFFIX TSSOP CASE 948G-01 ISSUE O**



#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI
- 714.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH,
  PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD
  FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION: ALLOWABLE DAMBAR
  PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
  EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.

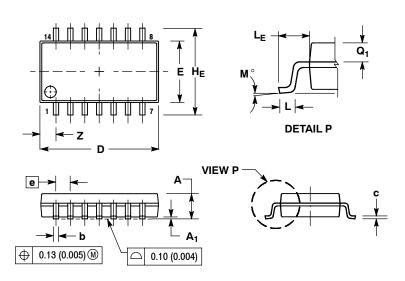
  6. TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.

  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026	BSC	
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BSC		
M	0°	8°	0° 8°		

#### PACKAGE DIMENSIONS

### **M SUFFIX** SO-14 **CASE 965-01 ISSUE O**



#### NOTES

- DIMENSIONING AND TOLERANCING PER ANSI
- Y14.5M, 1982. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006)
- TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
  THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE INCLUDE DAMBAR FROTROSION. ALEXWALL
  DAMBAR PROTRUSION SHALL BE 0.08 (0.003)
  TOTAL IN EXCESS OF THE LEAD WIDTH
  DIMENSION AT MAXIMUM MATERIAL CONDITION.
  DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE
  BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 ( 0.018).

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α		2.05		0.081	
A <sub>1</sub>	0.05	0.20	0.002	0.008	
b	0.35	0.50	0.014	0.020	
С	0.18	0.27	0.007	0.011	
D	9.90	10.50	0.390	0.413	
E	5.10	5.45	0.201	0.215	
е	1.27	BSC	0.050	BSC	
HE	7.40	8.20	0.291	0.323	
0.50	0.50	0.85	0.020	0.033	
LE	1.10	1.50	0.043	0.059	
M	0 °	10 °	0°	10°	
Q <sub>1</sub>	0.70	0.90	0.028	0.035	
Z		1.42	0.056		

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