2.5 V / 3.3 V / 5.0 V 1:4 Clock Fanout Buffer

Description

The NB3L553 is a low skew 1-to 4 clock fanout buffer, designed for clock distribution in mind. The NB3L553 specifically guarantees low output-to-output skew. Optimal design, layout and processing minimize skew within a device and from device to device.

The output enable (OE) pin three-states the outputs when low.

Features

- Input/Output Clock Frequency up to 200 MHz
- Low Skew Outputs (35 ps), Typical
- Output goes to Three-State Mode via OE
- Operating Range: $V_{DD} = 2.375 \text{ V}$ to 5.25 V
- Ideal for Networking Clocks
- Packaged in 8-pin SOIC
- Industrial Temperature Range
- These are Pb-Free Devices



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MARKING DIAGRAMS*



SOIC-8 D SUFFIX CASE 751



3L553 = Specific Device Code A = Assembly Location L = Wafer Lot Y = Year

W = Work Week
■ Pb-Free Package

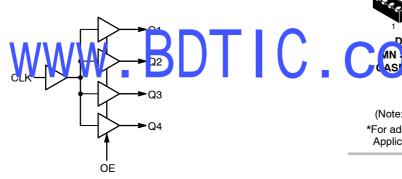


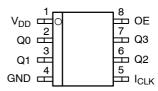
Figure 1. Block Diagram



XX = Specific Device Code \overline{M} = Date Code

(Note: Microdot may be in either location)
*For additional marking information, refer to
Application Note AND8002/D.

PINOUT



ORDERING INFORMATION

Device	Package	Shipping [†]
NB3L553DG	SOIC-8 (Pb-Free)	98 Units/Rail
NB3L553DR2G	SOIC-8 (Pb-Free)	2500/Tape & Reel
NB3L553MNR4G*	DFN-8 (Pb-Free)	1000/Tape & Reel

^{*}Contact Sales Representative

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

OE	Function
0	Disable
1	Enable

Table 1. OE, Output Enable Function

Table 2. PIN DESCRIPTION

Pin#	Name	Туре	Description
1	V_{DD}	Power	Positive supply voltage (2.375 V to 5.25 V)
2	Q0	(LV)CMOS/(LV)TTL Output	Clock Output 0
3	Q1	(LV)CMOS/(LV)TTL Output	Clock Output 1
4	GND	Power	Negative supply voltage; Connect to ground, 0 V
5	ICLK	(LV)CMOS/(LV)TTL Input	Clock Input. 5.0 V tolerant
6	Q2	(LV)CMOS/(LV)TTL Output	Clock Output 2
7	Q3	(LV)CMOS/(LV)TTL Output	Clock Output 3
8	OE	(LV)CMOS/(LV)TTL Input	Output Enable for the clock outputs. Outputs are enabled when HIGH: connect to V_{DD} for normal operation; OE pin has internal pull-up resistor. Three-states outputs when LOW.
-	EP	Thermal Exposed Pad	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

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Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{DD}	Positive Power Supply	GND = 0 V	-	6.0	V
VI	Input Voltage	-	-	GND $-0.5 \le V_{I} \le V_{DD} + 0.5$	V
T _A	Operating Temperature Range, Industrial	-	-	≥ -40 to ≤ +85	°C
T _{stg}	Storage Temperature Range	-	-	-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8	190 130	°C/W °C/W
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	(Note 1)	SOIC-8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W
$\theta_{\sf JC}$	Thermal Resistance (Junction-to-Case)	(Note 1)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

Table 4. ATTRIBUTES

Charac	Value	
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 150 V > TBD kV
Moisture Sensitivity, Indefinite T	ime Out of Drypack (Note 2)	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL-94 code V-0 @ 0.125 in
~~~~	and I IA/JE! D78 IC Latchup Tost	531 Devices

Table 5. DC CHARACTERISTICS (V_{DD} = 2.375 V to 2.625 V, GND = 0 V, T_A = -40°C to +85°C) (Note 3)

Symbol	Characteristic	Min	Тур	Max	Unit
I _{DD}	Power Supply Current @ 135 MHz, No Load	-	25	30	mA
V _{OH}	Output HIGH Voltage – I _{OH} = –16 mA	1.7	-	-	V
V _{OL}	Output LOW Voltage – I _{OL} = 16 mA		-	0.4	V
V _{IH,} I _{CLK}	I _{CLK} Input HIGH Voltage, I _{CLK}		-	3.8	V
V _{IL,} I _{CLK}	Input LOW Voltage, I _{CLK}		-	(V _{DD} ÷2)-0.5	V
V _{IH,} OE	Input HIGH Voltage, OE		-	V_{DD}	V
V _{IL,} OE	Input LOW Voltage, OE	_	-	0.7	V
ZO	Nominal Output Impedance		20	-	Ω
CIN	Input Capacitance, I _{CLK} , OE	-	5.0	-	pF
IOS	Short Circuit Current	-	± 28	-	mA

DC CHARACTERISTICS (V_{DD} = 3.15 V to 3.45 V, GND = 0 V, T_A = -40° C to $+85^{\circ}$ C) (Note 3)

Symbol	Characteristic	Min	Тур	Max	Unit
I _{DD}	Power Supply Current @ 135 MHz, No Load	_	35	40	mA
V _{OH}	Output HIGH Voltage – I _{OH} = -25 mA	2.4	ı	-	٧
V_{OL}	Output LOW Voltage – I _{OL} = 25 mA	-	I	0.4	V
V _{OH}	Output HIGH Voltage – I _{OH} = –12 mA (CMOS level)	V _{DD} – 0.4	-	-	V
V _{IH,} I _{CLK}	Input HIGH Voltage, I _{CLK}	(V _{DD} ÷2)+0.7	ı	3.8	V
V _{IL,} I _{CLK}	Input LOW Voltage, I _{CLK}	-	-	(V _{DD} ÷2)-0.7	V
V _{IH,} OE	Input HIGH Voltage, OE	2.0	I	V_{DD}	V
V _{IL,} OE	Input LOW Voltage, OE	0	-	2.8	V
ZO	Nornii I al Outbut Impedar 😎		2	1	Ω
CIN	input Cupacitance, JE		9.0		pF
IOS	Short Circuit Current	-	± 50	-	mA

DC CHARACTERISTICS (V_{DD} = 4.75 V to 5.25 V, GND = 0 V, T_A = $-40^{\circ}C$ to $+85^{\circ}C$) (Note 3)

Symbol	Characteristic	Min	Тур	Max	Unit
I _{DD}	Power Supply Current @ 135 MHz, - No Load	-	45	85	mA
V _{OH}	Output HIGH Voltage – I _{OH} = –35 mA	2.4	-	-	V
V _{OL}	Output LOW Voltage – I _{OL} = 35 mA	-	-	0.4	V
V _{OH}	Output HIGH Voltage – I _{OH} = –12 mA (CMOS level)		-	-	V
V _{IH,} I _{CLK}	Input HIGH Voltage, I _{CLK}	(V _{DD} ÷2) + 1	-	5.5	V
V _{IL,} I _{CLK}	Input LOW Voltage, I _{CLK}	-	-	(V _{DD} ÷2) – 1	V
V _{IH,} OE	Input HIGH Voltage, OE	2.0	-	V_{DD}	V
V _{IL,} OE	Input LOW Voltage, OE	-	-	0.8	V
ZO	Nominal Output Impedance	-	20	-	Ω
CIN	Input Capacitance, OE	-	5.0	-	pF
IOS	Short Circuit Current	-	± 80	-	mA

Table 6. AC CHARACTERISTICS; V_{DD} = 2.5 V ±5% (V_{DD} = 2.375 V to 2.625 V, GND = 0 V, T_A = -40°C to +85°C) (Note 3)

Symbol	pol Characteristic		Тур	Max	Unit
f _{in}	Input Frequency	-	-	200	MHz
t _r /t _f	Output rise and fall times; 0.8 V to 2.0 V	-	1.0	1.5	ns
t _{pd}	Propagation Delay, CLK to Qn (Note 4)	2.2	3.0	5.0	ns
t _{skew}	Output-to-output skew; (Note 5)	-	35	50	ps
t _{skew}	Device-to-device skew, (Note 5)	-	-	500	ps

AC CHARACTERISTICS; V_{DD} = 3.3 V ±5% (V_{DD} = 3.15 V to 3.45 V, GND = 0 V, T_A = -40°C to +85°C) (Note 3)

Symbol	Characteristic	Min	Тур	Max	Unit
f _{in}	Input Frequency	-	-	200	MHz
t _r /t _f	Output rise and fall times; 0.8 V to 2.0 V	-	0.6	1.0	ns
t _{pd}	Propagation Delay, CLK to Qn (Note 4)	2.0	2.4	4.0	ns
t _{skew}	t _{skew} Output-to-output skew; (Note 5)		35	50	ps
t _{skew}	Device-to-device skew, (Note 5)	_	-	500	ps

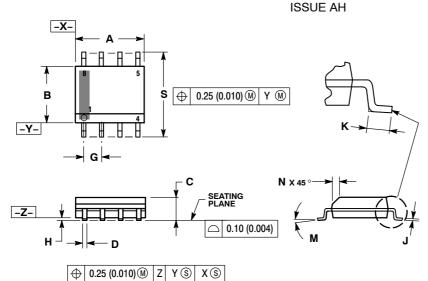
AC CHARACTERISTICS; V_{DD} = 5.0 V ±5% (V_{DD} = 4.75 V to 5.25 V, GND = 0 V, T_A = -40°C to +85°C) (Note 3)

Symbol	Characteristic		Тур	Max	Unit
f _{in}	Input Frequency		-	200	MHz
t _r /t _f	Output rise and fall times; 0.8 V to 2.0 V	-	0.3	0.7	ns
t _{pd}	Propagation Delay, CLK to Qn (Note 4)	1.7	2.5	4.0	ns
t _{skew}	Output-to-output skew; (Note 5)		35	50	ps
t _{skew}	Device-to-device skew, (Note 5)	_	-	500	ps

Outputs loaded with external R_L = 33-5 corie register and C_I = 15 pr to GND for proper operation. Duty cycle cut is duty in. A 0.01 μF decoupling copacitor should be connected betiveen V_{DI} and C ND.
 Measured vit air-to-ral in air clock
 Measured vit is air-to-ral in air to gestat V_{DD} ± 2 between any two outputs with rapid loading.

PACKAGE DIMENSIONS

SOIC-8 NB CASE 751-07



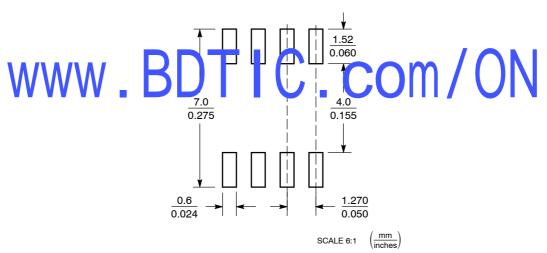
NOTES:

- DIMENSIONING AND TOLERANCING PER
 ANSI Y14 5M 1982
- ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
- PER SIDE.

 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
- 6. 751–01 THRU 751–06 ARE OBSOLETE. NEW STANDARD IS 751–07.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.80	5.00	0.189	0.197
В	3.80	4.00	0.150	0.157
С	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27	BSC	0.05	0 BSC
Η	0.10	0.25	0.004	0.010
7	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
М	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

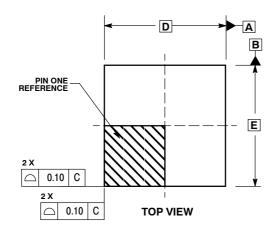
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

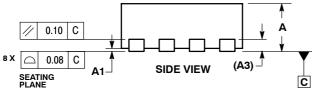
PACKAGE DIMENSIONS

DFN8 CASE 506AA-01 ISSUE D

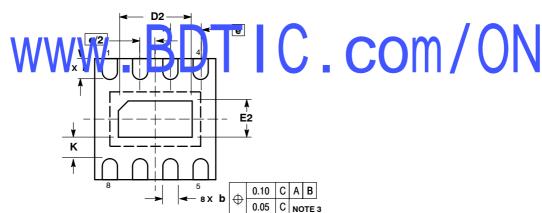


- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
- ASME Y14.5M, 1994 . CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b APPLIES TO PLATED
 TERMINAL AND IS MEASURED BETWEEN
- 0.25 AND 0.30 MM FROM TERMINAL.
 COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
Α	0.80	1.00
A1	0.00	0.05
АЗ	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
е	0.50 BSC	
K	0.20	
L	0.25	0.35



BOTTOM VIEW



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