

NB6L11S

2.5 V 1:2 AnyLevel™ Input to LVDS Fanout Buffer / Translator

The NB6L11S is a differential 1:2 clock or data receiver and will accept AnyLevel™ input signals: LVPECL, CML, LVCMOS, LVTTTL, or LVDS. These signals will be translated to LVDS and two identical copies of Clock or Data will be distributed, operating up to 2.0 GHz or 2.5 Gb/s, respectively. As such, the NB6L11S is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications.

The NB6L11S has a wide input common mode range from GND + 50 mV to $V_{CC} - 50$ mV. Combined with the 50 Ω internal termination resistors at the inputs, the NB6L11S is ideal for translating a variety of differential or single-ended Clock or Data signals to 350 mV typical LVDS output levels.

The NB6L11S is the 2.5 V version of the NB6N11S and is offered in a small 3 mm X 3 mm 16-QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

Features

- Input Clock Frequency > 2.0 GHz
- Input Data Rate > 2.5 Gb/s
- RMS Clock Jitter - 0.5 ps, Typical
- 622 Mb/s Data Dependent Jitter - 5 ps, Typical
- 380 ps Typical Propagation Delay
- 120 ps Typical Rise and Fall Times
- Single Power Supply; $V_{CC} = 2.5 \text{ V} \pm 5\%$
- These are Pb-Free Devices

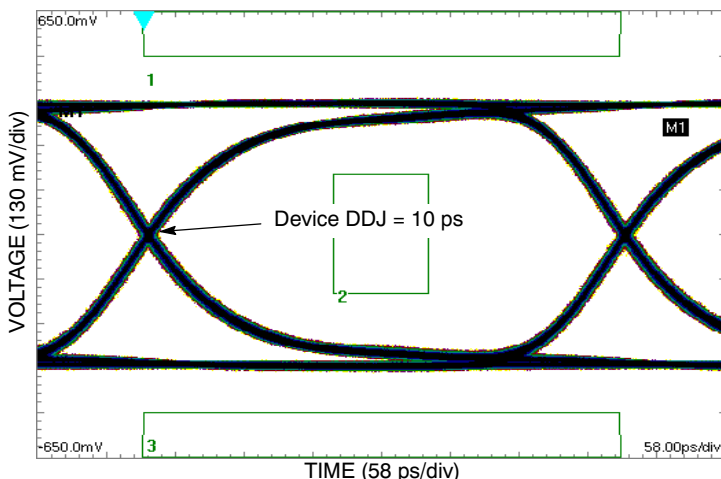


Figure 2. Typical Output Waveform at 2.488 Gb/s with PRBS $2^{23}-1$ ($V_{INPP} = 400$ mV; Input Signal DDJ = 14 ps)



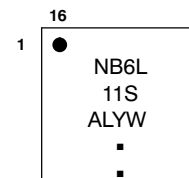
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM*



QFN-16
MN SUFFIX
CASE 485G



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)
*For additional marking information, refer to Application Note AND3002.D

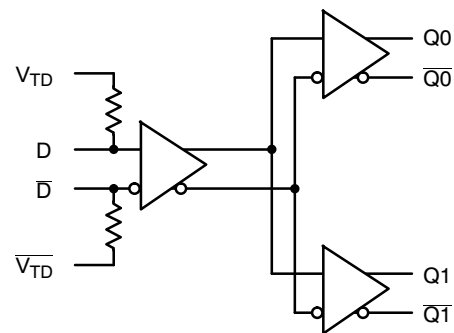


Figure 1. Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

NB6L11S

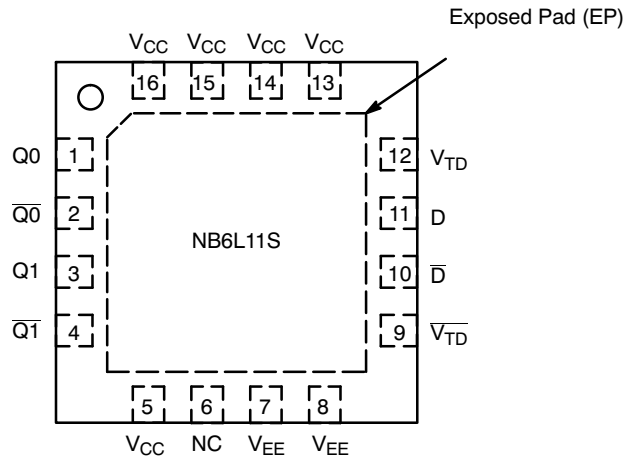


Figure 3. NB6L11S Pinout, 16-pin QFN (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	Q0	LVDS Output	Non-inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
2	$\overline{Q0}$	LVDS Output	Inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
3	Q1	LVDS Output	Non-inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
4	$\overline{Q1}$	LVDS Output	Inverted D output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
5	V_{CC}	-	Positive Supply Voltage.
6	NC	-	No Connect.
7	V_{EE}	-	Negative Supply Voltage.
8	V_{EE}	-	Negative Supply Voltage.
9	$\overline{V_{TD}}$	-	Internal 50 Ω termination pin for \overline{D} .
10	\overline{D}	LVPECL, CML, LVDS, LVCMOS, LVTTTL	Inverted Differential Clock/Data Input (Note 1).
11	D	LVPECL, CML, LVDS, LVCMOS, LVTTTL	Non-inverted Differential Clock/Data Input (Note 1).
12	V_{TD}	-	Internal 50 Ω termination pin for \overline{D} .
13	V_{CC}	-	Positive Supply Voltage.
14	V_{CC}	-	Positive Supply Voltage.
15	V_{CC}	-	Positive Supply Voltage.
16	V_{CC}	-	Positive Supply Voltage.
EP			Exposed pad. The exposed pad (EP) on the package bottom must be attached to a heat-sinking conduit. The exposed pad may only be electrically connected to V_{EE} .

1. In the differential configuration when the input termination pins (V_{TD0}/V_{TD0} , V_{TD1}/V_{TD1}) are connected to a common termination voltage or left open, and if no signal is applied on $D0/\overline{D0}$, $D1/\overline{D1}$ input, then the device will be susceptible to self-oscillation.

NB6L11S

Table 2. ATTRIBUTES

Characteristic	Value
ESD Protection Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 1 kV
Moisture Sensitivity (Note 2)	Pb-Free Pkg
QFN-16	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	225
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

2. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		3.8	V
V_{IN}	Positive Input	GND = 0 V	$V_{IN} \leq V_{CC}$	3.8	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		35 70	mA mA
I_{OSC}	Output Short Circuit Current Line-to-Line (Q to \bar{Q}) Line-to-End (Q or \bar{Q} to GND)	Q or \bar{Q} Q to \bar{Q} to GND	Continuous Continuous	12 24	mA
T_A	Operating Temperature Range	QFN-16		-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction to Ambient) (Note 3)	0 l fpm 500 l fpm	QFN-16 QFN-16	1.6 3.2	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction to Case)	1S2P (Note 3)	QFN-16	4.0	°C/W
T_{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board - 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

NB6L11S

Table 4. DC CHARACTERISTICS, CLOCK INPUTS, LVDS OUTPUTS $V_{CC} = 2.375 \text{ V to } 2.625 \text{ V}$, $GND = 0 \text{ V}$,
 $T_A = -40^\circ\text{C to } +85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Note 8)		30	45	mA

DIFFERENTIAL INPUTS DRIVEN SINGLE-ENDED (Figures 11, 12, 16, and 18)

V_{th}	Input Threshold Reference Voltage Range (Note 7)	$GND + 100$		$V_{CC} - 100$	mV
V_{IH}	Single-ended Input HIGH Voltage	$V_{th} + 100$		V_{CC}	mV
V_{IL}	Single-ended Input LOW Voltage	GND		$V_{th} - 100$	mV

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 7, 8, 9, 10, 17, and 19)

V_{IHD}	Differential Input HIGH Voltage	100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage	GND		$V_{CC} - 100$	mV
V_{CMR}	Input Common Mode Range (Differential Configuration)	$GND + 50$		$V_{CC} - 50$	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	100		$V_{CC} - GND$	mV
R_{TIN}	Internal Input Termination Resistor	40	50	60	Ω

LVDS OUTPUTS (Note 4)

V_{OD}	Differential Output Voltage	250		450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States (Note 9)	0	1	25	mV
V_{OS}	Offset Voltage (Figure 15)	1125		1375	mV
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States (Note 9)	0	1	25	mV
V_{OH}	Output HIGH Voltage (Note 5)		1425	1600	mV
V_{OL}	Output LOW Voltage (Note 6)	900	1075		mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 fpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- LVDS outputs require 100 Ω receiver termination resistor between differential pair. See Figure 14.
- $V_{OHmax} = V_{OSmax} + \frac{1}{2} V_{ODmax}$.
- $V_{OLmax} = V_{OSmin} - \frac{1}{2} V_{ODmax}$.
- V_{th} is applied to the complementary input when operating in single-ended mode.
- Input termination pins open, D/\bar{D} at the DC level within V_{CMR} and output pins loaded with $R_L = 100 \Omega$ across differential.
- Parameter guaranteed by design verification not tested in production.

NB6L11S

Table 5. AC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }2.625\text{ V}$, $GND = 0\text{ V}$; (Note 10)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \leq 1.0\text{ GHz}$ (Figure 4) $f_{in} = 1.5\text{ GHz}$ $f_{in} = 2.0\text{ GHz}$	220 200 170	350 300 270		220 200 170	350 300 270		220 200 170	350 300 270		mV
f_{DATA}	Maximum Operating Data Rate	1.5	2.5		1.5	2.5		1.5	2.5		Gb/s
t_{PLH} , t_{PHL}	Differential Input to Differential Output Propagation Delay	250		450	250	380	450	250		450	ps
t_{SKEW}	Duty Cycle Skew (Note 11) Within Device Skew (Note 16) Device-to-Device Skew (Note 15)		8 5 30	45 25 100		8 5 30	45 25 100		8 5 30	45 25 100	ps
t_{JITTER}	RMS Random Clock Jitter (Note 13) $f_{in} = 1.0\text{ GHz}$ $f_{in} = 1.5\text{ GHz}$ Peak-to-Peak Data Dependent Jitter (Note 14) $f_{DATA} = 622\text{ Mb/s}$ $f_{DATA} = 1.5\text{ Gb/s}$ $f_{DATA} = 2.488\text{ Gb/s}$		0.5 0.5 6 7 10			0.5 0.5 6 7 10			0.5 0.5 6 7 10		ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 12)	100		$V_{CC}-GND$	100		$V_{CC}-GND$	100		$V_{CC}-GND$	mV
t_r , t_f	Output Rise/Fall Times @ 250 MHz (20% – 80%) Q, \bar{Q}	70	120	170	70	120	170	70	120	170	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Measured by forcing $V_{INPPmin}$ with 50% duty cycle clock source and $V_{CC} = 1400\text{ mV}$ offset. All loading with an external $R_L = 100\ \Omega$ across "D" and "D" of the receiver. Input edge rates 150 ps (20%–80%).

11. See Figure 13 differential measurement of skew = $t_{PLH} - t_{PHL}$ for a nominal 50% differential clock input waveform @ 250 MHz.

12. Input voltage swings 2.5 single-ended measurement operating in differential mode.

13. RMS jitter with 50% Duty Cycle input clock signal.

14. Deterministic jitter with input NRZ data at P1ES223-1 and K2.5.

15. Skew is measured between outputs under identical transition @ 250 MHz.

16. The worst case condition between $Q0/\bar{Q}0$ and $Q1/\bar{Q}1$ from either $D0/\bar{D}0$ or $D1/\bar{D}1$, when both outputs have the same transition.

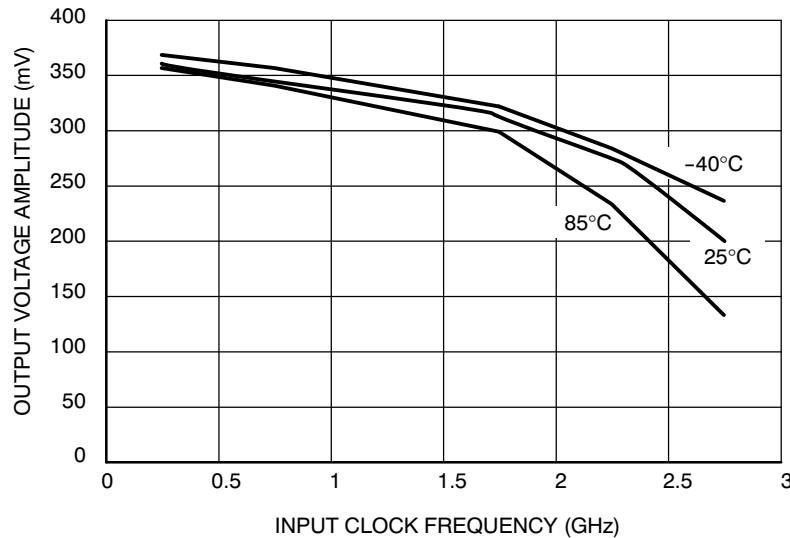


Figure 4. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{in}) and Temperature (@ $V_{CC} = 2.5\text{ V}$)

NB6L11S

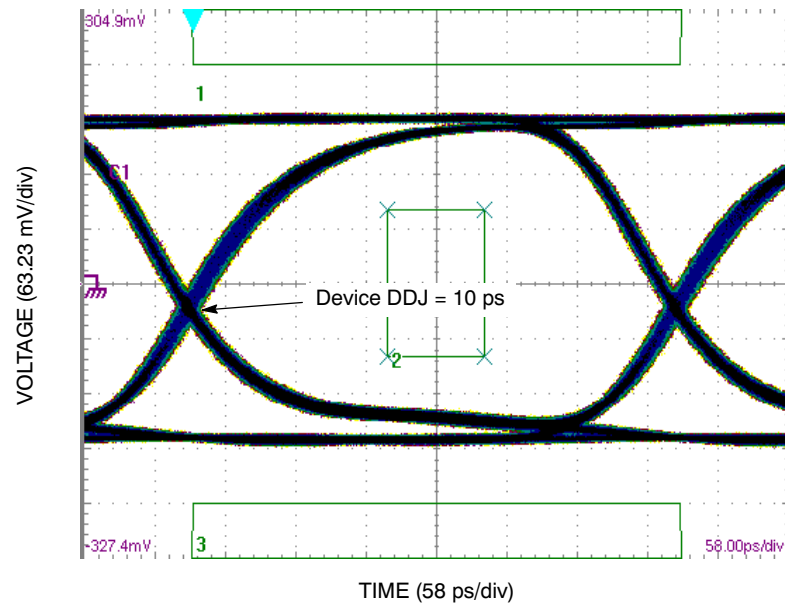


Figure 5. Typical Output Waveform at 2.488 Gb/s with PRBS $2^{23}-1$ and OC48 mask ($V_{INPP} = 100$ mV; Input Signal DDJ = 14 ps)

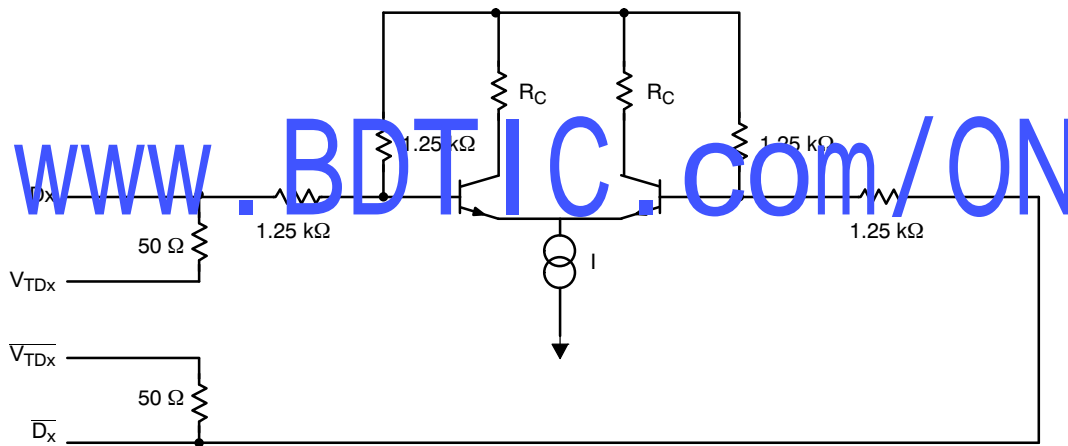


Figure 6. Input Structure

NB6L11S

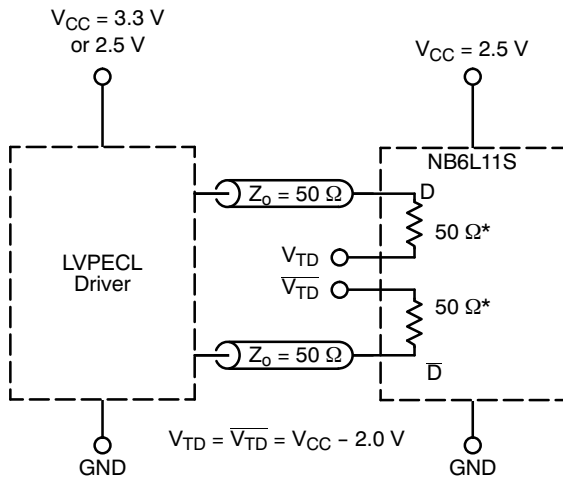


Figure 7. LVPECL Interface

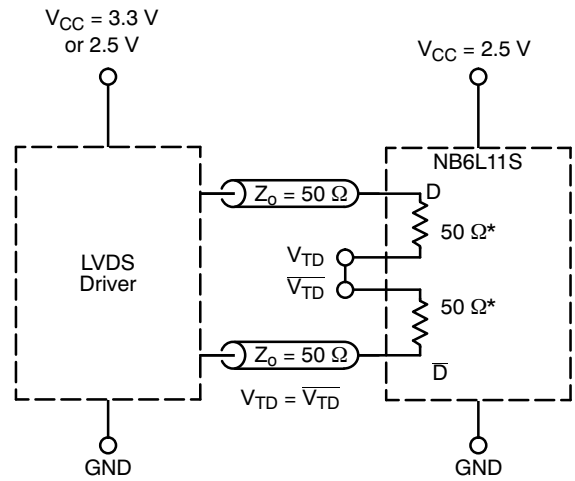


Figure 8. LVDS Interface

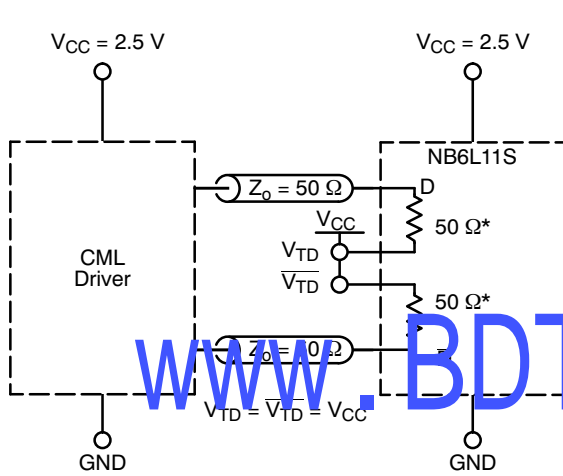


Figure 9. Standard 50 Ω Load CML Interface

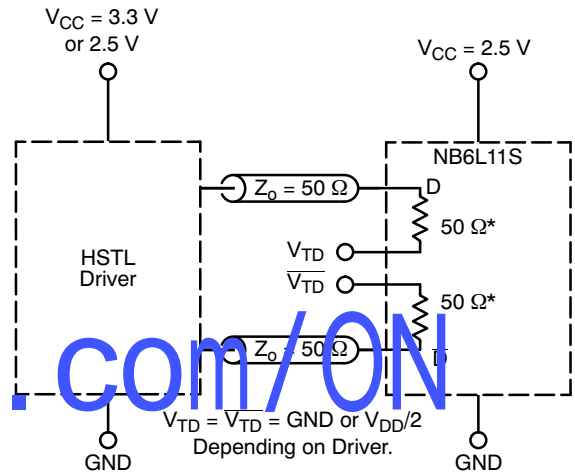


Figure 10. HSTL Interface

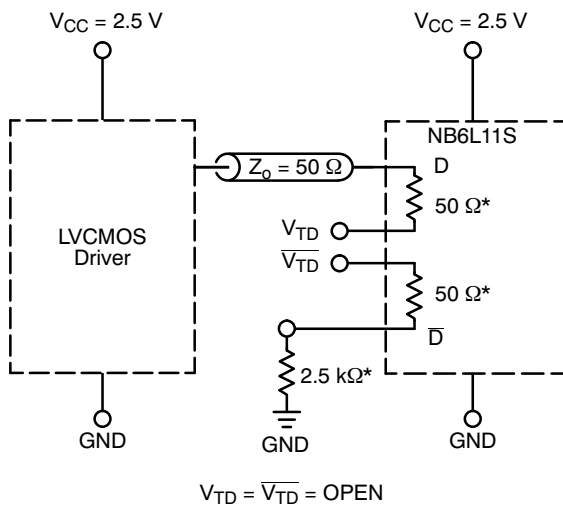


Figure 11. LVCMOS Interface

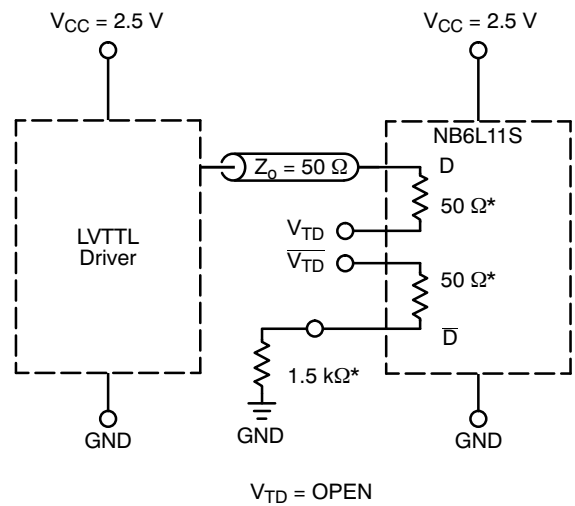


Figure 12. LVTTTL Interface

* R_{TIN} , Internal Input Termination Resistor.

The diagram shows the input and output waveforms for a CMOS inverter. The input signal D (solid line) and its complement \overline{D} (dashed line) are shown. The output signal Q (solid line) and its complement \overline{Q} (dashed line) are also shown. The input signal D transitions from low to high and high to low. The output signal Q transitions from high to low and low to high. The propagation delay t_{PLH} is the time from the input signal D crossing $V_{IL}(D)$ to the output signal Q crossing $V_{OL}(Q)$. The propagation delay t_{PHL} is the time from the input signal D crossing $V_{IH}(D)$ to the output signal Q crossing $V_{OH}(Q)$. The input signal D is labeled with $V_{INPP} = V_{IH}(D) - V_{IL}(D)$. The output signal Q is labeled with $V_{OUTPP} = V_{OH}(Q) - V_{OL}(Q)$.

Diagram illustrating the connection between an LVDS Driver Device and an LVDS Receiver Device. The driver outputs signals Q and \bar{Q} through impedances $Z_0 = 50\ \Omega$. These signals are connected to a differential load resistor of $100\ \Omega$, which is connected to the receiver inputs D and \bar{D} .

The diagram illustrates the relationship between the input signal levels and the output signal levels for a CMOS inverter. The input signals are labeled V_{thmax} and V_{thmin} . The output signals are labeled V_{IHmax} , V_{ILmax} , V_{IHmin} , and V_{ILmin} . The input signal D is shown as a step function that transitions from V_{thmin} to V_{thmax} . The output signal D is shown as a step function that transitions from V_{ILmin} to V_{IHmin} . The input signal \bar{D} is shown as a step function that transitions from V_{thmax} to V_{thmin} . The output signal \bar{D} is shown as a step function that transitions from V_{IHmax} to V_{ILmax} .

<http://onsemi.com>

NB6L11S

ORDERING INFORMATION

Device	Package	Shipping†
NB6L11SMNG	QFN-16, 3 X 3 mm (Pb-Free)	123 Units / Rail
NB6L11SMNR2G	QFN-16, 3 X 3 mm (Pb-Free)	3000 / Tape & Reel

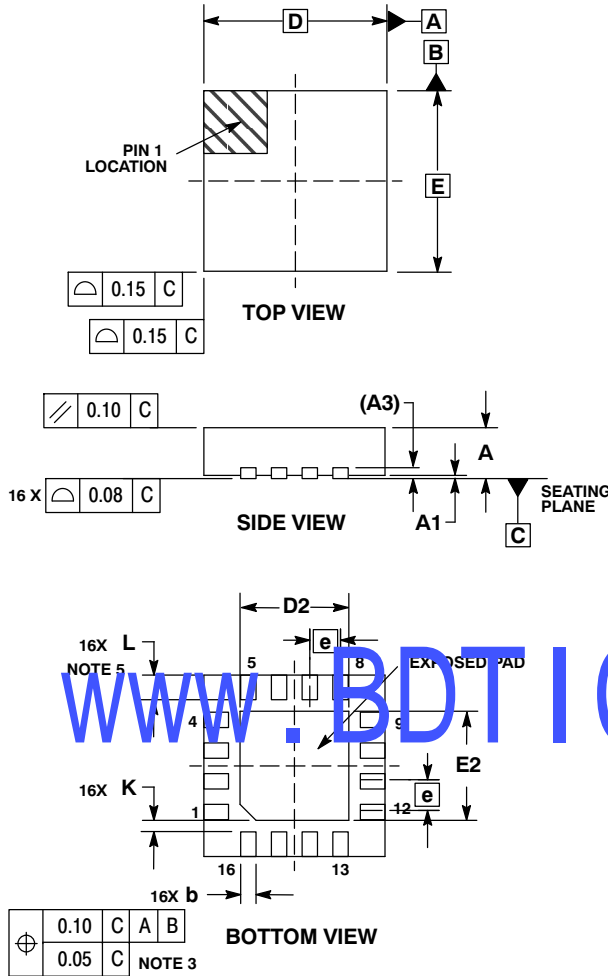
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

www.BDTIC.com/ON

NB6L11S

PACKAGE DIMENSIONS

16 PIN QFN
CASE 485G-01
ISSUE C

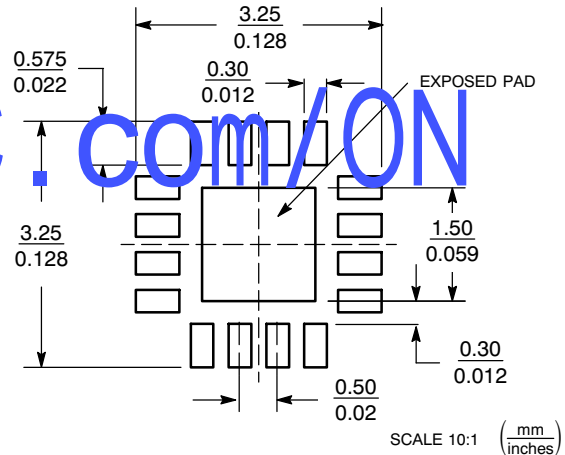


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. L_{max} CONDITION CAN NOT VIOLATE 0.2 MM MINIMUM SPACING BETWEEN LEAD TIP AND FLAG

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.18	0.30
D	3.00	BSC
D2	1.65	1.85
E	3.00	BSC
E2	1.65	1.85
e	0.50	BSC
K	0.18	TYP
L	0.30	0.50

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local Sales Representative