# 1.8V Differential 2:1 Mux Input to 1.2V/1.8V 1:6 CML Clock/Data Fanout Buffer / **Translator**

# Multi-Level Inputs w/ Internal Termination Description

The NB7V586M is a differential 1-to-6 CML Clock/Data Distribution chip featuring a 2:1 Clock/Data input multiplexer with an input select pin. The INx/ $\overline{\text{INx}}$  inputs incorporate internal 50  $\Omega$ termination resistors and will accept differential LVPECL, CML, or LVDS logic levels (see Figure 12). The INx/INx inputs and core logic are powered with a 1.8 V supply. The NB7V586M produces six identical differential CML output copies of Clock or Data. The outputs are configured as three banks of two differential pair. Each bank (or all three banks) have the flexibility of being powered by any combination of either a 1.8 V or 1.2 V supply.

The 16 mA differential CML output structure provides matching internal 50  $\Omega$  source terminations and 400 mV output swings when externally terminated with a 50  $\Omega$  resistor to  $V_{CCO}x$  (see Figure 11).

The 1:6 fanout design was optimized for low output skew and minimal jitter and is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock/Data dismorting ppn ation operating up to 6 GHz of 10 Ge/s typical. The Vacantee reference out outs can be up to 6 GHz o 10 Gu/s/typical. The V used to rebits tapycitor- a upled different alor single-ended input signals.

The NB7V586M is offered in a low profile 5x5 mm 32-pin Pb-Free QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

The NB7V586M is a member of the GigaComm<sup>™</sup> family of high performance clock products.

#### **Features**

- Maximum Input Data Rate > 10 Gb/s Typical
- Data Dependent Jitter < 10 ps
- Maximum Input Clock Frequency > 6 GHz Typical
- Random Clock Jitter < 0.8 ps RMS, Max
- Low Skew 1:6 CML Outputs, 20 ps Max
- 2:1 Multi-Level Mux Inputs
- 175 ps Typical Propagation Delay
- 50 ps Typical Rise and Fall Times
- Differential CML Outputs, 330 mV Peak-to-Peak, Typical
- Operating Range: V<sub>CC</sub> = 1.71 V to 1.89 V
- Operating Range: V<sub>CCO</sub>x = 1.14 V to 1.89 V
- Internal 50  $\Omega$  Input Termination Resistors
- V<sub>REFAC</sub> Reference Output
- QFN32 Package, 5 mm x 5 mm
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices



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#### **MARKING DIAGRAM\***



QFN32 **MN SUFFIX** CASE 488AM

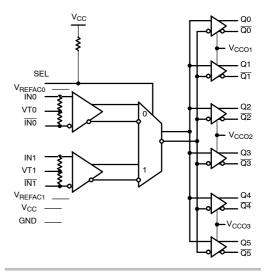


= Assembly Location

WI = Wafer Lot YY = Year WW = Work Week G or ■ = Pb-Free Package

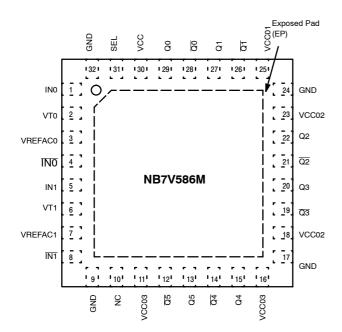
\*For additional marking information Note AND 300 2/D.

# SIMPLIFIED LOGIC DIAGRAM



#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.



**Table 1. INPUT SELECT FUNCTION TABLE** 

SEL*	CLK Input Selected
0	IN0
1	IN1

<sup>\*</sup>Defaults HIGH when left open.

Figure 1. 32-Lead QFN Pinout (Top View)

# **Table 2. PIN DESCRIPTION**

	ubic 2.1 IN DECOMI TION				
Pin	Name	I/O	Description		
1,4 5,8	IN0, <u>IN0</u> IN1, <u>IN1</u>	LVPECL, CML, LVDS Input	Non-inverted, Inverted, Differential Inputs		
2,6	VT0, VT1		Internal 100 $\Omega$ Center-tapped Termination Pin for IN0/ $\overline{\text{IN0}}$ and IN1/ $\overline{\text{IN1}}$		
31	ASEL A/\\	LVTTL/LVCN OS Input	npu Sel ict pin; LOV for N0 Inputs LIGH for IN1 Inputs; defai its PIC i wien left open		
10	NO	<b>VV</b> . <b>D</b>	Lis Connect		
30	VCC	-	1.8 V Positive Supply Voltage for the Inputs and Core Logic.		
25	VCCO1		1.2 V or 1.8 V Positive Supply Voltage for the Q0, Q0, Q1, Q1 CML Outputs		
18, 23	VCCO2	-	1.2 V or 1.8 V Positive Supply Voltage for the Q2, Q2, Q3, Q3 CML Outputs		
11, 16	VCCO3		1.2 V or 1.8 V Positive Supply Voltage for the Q4, Q4, Q5, Q5 CML Outputs		
29, 28 27, 26	Q0, <u>Q0</u> Q1, <u>Q1</u>	1.2 V or 1.8 V CML Output	Non-inverted, Inverted Differential Outputs; powered by VCCO1 (Notes 1 and 2).		
22, 21 20, 19	Q2, <u>Q2</u> Q3, <u>Q3</u>	1.2 V or 1.8 V CML Output	Non-inverted, Inverted Differential Outputs; powered by VCCO2 (Notes 1 and 2).		
15, 14 13, 12	Q4, <u>Q4</u> Q5, <u>Q5</u>	1.2 V or 1.8 V CML Output	Non-inverted, Inverted Differential Outputs; powered by VCCO3 (Notes 1 and 2).		
9, 17, 24, 32	GND		Negative Supply Voltage, connected to Ground		
3 7	VREFAC0 VREFAC1	-	Output Voltage Reference for Capacitor-Coupled Inputs, only		
-	EP	-	The Exposed Pad (EP) on the QFN-32 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board.		

In the differential configuration when the input termination pins (VT0, VT1) are connected to a common termination voltage or left open, and
if no signal is applied on INn/INn input, then, the device will be susceptible to self-oscillation. Qn/Qn outputs have internal 50 Ω source
termination resistors.

<sup>2.</sup> All  $V_{CC}$ , VCC0x and GND pins must be externally connected to a power supply for proper operation.

Table 3. ATTRIBUTES

Characte	Value			
ESD Protection	> 2 kV > 200 V			
Input Pullup Resistor (R <sub>PU</sub> )	75 kΩ			
Moisture Sensitivity (Note 3)	Level 1			
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in		
Transistor Count	308			
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test				

<sup>3.</sup> For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS** 

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		3.0	V
V <sub>CCOx</sub>	Positive Power Supply	GND = 0 V		3.0	V
V <sub>IO</sub>	Input/Output Voltage	GND = 0 V	$-0.5 \le V_{IO} \le V_{CC} + 0.5$	$-0.5$ to $V_{CC} + 0.5$	V
V <sub>INPP</sub>	Differential Input Voltage  IN <sub>x</sub> - IN <sub>x</sub>			1.89	V
I <sub>IN</sub>	Input Current Through R $_{T}$ (50 $\Omega$ Resistor)			±40	mA
I <sub>OUT</sub>	Output Current	Continuous Surge		34 40	mA
I <sub>VFREFAC</sub>	V <sub>REFAC</sub> Sink/Source Current			± 1.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range		00m	-6 i t ) +1 i0	°C
$\theta_{\sf JA}$	The man Registance (Junction -to- Ambient) (Noto 4)	0 lfr n 500 .fpm	CFN-31 Cr12-32	17	°C/W °C/W
θJC	Thermal Resistance (Junction-to-Case) (Note 4)	Standard Board	QFN-32	12	°C/W
T <sub>sol</sub>	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

 $\textbf{Table 5. DC CHARACTERISTICS - CML OUTPUT} \ \ V_{CC} = 1.8 \ V \ \pm 5\%, \ V_{CCO1} = 1.2 \ V \ \pm 5\% \ \ \text{or } 1.8 \ V \ \pm 5\%, \ V_{CCO2} = 1.2 \ V \ \pm 5\%$ or 1.8 V  $\pm$ 5%, V<sub>CCO3</sub> = 1.2 V  $\pm$ 5% or 1.8 V  $\pm$ 5%, GND = 0 V, T<sub>A</sub> = -40°C to 85°C (Note 5)

Symbol	Characteristic	Min	Тур	Max	Unit
POWER	SUPPLY CURRENT (Inputs and Outputs open)				
I <sub>CC</sub> I <sub>CCO</sub>	Power Supply Current for V <sub>CC</sub> (Inputs and Outputs Open) Power Supply Current for VCCOx (Inputs and Outputs Open)		75 95	125 105	mA
CML OU	FPUTS (Note 6)		•		
V <sub>OH</sub>	Output HIGH Voltage $ \begin{array}{c} V_{CC} = 1.8 \ \text{V, VCCOx} = 1.8 \ \text{V} \\ V_{CC} = 1.8 \ \text{V, VCCOx} = 1.2 \ \text{V} \\ \end{array} $	V <sub>CCOx</sub> - 40 1760 1160	V <sub>CCOx</sub> - 20 1780 1180	V <sub>CCOx</sub> 1800 1200	mV
V <sub>OL</sub>	Output LOW Voltage $ V_{CC} = 1.8 \text{ V, VCCOx} = 1.8 \text{ V} $ $ V_{CC} = 1.8 \text{ V, VCCOx} = 1.2 \text{ V} $	V <sub>CCOx</sub> – 500 1300 700	V <sub>CCOx</sub> – 400 1400 800	V <sub>CCOx</sub> – 275 1525 925	mV
DIFFERE	NTIAL INPUTS DRIVEN SINGLE-ENDED (Note 7) (Figure 6)				
V <sub>th</sub>	Input Threshold Reference Voltage Range (Note 8)	1050		V <sub>CC</sub> – 100	mV
$V_{IH}$	Single-Ended Input HIGH Voltage	V <sub>th</sub> + 100		V <sub>CC</sub>	mV
$V_{IL}$	Single-Ended Input LOW Voltage	GND		V <sub>th</sub> – 100	mV
$V_{ISE}$	Single-Ended Input Voltage (V <sub>IH</sub> - V <sub>IL</sub> )	200		1200	mV
V <sub>REFAC</sub>					
V <sub>REFAC</sub>	Output Reference Voltage @ 100 μA for Capacitor – Coupled Inputs, Only	V <sub>CC</sub> – 550	V <sub>CC</sub> – 450	V <sub>CC</sub> – 300	mV
DIFFERE	NTIAL INPUTS DRIVEN DIFFERENTIALLY (Note 9) (Figures 4 and	d 7)			
$V_{IHD}$	Differential Input HIGH Voltage (IN, IN)	1100		V <sub>CC</sub>	mV
$V_{ILD}$	Differential Input LOW Voltage (IN, IN)	GND	,	V <sub>CC</sub> - 100	mV
$V_{ID}$	Differential Input Voltage (IN, I I) (V <sub>IH</sub> ) - V <sub>LD</sub> )	100	m	12 C O	mV
V <sub>CMR</sub>	In 11t Gor 1 n 2 1 N loce Range (Liffer en ial Configuration, No e 10) (Figure 9)	050	/	V <sub>2</sub> c - 34	mV
I <sub>IH</sub>	Input HIGH Current IN/IN (VTO / VT1 Open)	-150		150	μΑ
I <sub>IL</sub>	Input LOW Current IN/IN (VTO / VT1 Open)	-150		150	μΑ
CONTRO	L INPUT (SEL Pin)				
V <sub>IH</sub>	Input HIGH Voltage for Control Pin	V <sub>CC</sub> x 0.65		V <sub>CC</sub>	mV
V <sub>IL</sub>	Input LOW Voltage for Control Pin	GND		V <sub>CC</sub> x 0.35	mV
I <sub>IH</sub>	Input HIGH Current	-150	20	+150	μΑ
I <sub>IL</sub>	Input LOW Current	-150	5	+150	μΑ
TERMINA	ATION RESISTORS				
R <sub>TIN</sub>	Internal Input Termination Resistor (Measured from INx to VTx)	45	50	55	Ω
R <sub>TOUT</sub>	Internal Output Termination Resistor	45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 5. Input parameters vary 1:1 with V<sub>CC</sub>. and output parameters vary 1:1 with V<sub>CCOx</sub>.
  6. CML outputs (Qn/Qn) have internal 50 Ω source termination resistors and must be externally terminated with 50 Ω to V<sub>CCOx</sub> for proper operation.
- 7.  $V_{th}$ ,  $V_{lH}$ ,  $V_{lL}$  and  $V_{lSE}$  parameters must be complied with simultaneously. 8.  $V_{th}$  is applied to the complementary input when operating in single–ended mode.
- 9. V<sub>IHD</sub>, V<sub>ILD</sub>, V<sub>ID</sub> and V<sub>CMR</sub> parameters must be complied with simultaneously.

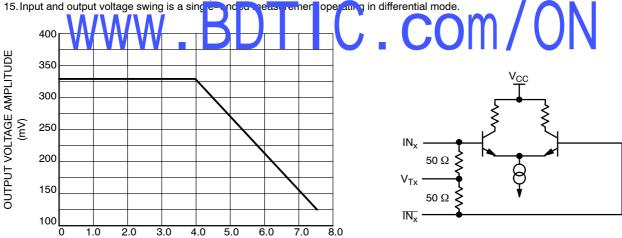
  10. V<sub>CMR</sub> min varies 1:1 with GND, V<sub>CMR</sub> max varies 1:1 with V<sub>CC</sub>. The V<sub>CMR</sub> range is referenced to the most positive side of the differential input signal.

**Table 6. AC CHARACTERISTICS**  $V_{CC} = 1.8 \text{ V} \pm 5\%$ ,  $V_{CCO1} = 1.2 \text{ V} \pm 5\%$  or  $1.8 \text{ V} \pm 5\%$ ,  $V_{CCO2} = 1.2 \text{ V} \pm 5\%$  or  $1.8 \text{ V} \pm 5\%$ , or  $1.8 \text{ V} \pm 5\%$ , GND = 0 V,  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (Note 11)

Symbol	Characteristic	Min	Тур	Max	Unit
f <sub>MAX</sub>	Maximum Input Clock Frequency, V <sub>OUTPP</sub> ≥ 200 mV	4.0	6.0		GHz
f <sub>DATAMAX</sub>	Maximum Operating Input Data Rate (PRBS23)	10			Gbps
V <sub>OUTPP</sub>	Output Voltage Amplitude (See Figures 4, Note 15) $f_{in} \le 4.0 \text{ GHz}$	200	330		mV
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay to Output Differential @ 1 GHz, $IN_x/IN_x$ to $Q_n/\overline{Q_n}$ Measured at Differential Crosspoint SEL to $Q_n$	125 125	175	250 300	ps
t <sub>PLH</sub> TC	Propagation Delay Temperature Coefficient		100		fs/°C
t <sub>SKEW</sub>	Output - Output Skew (Within Device) (Note 12) Device - Device Skew (t <sub>pd</sub> Max - t <sub>pdmin</sub> )			30 50	ps
t <sub>DC</sub>	Output Clock Duty Cycle (Reference Duty Cycle = 50%) $f_{in} \leq 4.0 \text{ GHz}$	45	50	55	%
t <sub>JITTER</sub>	Output Random Jitter (RJ) (Note 13) $ f_{in} \leq 4.0 \text{ GHz} $ Deterministic Jitter (DJ) (Note 14) $ 10 \text{ Gbps} $		0.2	0.8 10	ps rms ps pk-pk
V <sub>INPP</sub>	Input Voltage Swing (Differential Configuration) (Note 15)	100		1200	mV
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Times @ 1 GHz (20% – 80%) Q <sub>n</sub> , Q <sub>n</sub>		50	65	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 11. Measured using a 400 mV source, 50% duty cycle clock source. All outputs must be loaded with external 50 Ω to V<sub>CCOx</sub>. Input edge rates 40 ps (20% 80%).
- 12. Skew is measured between outputs under identical transitions and conditions. Duty cycle skew is defined only for differential operation when the delays are measured from cross-point of the inputs to the crosspoint of the outputs.
- 13. Additive RMS jitter with 50% duty cycle clock signal.
- 14. Additive Peak-to-Peak data dependent jitter with input NRZ data at PRBS23.

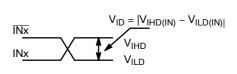


f<sub>out</sub>, CLOCK OUTPUT FREQUENCY (GHz)

Figure 2. Output Voltage Amplitude (V<sub>OUTPP</sub>) vs. Input

Frequency (f<sub>in</sub>) at Ambient Temperature (Typical)

Figure 3. Input Structure



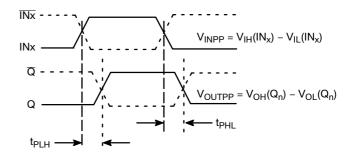
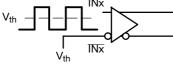
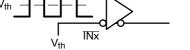


Figure 4. Differential Inputs Driven Differentially

Figure 5. AC Reference Measurement





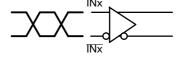


Figure 6. Differential Input Driven Single-Ended

Figure 7. Differential Inputs Driven Differentially

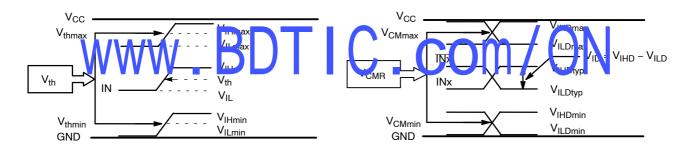


Figure 8. V<sub>th</sub> Diagram

Figure 9. V<sub>CMR</sub> Diagram

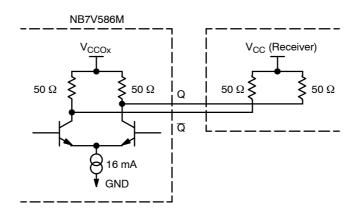


Figure 10. Typical CML Output Structure and Termination

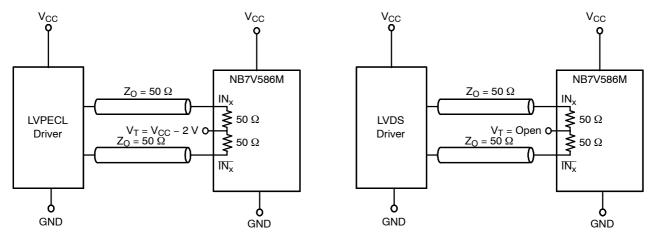


Figure 11. LVPECL Interface

Figure 12. LVDS Interface

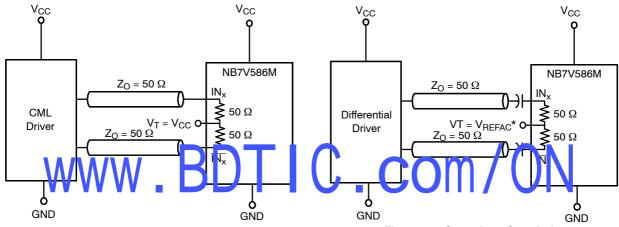


Figure 13. Standard 50  $\Omega$  Load CML Interface

Figure 14. Capacitor–Coupled Differential Interface (V<sub>T</sub> Connected to V<sub>REFAC</sub>)

\*V\_REFAC bypassed to ground with a 0.01  $\mu\text{F}$  capacitor

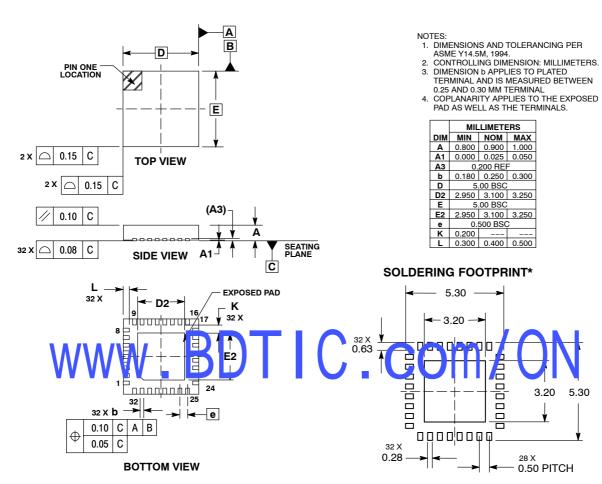
#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NB7V586MMNG	QFN32 (Pb-Free)	74 Units / Rail
NB7V586MMNR4G	QFN32 (Pb-Free)	1000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### PACKAGE DIMENSIONS

#### QFN32 5\*5\*1 0.5 P CASE 488AM-01 ISSUE O



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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