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# FPD200

## GENERAL PURPOSE pHEMT DIE

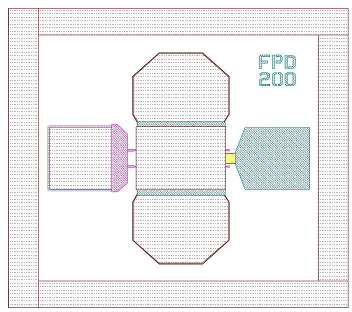
**Package Style: Bare Die**

## Product Description

The FPD200 is an AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT), featuring a 0.25μmx200μm Schottky barrier gate, defined by high-resolution stepper-based photolithography. The recessed gate structure minimizes parasitics to optimize performance. The epitaxial structure and processing have been optimized for reliable high-power applications.

**Optimum Technology Matching® Applied**

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☐ SiGe HBT
- ✓ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ InP HBT
- ☐ RF MEMS
- ☐ LDMOS




## Features

- 19dBm Output $P_{1dB}$
- 13dB Power Gain at 12GHz
- 17dB Maximum Stable Gain at 12GHz
- 12dB Maximum Stable Gain at 18GHz
- 45% Power-Added Efficiency

## Applications

- Narrowband and Broadband High-Performance Amplifiers
- SATCOM Uplink Transmitters
- PCS/Cellular Low-Voltage High-Efficiency Output Amplifiers
- Medium-Haul Digital Radio Transmitters

| Parameter | Specification | | | Unit | Condition |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| $P_{1dB}$ Gain Compression | 18 | 19 | | dBm | $V_{DS}$=5V, $I_{DS}$=50% $I_{DSS}$ |
| Power Gain at $P_{1dB}$ ($G_{1dB}$) | 11.0 | 13.0 | | dB | $V_{DS}$=5V, $I_{DS}$=50% $I_{DSS}$ |
| Noise Figure | | 1.2 | | dB | $V_{DS}$=5V, $I_{DS}$=50% $I_{DSS}$ |
| PAE | | 45 | | % | $V_{DS}$=5V, $I_{DS}$=50% $I_{DSS}$, $P_{OUT}$=$P_{1dB}$ |
| Maximum Stable Gain (S21/S12) | 16 | 17 | | dB | $V_{DS}$=5V, $I_{DS}$=50% $I_{DSS}$, f=12GHz |
| | 10.5 | 12 | | dB | $V_{DS}$=5V, $I_{DS}$=50% $I_{DSS}$, f=24GHz |
| Saturated Drain-Source Current ($I_{DSS}$) | 45 | 60 | 75 | mA | $V_{DS}$=1.3V, $V_{GS}$=0V |
| Maximum Drain-Source Current ($I_{MAX}$) | | 120 | | mA | $V_{DS}$=1.3V, $V_{GS}$≈+1V |
| Transconductance | | 80 | | ms | $V_{DS}$=1.3V, $V_{GS}$=0V |
| Gate-Source Leakage Current ($I_{GSO}$) | | 1 | 10 | μA | $V_{GS}$=-5V |
| Pinch-Off Voltage ($V_P$) | \|0.7\| | \|1.0\| | \|1.3\| | V | $V_{DS}$=1.3V, $I_{DS}$=0.2mA |
| Gate-Source Breakdown Voltage ($V_{BDGS}$) | \|12.0\| | \|14.0\| | | V | $I_{GS}$=0.2mA |
| Gate-Drain Breakdown Voltage ($V_{BDGD}$) | \|14.5\| | \|16.0\| | | V | $I_{GD}$=0.2mA |
| Thermal Resistivity (θJC) | | 280 | | °C/W | $V_{DS}$>3V |

Note: $T_{AMBIENT}$=22°C, RF specifications measured at f=12GHz using CW signal on a sample basis.





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## Absolute Maximum Ratings[1]

| Parameter | Rating | Unit |
|---|---|---|
| Drain-Source Voltage ($V_{DS}$) ($-3V<V_{GS}<-0.5V$)[2] | 8 | V |
| Gate-Source Voltage ($V_{GS}$) ($0V<V_{DS}<+8V$) | -3 | V |
| Drain-Source Current ($I_{DS}$) (For $V_{DS}<2V$) | $I_{DSS}$ | |
| Gate Current ($I_G$) (Forward or reverse current) | 10 | mA |
| RF Input Power ($P_{IN}$) (Under any acceptable bias state) | 20 | dBm |
| Channel Operating Temperature ($T_{CH}$) (Under any acceptable bias state) | 175 | °C |
| Storage Temperature ($T_{STG}$) (Non-Operating Storage) | -65 to 150 | °C |
| Total Power Dissipation ($P_{TOT}$)[3, 4, 5] | 0.5 | W |
| Gain Compression (under any bias conditions) | 5 | dB |
| Simultaneous Combination of Limits[6] (2 or more max. limits) | 80 | % |

Notes:

[1]$T_{AMBIENT}=22°C$ unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device.

[2]Operating at absolute maximum $V_D$ continuously is not recommended. If operation at 8V is considered then $I_{DS}$ must be reduced in order to keep the part within its thermal power dissipation limits. Therefore $V_{GS}$ is restricted to $<-0.5V$.

[3]Total Power Dissipation to be de-rated as follows above 22°C: $P_{TOT}=500mW-(3.6mW/°C)xT_{HS}$, where $T_{HS}$=heatsink or ambient temperature above 22°C.
Example: For a 85°C carrier temperature: $P_{TOT}=500-(3.6mWx(85-22))=.27W$

[4]Total Power Dissipation ($P_{TOT}$) defined as $(P_{DC}+P_{IN})-P_{OUT}$, where $P_{DC}$: DC Bias Power, $P_{IN}$: RF Input Power, $P_{OUT}$: RF Output Power.

[5]Users should avoid exceeding 80% of 2 or more Limits simultaneously.

[6]Thermal Resistivity specification assumes a Au/Sn eutectic die attach onto an Au-plated copper heatsink or rib.

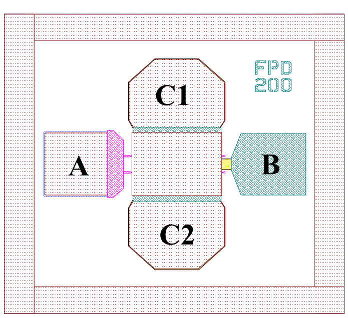
**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).



## Pad Layout




| Pad | Description | Pin Coordinates (μm) |
|---|---|---|
| A | Gate Pad | 90, 200 |
| B | Drain Pad | 320, 200 |
| C1/C2 | Source Pad | 200, 290/110 |

Note: Coordinates are referenced from the bottom left hand corner of the die to the center of the bond pad opening.

| Die Size (μm) | Die Thickness (μm) | Min. Bond Pad Opening (μmxμm) |
|---|---|---|
| 400x400 | 75 | 75x80 |



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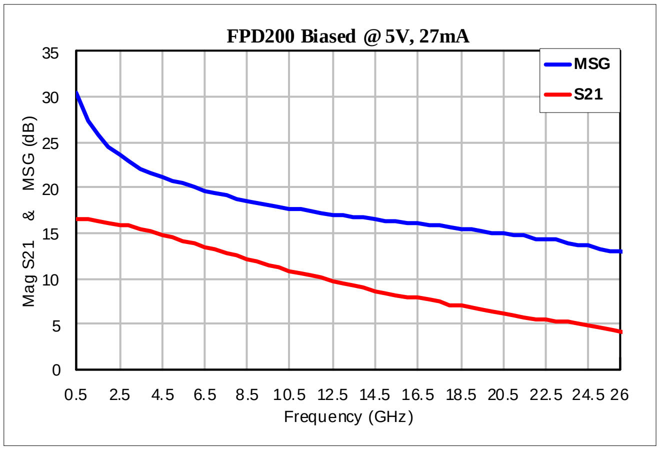
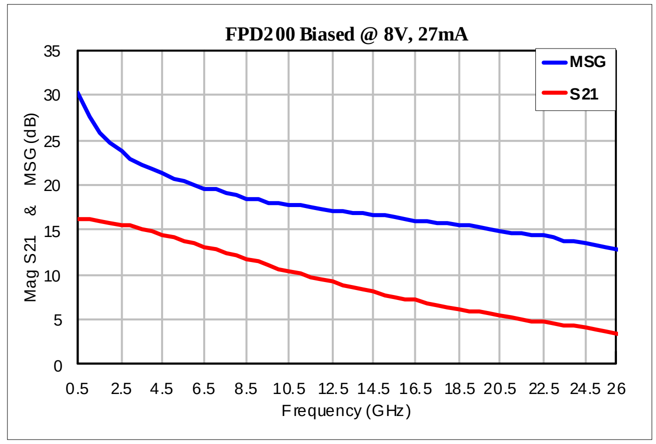
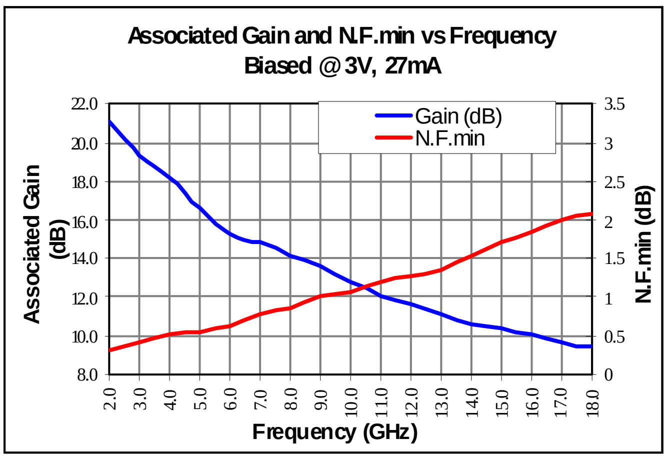
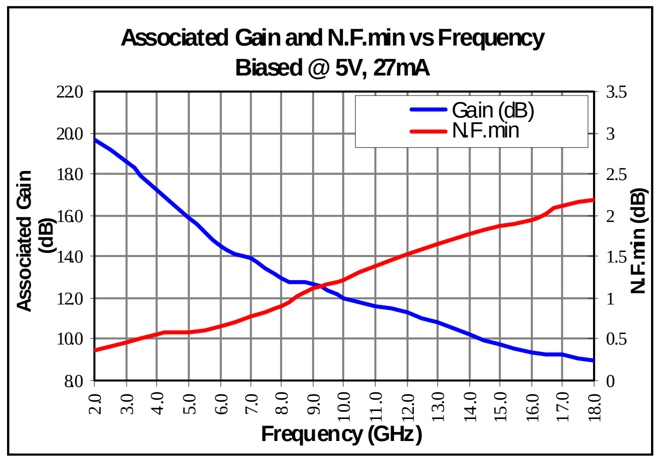
## Typical Measured Performance



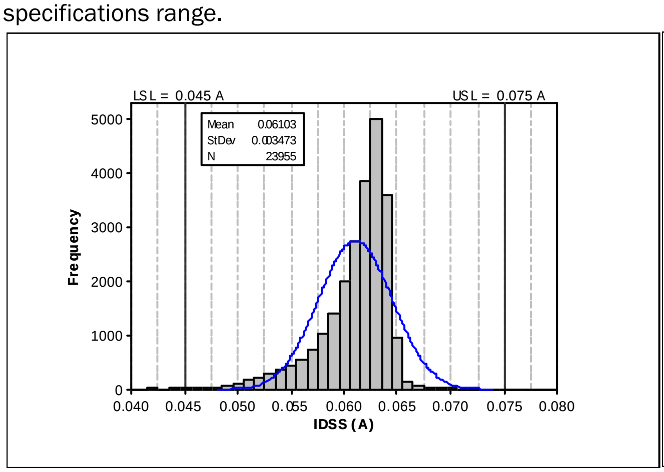



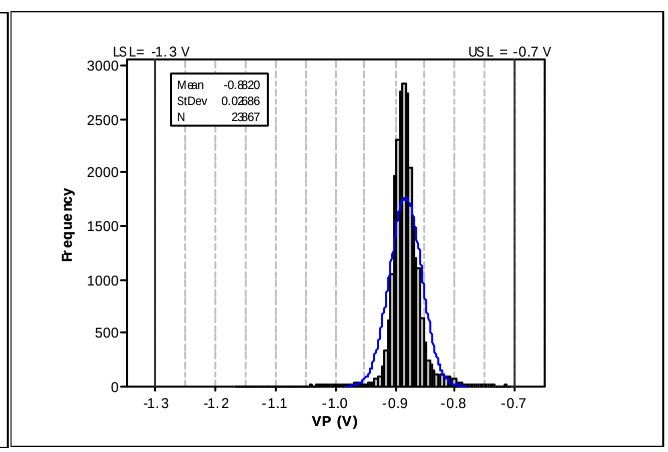




## Typical Wafer Distributions

Note: Data taken from a typical wafer at ambient temperature. Future wafers may have nominal values anywhere within the specifications range.



Noise Parameters (Biased @ $V_{DS}$=3V, $I_{DS}$=27mA)

| Freq | N.F.min | Rn/50 | Gamma Opt. | |
|---|---|---|---|---|
| GHz | dB | Ω | Mag | Angle |
| 2.00 | 0.32 | 0.31 | 0.75 | 6.70 |
| 3.00 | 0.41 | 0.31 | 0.71 | 14.60 |
| 4.00 | 0.52 | 0.29 | 0.74 | 22.60 |
| 5.00 | 0.55 | 0.28 | 0.62 | 27.90 |
| 6.00 | 0.62 | 0.26 | 0.63 | 34.90 |
| 7.00 | 0.78 | 0.26 | 0.54 | 41.50 |
| 8.00 | 0.87 | 0.26 | 0.48 | 47.50 |
| 9.00 | 1.00 | 0.25 | 0.43 | 54.40 |
| 10.00 | 1.08 | 0.24 | 0.41 | 60.20 |
| 11.00 | 1.20 | 0.24 | 0.41 | 65.70 |
| 12.00 | 1.28 | 0.24 | 0.34 | 78.60 |
| 13.00 | 1.37 | 0.24 | 0.28 | 89.70 |
| 14.00 | 1.55 | 0.22 | 0.24 | 95.90 |
| 15.00 | 1.70 | 0.20 | 0.23 | 103.70 |
| 16.00 | 1.85 | 0.20 | 0.24 | 113.50 |
| 17.00 | 1.99 | 0.19 | 0.17 | 137.10 |
| 18.00 | 2.09 | 0.18 | 0.20 | 156.80 |



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## Preferred Assembly Instructions

GaAs devices are fragile and should be handled with great care. Specially designed collets should be used where possible.

The back of the die is metallized and the recommended mounting method is by the use of conductive epoxy. Epoxy should be applied to the attachment surface uniformly and sparingly to avoid encroachment of epoxy on to the top face of the die and ideally should not exceed half the chip height. For automated dispense Ablestick LMISR4 is recommended. For manual dispense Ablestick 84-1 LMI or 84-1 LMIT are recommended. These should be cured at a temperature of 150 °C for 1 hour in an oven especially set aside for epoxy curing only. If possible, the curing oven should be flushed with dry nitrogen. The gold-tin (80% Au 20% Sn) eutectic die attach has a melting point of approximately 280 °C but the absolute temperature being used depends on the leadframe material used and the particular application. The maximum time should be kept to a minimum.

This part has gold (Au) bond pads requiring the use of gold (99.99% pure) bondwire. It is recommended that 25.4 mm diameter gold wire be used. Recommended lead bond technique is thermocompression wedge bonding with 0.001" (25 μm) diameter wire. Bond force, time stage temperature, and ultrasonics are all critical parameters and the settings are dependant on the setup and application being used. Ultrasonic or thermosonic bonding is not recommended.

Bonds should be made from the die first and then to the mounting substrate or package. The physical length of the bondwires should be minimized especially when making RF or ground connections.


## Handling Precautions

To avoid damage to the devices, care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing.

## ESD/MSL Rating

These devices should be treated as Class 0 (0 V to 250 V) as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

## Application Notes and Design Data

Application Notes and design data including S-parameters, noise parameters, and device model are available on request and from www.rfmd.com.

## Reliability

An MTTF of 4.2 million hours at a channel temperature of 150 °C is achieved for the process used to manufacture this device.

## Disclaimers

This product is not designed for use in any space-based or life-sustaining/supporting equipment.

## Ordering Information

| Delivery Quantity | Ordering Code |
|---|---|
| Full Pack (100) | FPD200-000 |
| Small Quantity (25) | FPD200-000SQ |
| Sample Quantity (3) | FPD200-000S3 |


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