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ML4622/4624

FIBER OPTIC DATA QUANTIZER

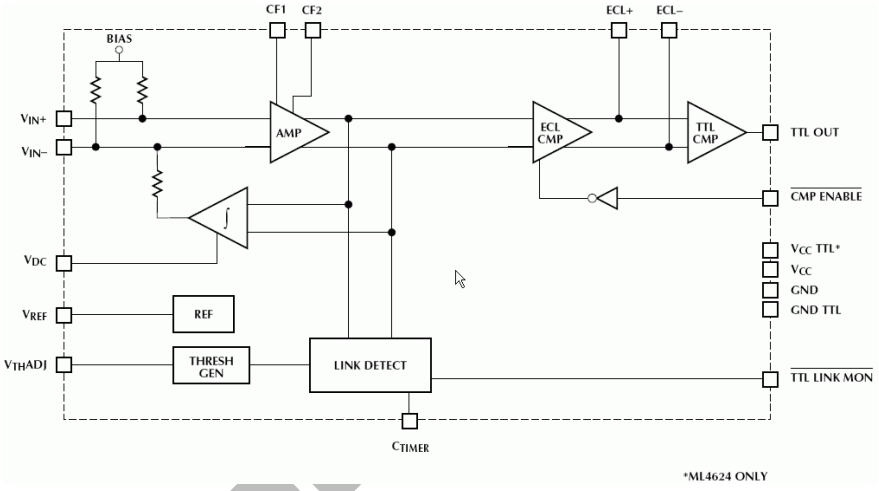
Package: QFN, 16-Pin, 3x3

Features

- Data Rates up to 40MHz or 80MBd
- Can Be Powered by Either +5V Providing TTL or Raised ECL Level Outputs or –5.2V Providing ECL Levels
- Low Noise Design: 25µV RMS Over Bandwidth
- Adjustable Link Monitor Function with Hystersis
- Wide 55dB Input Dynamic Range
- Low Power Design
- ML4624 is Pin Compatible with the ML4621

Applications

- IEEE 802.3 10BASE-FL Receiver
- IEEE 802.5 Fiber Optic Token Ring, 4 and 16mbps
- Fiber Optic Data Communications and Telecommunications Receivers



Functional Block Diagram

Product Description

The ML4622 and ML4624 data quantizers are low noise, wideband, bipolar monolithic ICs designed specifically for signal recovery applications in fiberoptic receiver systems. They contain a wideband limiting amplifier which is capable of accepting an input signal as low as 2mV$_{P-P}$ with a 55dB dynamic range. This high level of sensitivity is achieved by using a DC restoration feedback loop which nulls any offset voltage produced in the limiting amplifier.

The output stage is a high speed comparator circuit with both TTL and ECL outputs. An enable pin is included for added control.

The Link Detect circuit provides a Link Monitor function with a user selectable reference voltage. This circuit monitors the peaks of the input signal and provides a logic level output indicating when the input falls below an acceptable level. This output can be used to disable the quantizer and/or drive an LED, providing a visible link status.

Ordering Information

ML4622CP	Molded DIP (P16), 0 °C to 70 °C
ML4622CS	Molded SOIC (S16N), 0 °C to 70 °C
ML4622IS	Molded SOIC (S16N), -40 °C to 85 °C
ML4624CP	Molded DIP (P24N), 0 °C to 70 °C
ML4624CQ	Molded PCC (Q28), 0 °C to 70 °C

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☒ Si CMOS	☐ RF MEMS
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
V_{CC} - GND	-0.3 to +7.0	V
V_{CC} Total - GND Total	-0.3 to +7.0	V
Inputs/Outputs GND	-0.3 to V_{CC} +0.3	V
Storage Temperature Range	-65 to +150	°C
Lead Temperature (Soldering 10 seconds)	+260	°C

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Electrical Characteristics[2, 3]					Commercial T_A=0 °C to 70 °C, industrial T_A=-40 °C to 85 °C, V_{CC}=5V ± 10%, GND=0V[1]
V_{CC} Supply Current		35	45	mA	GND TTL=V_{CC}, TTL Output Disabled
		55	70	mA	GND TTL=GND, TTL Output Enabled
Reference Voltage	2.40	2.50	2.60	V	
V_{REF} Output Source Current			5	mA	
Amplifier Gain		100		V/V	
Input Signal Range	2		1600	mV_{P-P}	
External Voltage V_{TH}ADJ to Set V_{TH}	0.5		2.6	V	
Input Offset		3		mV	V_{DS}=V_{REF} (DC loop inactive)
Input Referred Noise		25		µV	50MHz Bw
3dB Bandwidth		45		MHz	
Input Resistance	1	1.6	2.5	kΩ	V_{IN+}, V_{IN-}
Input Bias Current of V_{TH}ADJ	-200	10	+200	µA	
Propagation Delay		15		ns	From V_{IN+}, V_{IN-} to TTL Out V_{IN}=10mV_{P-P}
		11		ns	From V_{IN+}, V_{IN-} to ECL+, ECL- V_{IN}=10mV_{P-P}
TTL V_{OH}	2.4			V	V_{CC} TTL=5V, I_{OH}=-50µA
TTL V_{OL}			0.55	V	V_{CC} TTL=5V, I_{OL}=2mA
TTL V_{IH}	2.0			V	
TTL V_{IL}			0.8	V	
TTL I_{IH}	-50		50	µA	V_{IH}=2.4V
TTL I_{IL}	-1.6		0	mA	V_{IH}=0.4V
Input Threshold Voltage ML4622	4	5	6	mV_{P-P}	V_{TH}ADJ=V_{REF}[4]
Input Threshold Voltage ML4624	5	6	7	mV_{P-P}	V_{TH}ADJ=V_{REF}[4]
Hystersis		20		%	
Common Mode Voltage V_{IN+}, V_{IN-}		1.65		V	
Output High Voltage at ECL+, ECL-	V_{CC}-1.06		V_{CC}-0.7 V_{CC}-0.6[5]		With 200Ω load tied to V_{CC}-2V
Output Low Voltage at ECL+, ECL-	V_{CC}-1.89		V_{CC}-1.62 V_{CC}-1.56[5]		With 200Ω load tied to V_{CC}-2V

Notes: 1. Voltages measured with respect to ground unless otherwise specified. 2. Limits guaranteed by 100% testing, sampling, or correlation with worst-cast test conditions. 3. Low duty cycle pulse testing performed at T_A. 4. DC tested: Threshold for switching TTL LINK Mon from High (off) to Low (on). 5. Industrial temperature range specification.

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Function	Description
TTL LINK MON	TTL Link Monitor output. Signal is low when the VIN+, VIN– inputs exceed the minimum threshold, which is set by a voltage on the VTHADJ pin. Signal is high when the input signal level is below the threshold. Capable of driving a 10mA LED indicator. This pin can be tied to CMP ENABLE.
CMP ENABLE	A low voltage at this TTL input pin enables both the ECL and the TTL outputs. A high TTL voltage disables the comparator output with ECL+ high, ECL– low, and TTL OUT high.
VIN-	This input pin should be capacitively coupled to the input source or to filtered ground. (The input resistance is approximately 1.6kΩ.)
VIN+	This input pin should be capacitively coupled to the input source or to filtered ground. (The input resistance is approximately 1.6kΩ.)
ECL-	The ECL comparator negative output. Has internal pull down resistor. External pull downs are not required unless driving a large capacitive load.
ECL+	The ECL comparator positive output. Has internal pull down resistor. External pull downs are not required unless driving a large capacitive load.
GND TTL	The negative supply for the TTL comparator stage. If the TTL output is not necessary, connect GND TTL to VCC.
VCC TTL	The positive supply for the TTL comparator stage. If the TTL output is not necessary, connect VCC TTL to VCC. (ML4624 only)
TTL OUT	TTL data output.
VDC	An external capacitor on this pin integrates an error signal which nulls the offset of the input amplifier. If the DC feedback loop is not being used, this pin should be connected to VREF.
CF2	A capacitor from this pin to CF1 controls the maximum bandwidth of the amplifier.
CF1	Connect to CF2 through a capacitor.
GND	Negative supply. Connect to –5.2V for ECL operation, or to ground for TTL or raised ECL operation.
VTHADJ	This input pin sets the link monitor threshold.
VREF	A 2.5V reference with respect to GND.
CTIMER	A capacitor from this pin to VCC determines the Link Monitor response time.
VCC	Positive supply. Connect to ground for negative ECL operation, or to 5V for TTL or raised ECL operation.

Functional Description

Amplifier

The ML4622, ML4624 have an adjustable Bandwidth limiting amplifier. Maximum sensitivity is achieved through the use of a DC restoration feedback loop and AC coupling the input. When AC coupled, the input DC bias voltage is set by an on-chip network at about 1.7V. These coupling capacitors, in conjunction with the input impedance of the amplifier, establish a high pass filter with a 3dB corner frequency, f_L, at:

(1)

$$f_L = \frac{1}{2\pi 1600C}$$

Since the amplifier has a differential input, two capacitors of equal value are required. If the signal driving the input is single ended, one of the coupling capacitors can be tied to V_{CC} as shown in Figure 2. CF1 and CF2 create a low pass filter with the corner frequency determined by the following equation:

(2)

$$f_H = \frac{1}{2\pi 800(C + 4pF)}$$

The above equation applies when a single capacitor is tied between CF1 and CF2. When using two capacitors of equal value (Cap1 from CF1 to V_{CC}, Cap2 from CF2 to V_{CC}) the value derived for C should be doubled. Although the input is AC coupled, the offset voltage within the amplifier will be present at the amplifier's output. This is represented by V_{OS} in figure 2. In order to reduce this error a DC feedback loop is incorporated. This negative feedback loop nulls the offset voltage, forcing V_{OS} to be zero. Although the capacitor on VDC is non- critical, the pole it creates can effect the stability of the feedback loop. To avoid stability problems, the value of this capacitor should be at least 10 times larger than the input coupling capacitors.

Figure 1. V_{OUT+}, V_{OUT-}, and V_{OS}

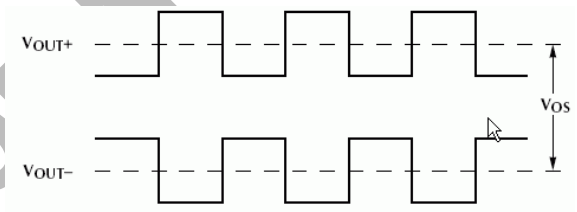

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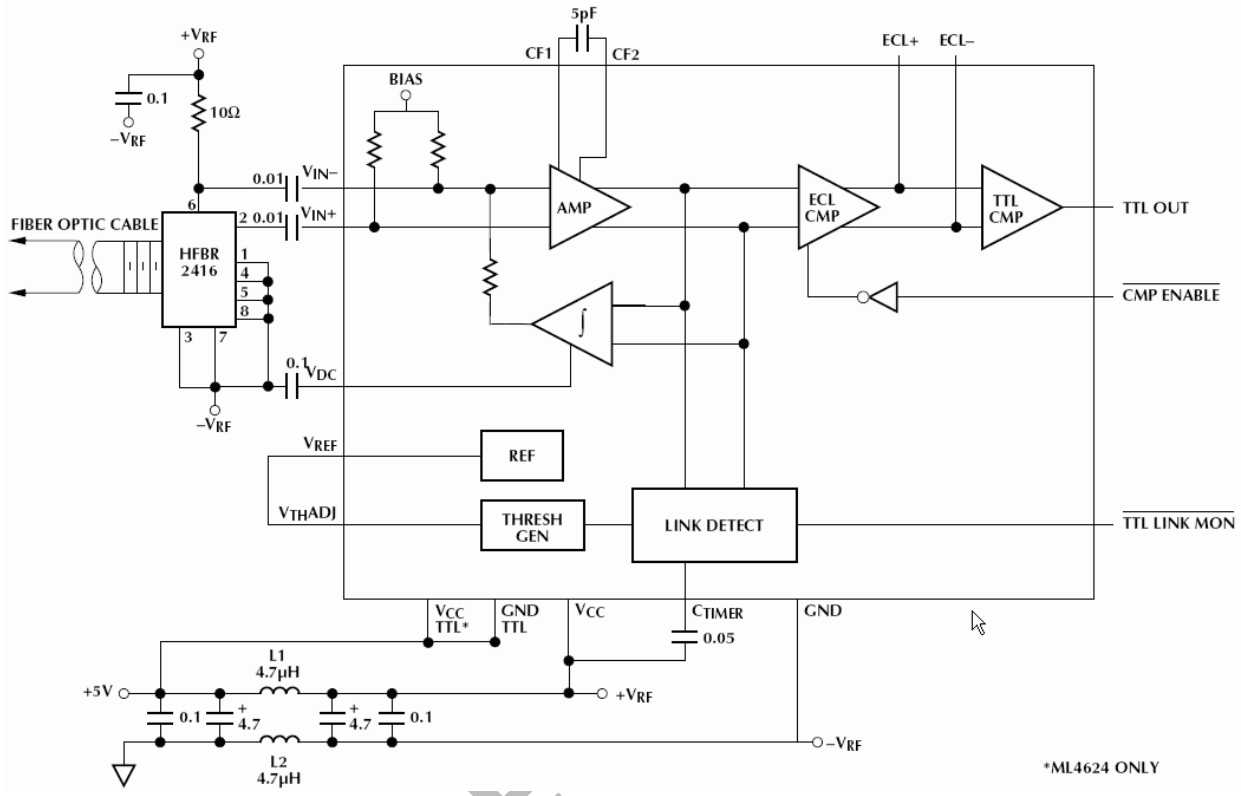
Figure 2. ML4622/4 Configured for 20MHz Bandwidth



Note: If TTL OUT is used, tie GND TTL to unfiltered ground and remove L1. If TTL OUT and ECL outputs are both used, add 3K pulldown resistors at ECL outputs.

Comparator

Two types of comparators are employed in the output section of these Quantizers. The high speed ECL comparator is used to provide the ECL level outputs and in turn drives the TTL comparator. The enable pin, CMP ENABLE, is provided to control the ECL comparator. When CMP ENABLE is low the comparators function normally. When it's high, it forces ECL+ high, ECL– low, and TTL OUT high. The CMP ENABLE pin can be controlled with TTL level signals when the Quantizer is powered by 5V and ground.

Link Detect Circuit

The Link Detect circuit monitors the input signal and provides a status signal indicating when the input falls below a preset voltage level. When the input falls below the preset voltage level, the TTL Link Mon output changes from active (low) to inactive (high). This signal can be fed to the ML4662 10BASE-FL transceiver or a similar type of function to indicate a Low Light Condition. This output can also be used to disable the output data by tying it to the CMP Enable input.

In many fiber optic systems, including Ethernet and Token Ring, a bit error rate is given at a minimum power level. For example, in a 10Base-FL receiver there must be less than 1 x 10–9 bit errors at a receive power level of –32.5dBm average. Designers of these systems must insure that the bit error rate is lower than the specification at the given minimum power level. One procedure to determine the sensitivity of a receiver is to start at the lowest optical power level and gradually increase the optical power until the BER is met. In this case the Link Detect circuit must not disable the receiver (i.e. CMP ENABLE should be tied to Ground). Once the sensitivity of the receiver is determined, the Link Detector circuit can be set just above the power level that meets the BER specification. This way the receiver will shut off before the BER is exceeded.

The ML4622 and ML4624 quantizers have greater Link Detect sensitivity, noise immunity, and accuracy than their predecessor the ML4621. The threshold generator shifts the reference voltage at VTHADJ through a circuit which has a temperature

coefficient matching that of the limiting amplifier. The relationship between the VTHADJ and the VTH (the peak to peak input threshold) is:

(3)

$$V_{TH}ADJ = 417V_{TH}(ML4624)$$

$$V_{TH}ADJ = 500V_{TH}(ML4622)$$

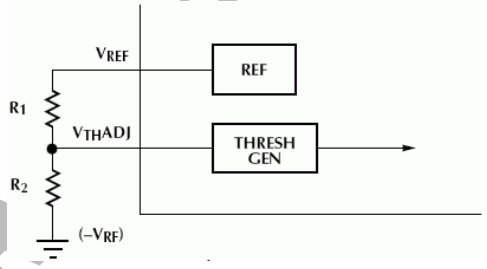
In most cases, including 10Base-FL, 10Base-FB and Token-Ring, VTHADJ can be tied directly to VREF. However if greater sensitivity is required the circuit in figure 3 can be used to adjust the VTHADJ voltage. Even if VREF is tied to VTHADJ, it is a good idea to layout a board with these two resistors available. This will allow potential future adjustments without board revisions. The response time of the Link Detect circuit is set by the CTIMER pin. Starting from the link off state (i.e., TTLÊLINKÊMON is high), the link can be switched on if the input exceeds the set threshold for a time given by:

(4)

$$T = \frac{C_{TIMER} \times 0.7V}{700\mu A}$$

To switch the link from on to off, the above time will be doubled.

Figure 3. ML4622/4 Greater Sensitivity via Two Resistor Layout



Burst Mode

In some fiber optic links, the idle signal is DC, or of a frequency that is substantially different from the data. For these links, a faster response time of the DC loop and the Link Monitor is required. The ML4622 and ML4624 has been designed to accommodate these two requirements. The input coupling capacitors can be relatively small and still maintain stability. With smaller input coupling capacitors and VDC capacitor a faster DC loop response time can be achieved. The Link Monitor is also enhanced to have a faster response time.

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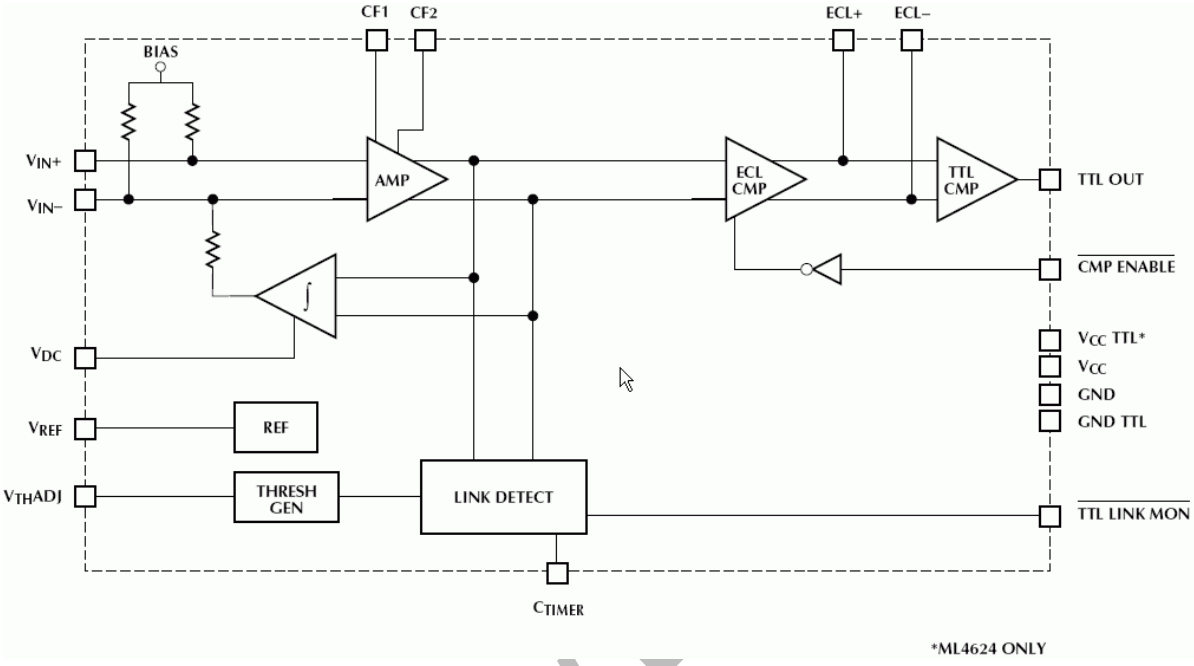
Detailed Functional Block Diagram



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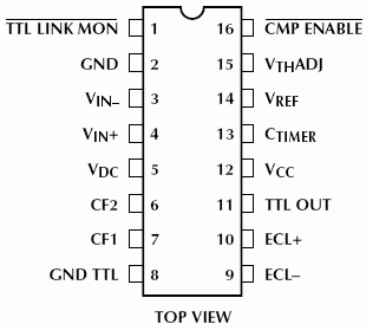
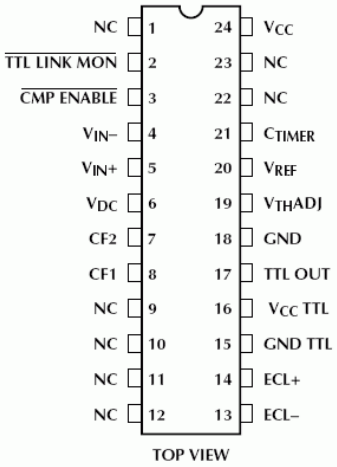
Pin Out

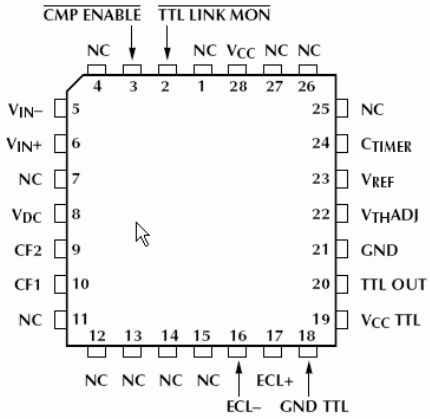
ML4622
16-Pin DIP or
SOIC (Narrow)



ML4624
24-Pin Narrow DIP



ML4624
28-Pin PCC



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