

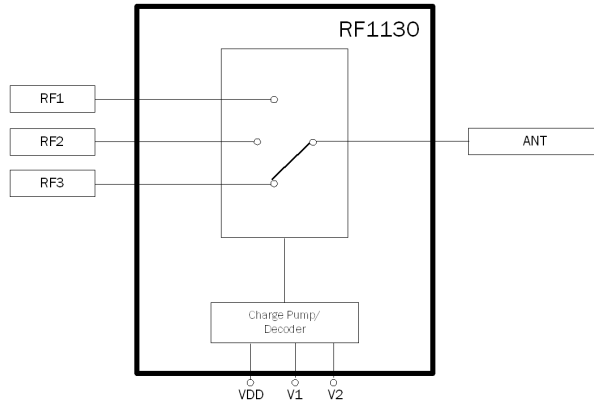


Features

- Low Frequency - 2.5GHz
- Very Low Insertion Loss:
Cell Band: 0.3dB (Typ.)
PCS Band: 0.4dB (Typ.)
- High Isolation
Cell Band: 29.5dB (Typ.)
PCS Band: 21dB (Typ.)
- Compatible With Low Voltage Logic: $V_{HIGH} = 1.8V$
- Excellent Linearity Performance (IIP2):
Cell Band: 114dBm (Typ.)
PCS Band: 115dBm (Typ.)
- Lowest BOM Cost and Small Solution Size: No DC-Blocking Capacitors Required on the RF Paths

Applications

- Antenna Tuning Applications
- IEEE802.11b/g WLAN Applications
- Multi-Mode GSM/WCDMA Handsets
- CDMA Primary Path Handsets



Functional Block Diagram

Product Description

The RF1130 is a single-pole three-throw (SP3T) switch designed for general purpose switching applications which require very low insertion loss and high power handling capability. The RF1130 is ideally suited for battery operated applications requiring high performance switching with very low DC power consumption. The RF1130 features low insertion loss, low control voltage, high linearity, and very good harmonic characteristics. Additionally, RF1130 integrates decoding logic, which allows just two control lines needed for switch control. This part is based off RFMD's GaAs pHEMT and is packaged in a very compact 3.0mmx3.0mmx0.55mm, 16-pin, leadless QFN package.

Ordering Information

- RF1130 Broadband High Power SP3T Switch
- RF1130PCBA-410 Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

- | | | | |
|--------------------------------------|--------------------------------------|------------------------------------------------|-----------------------------------|
| <input type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input checked="" type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS | <input checked="" type="checkbox"/> Si CMOS | <input type="checkbox"/> RF MEMS |
| <input type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si BJT | <input type="checkbox"/> LDMOS |

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Absolute Maximum Ratings

Parameter	Rating	Unit
VDD, V1, V2	6.0	V
Maximum Input Power (0.6GHz to 2.5GHz), RF1, RF2, RF3, ANT	+38	dBm
Operating Temperature	-30 to +85	°C
Storage Temperature	-65 to +100	°C



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Operating Frequency	450		2500	MHz	VDD=2.6V, V1, V2=High=1.8V, V1, V2=Low=0V, Temp=25°C
Insertion Loss					
RF1-ANT, RF2-ANT, RF3-ANT		0.28	0.40	dB	RF ON, 50MHz to 450MHz
		0.30	0.50	dB	RF ON, 824MHz to 960MHz
		0.40	0.60	dB	RF ON, 1850MHz to 1990MHz
		0.50	0.80	dB	RF ON, 2170MHz to 2500MHz
Isolation					
RF1-ANT, RF2-ANT, RF3-ANT	28.0	29.5		dB	RF ON, 824MHz to 960MHz
	20	21		dB	RF ON, 1850MHz to 1990MHz
	19	20		dB	RF ON, 2170MHz to 2500MHz
880MHz Harmonics					
Harmonic (2fo)		-85	-79	dBc	P _{IN} =+35dBm, 880MHz
Third Harmonic (3fo)		-83	-73	dBc	P _{IN} =+35dBm, 880MHz
1800MHz Harmonics					
Harmonic (2fo)		-85	-79	dBc	P _{IN} =+32dBm, 1800MHz
Third Harmonic (3fo)		-83	-73	dBc	P _{IN} =+32dBm, 1800MHz
2500MHz Harmonics					
Harmonic (2fo)		-89	-79	dBc	P _{IN} =+32dBm, 2500MHz
Third Harmonic (3fo)		-81	-73	dBc	P _{IN} =+32dBm, 2500MHz
IIP2					
IIP2 (IMT, PCS, AWS)	107	115		dBm	Tone 1: +26dBm, Tone 2: -20dBm
IIP2 (Cell)	107	114		dBm	Tone 1: +26dBm, 836.5MHz Tone 2: -20dBm, 1718MHz
RF Port Return Loss					
VSWR			1.5:1		

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Input Power at 0.1dB Compression Point					
	37			dBm	
Switching Speed					
		1	5	us	10% to 90% RF, 90% to 10% RF
Triple Beat Ratio					
TBR	81	90		dBc	650 MHz to 900 MHz ^{1, 2}
TBR	81	95		dBc	AWS ^{1, 2}
TBR	81	85		dBc	PCS ^{1, 2}
DC Supply					
V _{DD} (Switch Supply)	2.5	2.6	3.3	V	
V1 and V2 (H)	1.3	1.8	2.9	V	
V1 and V2 (L)	0		0.4	V	
Control Current			1.5	μA	
Supply Current			1	mA	P _{IN} =26 dBm

Notes: Parameters hold at 25 °C and VDD=2.5V
 1. Tested under load with VSWR of 2:1 at all phases
 2. Temp= +15 °C to +60 °C

Switch Control Settings

The switch is operable in three states (see truth table below). The switch is designed for two modes: Active and Stand-by. These modes are controlled by the VDD signal. When VDD is high, the switch is active.

Signal Paths	Control Signals					
Mode	V1	V2	S1	S2	S3	
ANT - RF1	Low	Low	ON	OFF	OFF	
ANT - RF2	High	Low	OFF	ON	OFF	
ANT - RF3	Low	High	OFF	OFF	ON	
INVALID STATE	High	High	Intermediate State*			

*Note: In an indeterminate state, all paths are on with degraded performance.

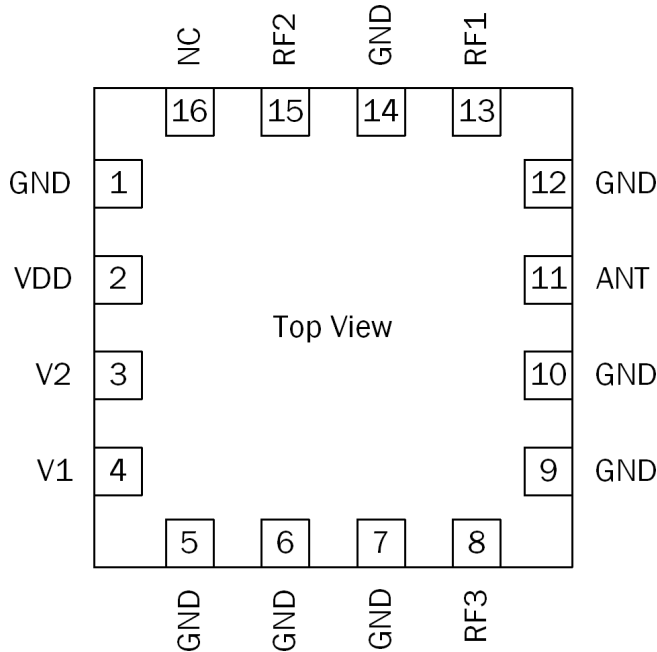
Electrical Test Methods:

The electrical parameters for the switch were measured on the test evaluation board provided by the switch supplier. The test evaluation board includes means for decoupling RF signals from the control signal port (shunt capacitor at control signal ports).

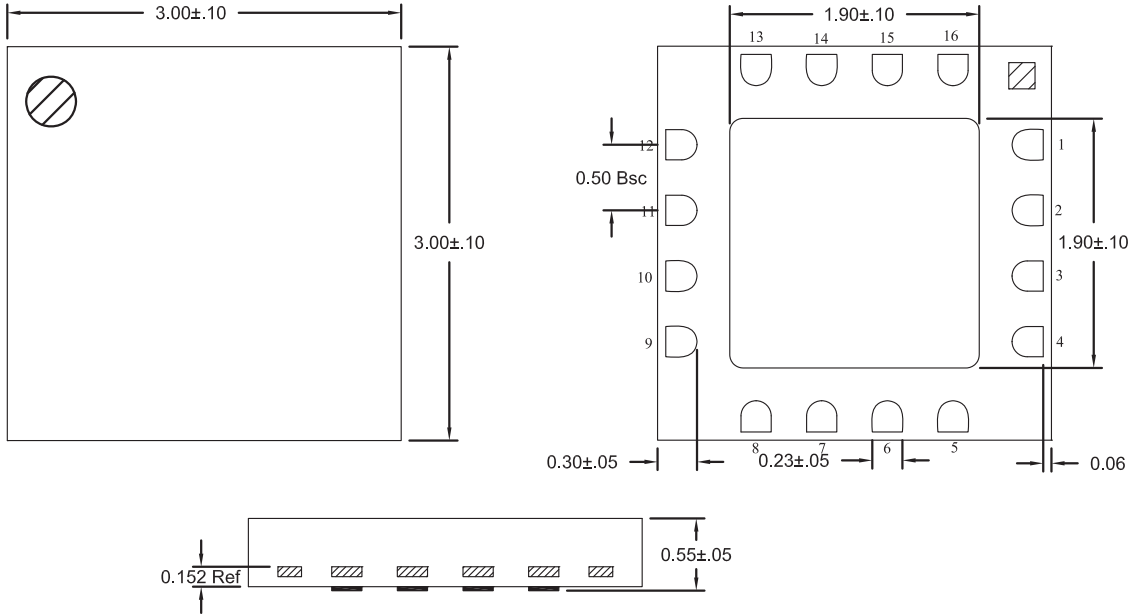
All measurements were done with the calibration plane at switch pins. The effect of the test board losses and phase delay has been removed from the results.

Pin	Function	Description
1	GND	Can be left floating or grounded.
2	VDD	Supply.
3	V2	Control Signal 2.
4	V1	Control Signal 1.
5	GND	Ground.
6	GND	Ground.
7	GND	Ground.
8	RF3	RF output 3.
9	GND	Ground.
10	GND	Ground.
11	ANT	RF input. Connected to antenna.
12	GND	Ground.
13	RF1	RF output 1.
14	GND	Ground.
15	RF2	RF output 2.
16	NC	Can be left floating or grounded.

Pin Configuration

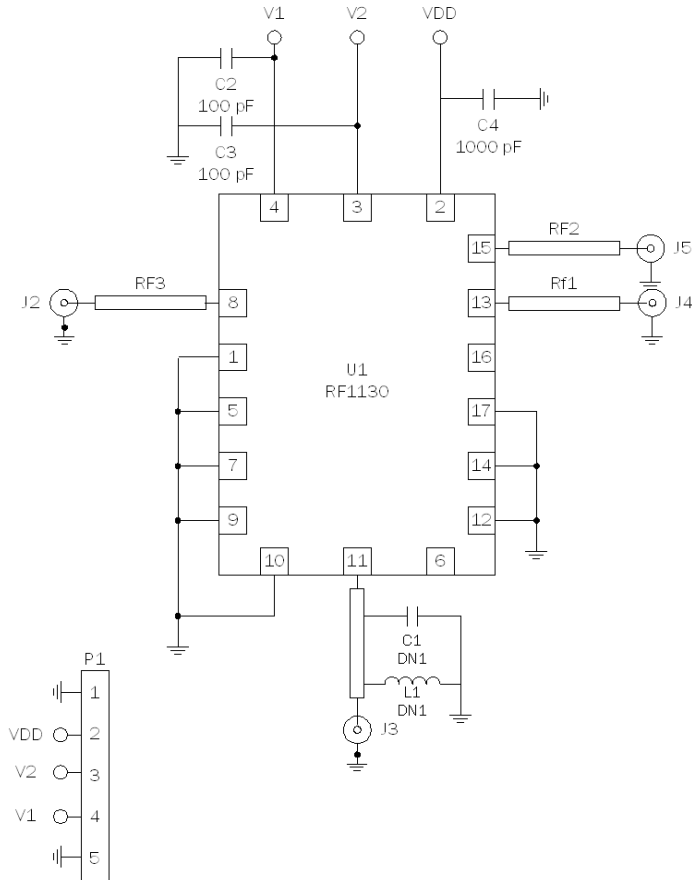


Package Outline



NOTES:
1) PIN 1 SHADED AREA

Evaluation Board Schematic



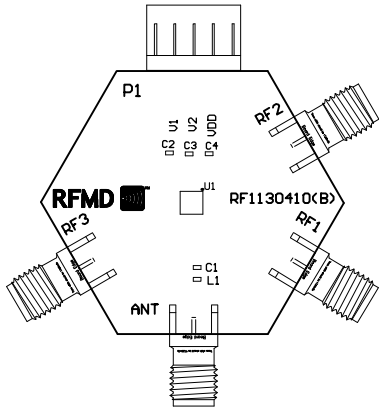
Application Diagram and Guidelines:

The decoupling capacitors are an optional taken and, if necessary, may be used for noise reduction. Decoupling capacitors on the control pins protect the control circuitry from possible RF leakage. DC-blocking capacitors are not needed on the RF paths, as there is no DC on the RF path, however, care should be taken to ensure that DC is not injected in the switch from external circuitry. An ESD filter is needed to protect the switch from antenna ESD events. The filter is formed by LESD inductor and CESD capacitor. The switch has a supply input to feed the built-in logic decoding.

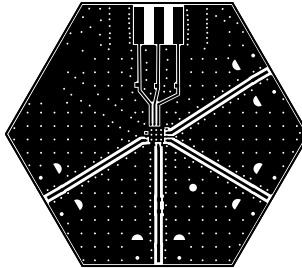
LESD value will depend on the level of ESD protection and the loss acceptable in a given application.

Evaluation Board Layout
Board Thickness 0.0658", Board Material FR-4

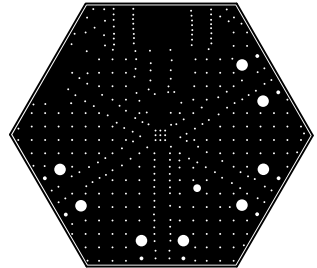
Component Layer



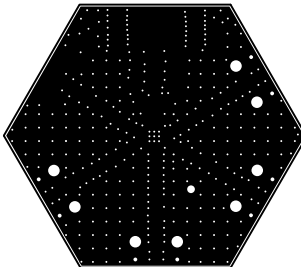
Topside RF Layer



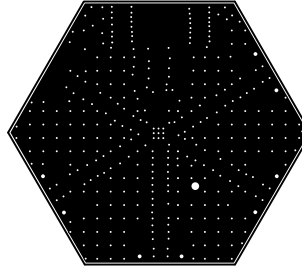
Inner Layer 1



Inner Layer 2



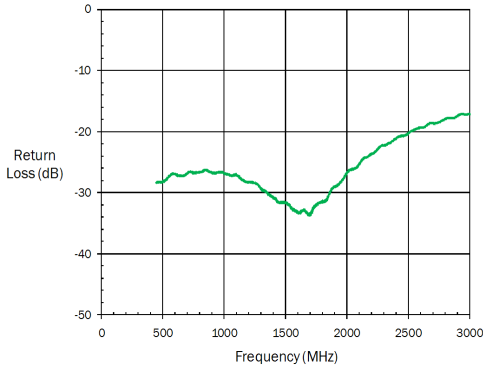
Ground Plane Layer



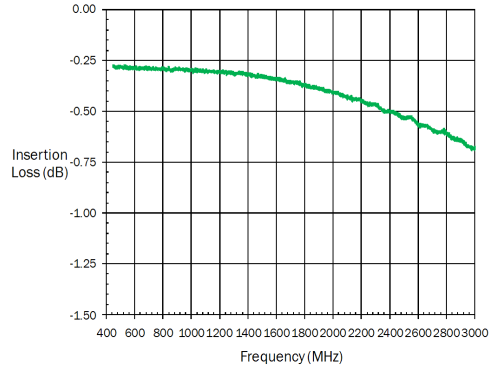
Typical Performance Data on Evaluation Board:

Fixture losses have been de-embedded (Temp = 25 °C, VDD=2.6V, V1=V2=High = 1.8V, V1=V2=0V)

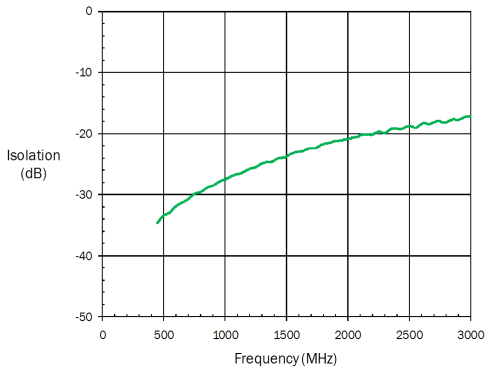
Ant Port Return Loss
(Temp=25 °C, V_{DD}=2.6V)



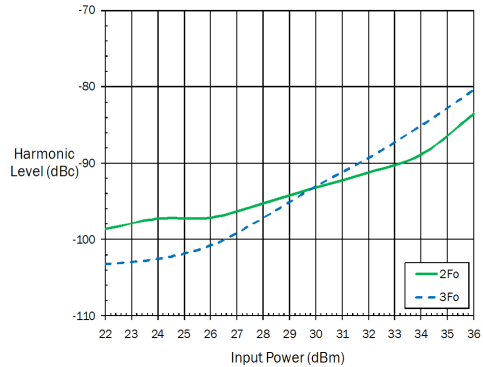
Insertion Loss
(Temp=25 °C, V_{DD}=2.6V)



Antenna to Port Isolation
(Temp=25 °C, V_{DD}=2.6V)



Harmonics
(Temp=25 °C, V_{DD}=2.6V)



Output Power versus Input Power
(Temperature=25 °C, Frequency=1880MHz, V_{DD}=2.6V)

