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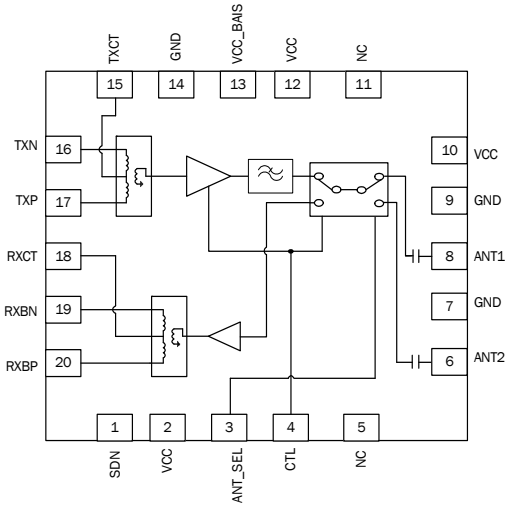
RF6535

3.0V TO 4.2V, 2.4GHz FRONT END MODULE

Package Style: QFN, 20-Pin, 3.5mmx3.5mmx0.5mm



Functional Block Diagram

Features

- TX Output Power: 23dBm
- TX Gain: 28dB
- RX Gain: 11.5dB
- RX NF: 3dB
- Integrated LNA

Applications

- ZigBee® 802.15.4 Based Systems for Remote Monitoring and Control
- WiFi 802.11b/g
- 2.4GHz ISM band applications
- Smart Meters for Energy Management

Product Description

The RF6535 integrates a complete solution in a single Front End Module (FEM) for WiFi and ZigBee® applications in the 2.4GHz to 2.5GHz band. This FEM integrates the PA plus harmonic filter in the transmit path and an LNA in the receive side. It also integrates a diversity switch and provides balanced input and output signals for both the TX and RX paths respectively.

The RF6535 FEM is ideal for ZigBee® systems operating with a minimum output power of 20dBm and high efficiency requirements. On the receive path, the LNA provides 11.5dB of typical gain with only 8mA of current and excellent NF down to 3dB. This FEM meets or exceeds the system requirements for WiFi and ZigBee® applications operating in the 2.4GHz to 2.5GHz band. The device is provided in a 3.5mm x 3.5mm x 0.5mm, 20-pin QFN package.

Ordering Information

RF6535SQ	Standard 25 piece bag
RF6535SR	Standard 100 piece reel
RF6535TR13	Standard 2500 piece reel
RF6535PCK-410	Fully assembled evaluation board and 5 loose pieces

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☑ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
DC Supply Voltage	5	V
Operating Case Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
ESD Human Body Model RF Pins	500	V
ESD Human Body Model All Other Pins	500	V
ESD Charge Device Model All Pins	500	V
Moisture Sensitivity Level	MSL 2	
Maximum Input Power to PA	+5	dBm
Maximum Input Power to LNA	+10	dBm

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					Specifications must be met across supply voltage, control voltage, and temperature ranges unless otherwise noted. Typical conditions: T=25°C, V_{CC}=3.3V, CTL=High
Operating Frequency Range	2400		2483	MHz	
Operating Voltage (V_{CC})	3.0	3.3	4.2	V	
Operating Voltage (V_{CC_BIAS})	3	3.3	4.2	V	
Leakage Current		45	60	uA	V_{CC}=3.3V, RF=OFF, CTL=Low
Transmit Parameters					
Frequency	2400		2483	MHz	
Input Return Loss	9				
Balanced Input Impedance		200		Ω	
Amplitude Imbalance	-1		1	dB	
Phase Imbalance	-15		15	deg	
Output Return Loss	10				
Gain	24	28		dB	At rated power
Gain Flatness	-0.8		0.8	dB	
Rated Output Power		23		dBm	V_{CC}=3.3, T = 25°C
	22			dBm	V_{CC} greater than or equal to 3.3V; Temperature less than or equal to 70°C
	21			dBm	All conditions
Supply current		240	260	mA	P_O=23dBm 802.15.4 OQPSK
Supply current		230	250	mA	P_O=22dBm 802.15.4 OQPSK
Supply current		220	240	mA	PO=21dBm, All conditions
Thermal Resistance		55		°C/W	V_{CC} = 3.6V, P_{OUT} = 23dBm, T_{REF} = 85°C
2nd through 5th harmonic level		-45	-42	dBm/MHz	Measured using standard 802.15.4 OQPSK modulation signal
VSWR Stability and load mismatch susceptibility	4:1				
VSWR No damage	8:1				
Gain settling time		1	10	uS	

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Transmit Parameters, cont.					
Current sourced through TXCT pin			18.0	mA	
Voltage drop from TXCT pin to TXP/TXN			0.1	V	
Receive Parameters					
Frequency	2400		2483	MHz	
Gain	9.5	11.5	13.5	dB	From antenna to RX pin (entire RX path).
Noise Figure		3	4	dB	From antenna to RX pin (entire RX path).
Current		8	11	mA	LNA + Switches
Input IP3		7		dBm	
Gain flatness	-0.5		0.5	dB	
Input return loss	6	8.5		dB	
Output return loss	7.5			dB	
Balanced Output Impedance		200		Ω	
Amplitude imbalance	-1		1	dB	
Phase imbalance	-15		15	deg	
Current sourced through RXCT pin			1	mA	
Voltage drop from RXCT pin to RXP/RXN			0.1	V	
Antenna Switch					
RF-to-Control Isolation	50			dB	Measured at any control pin while in TX or RX mode.
RF-to-ANT Isolation	17	20		dB	Measured from Antenna to RX port while in Transmit mode. Measured from Antenna to TX port while in Receive mode.
RF-to-RF Isolation	18	20		dB	Measured from TX port to RX port while in receive or transmit modes.
Antenna Select Switch Speed			1	uS	ANT1 or ANT2 path, TX or RX mode
Control Logic					
Control Logic = HIGH	$=V_{CC}$-0.3		$=V_{CC}$	V	SDN and ANT_SEL
Control Logic = HIGH	1.7	1.8	3.6	V	CTL
Control Logic = LOW		0	0.2	V	All Logic I/O's
Control Current. Logic HIGH		10		µA	All Logic I/O's
Control Current. Logic LOW		0.1		µA	All Logic I/O's

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Pin	Function	Description
1	SDN	Enable/Shutdown pin for entire module. See logic table for operation.
2	VCC	Voltage Supply. An external 1uF capacitor might be needed for low frequency decoupling.
3	ANT_SEL	Control pin for Antenna select. See logic table for operation.
4	CTL	Enable voltage pin for both PA/Transmit Switch and LNA/Receive Switch. See logic table for operation.
5	NC	No connect pin. Must be left floating.
6	ANT2	This is the common port (antenna). It is matched to 50Ω and DC-block is provided internally.
7	GND	Ground.
8	ANT1	This is the common port (antenna). It is matched to 50Ω and DC-block is provided internally
9	GND	Ground.
10	VCC	Voltage Supply. An external 1uF capacitor might be needed for low frequency decoupling
11	NC	No connect pin. Must be left floating.
12	VCC	Voltage Supply. An external 1uF capacitor might be needed for low frequency decoupling
13	VCC_BIAS	Voltage Supply. An external 1 uF capacitor might be needed for low frequency decoupling
14	GND	Ground.
15	TXCT	Center tap for pass-thru DC voltage to TXN and TXP pins that connect to the TXVR SOIC.
16	TXN	100Ω single ended, 200Ω differential.
17	TXP	100Ω single ended, 200Ω differential.
18	RXCT	Center tap for pass-thru DC voltage to RXBN and RXBP pins that connect to the TXVR SOIC.
19	RXBN	100Ω single ended, 200Ω differential.
20	RXBP	100Ω single ended, 200Ω differential.

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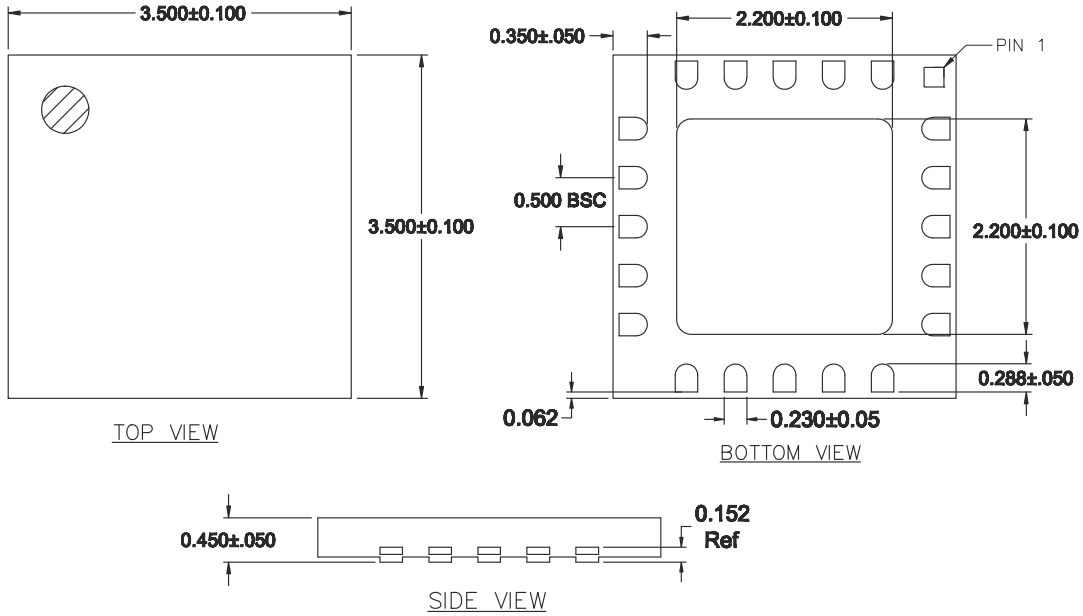
Package Drawing



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RF6535 Biasing Instructions

TX Mode

- With the RF source disabled, apply 3.3V to V_{CC} with other controls set to 0V
- Apply 3.0V to SDN and 1.8V to CTL
- Apply 0V to ANT_SEL to select the ANT1 port, or 3.0V to select the ANT2 port
- Vcc current should rise to 70mA to 80mA quiescent current
- Enable the RF source; Vcc current should rise to a maximum of 200mA depending on output power

RX Mode

- With the RF source disabled, apply 3.3V to V_{CC} with other controls set to 0V
- Apply 3.0V to SDN, keeping CTL at 0V
- Apply 0V to ANT_SEL to select the ANT1 port, or 3.0V to select the ANT2 port
- Vcc current should rise to 7mA to 8mA
- Enable the RF source; V_{CC} current may increase a few mA depending on output power

	Logic Table		
Mode	**SDN**	**CTL**	**ANT_SEL**
TX-ANT1	3.0V	1.8V	0V
TX_ANT2	3.0V	1.8V	3.0V
RX-ANT1	3.0V	0	0V
RX-ANT1	3.0V	0	3.0V
All OFF	0	0	0

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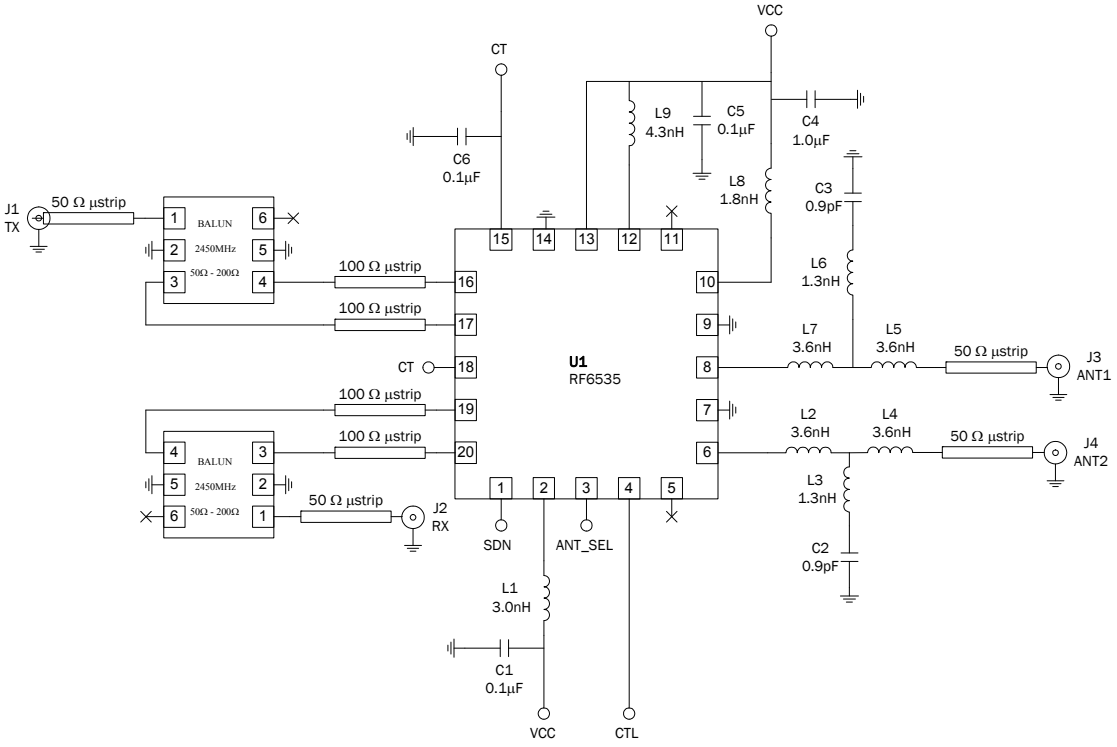
Evaluation Board Schematic



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PCB Design Requirements

PCB Surface Finish

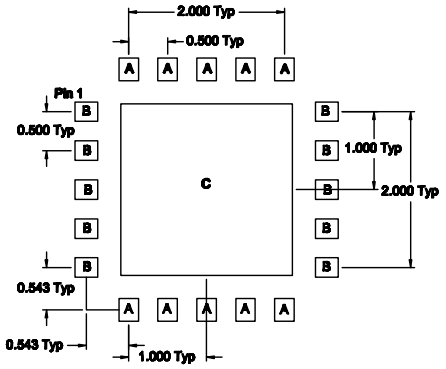
The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3µinch to 8µinch gold over 180µinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

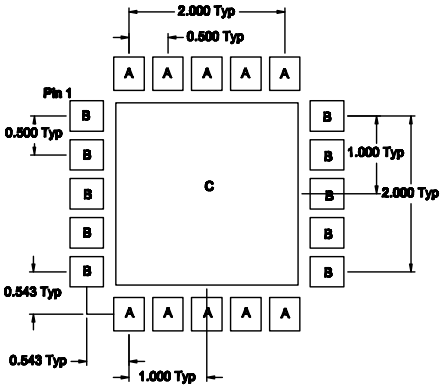
PCB Metal Land and Solder Mask Pattern

A = 0.250 x 0.290 (mm) Typ Rounded Rectangle 50%
B = 0.290 x 0.250 (mm) Typ Rounded Rectangle 50%
C = 2.200 (mm) Sq Rounded Rectangle 5%



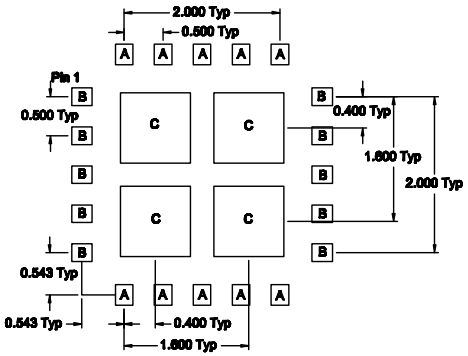
PCB METAL LAND PATTERN

A = 0.390 x 0.430 (mm) Typ Rounded Rectangle 50%
B = 0.430 x 0.390 (mm) Typ Rounded Rectangle 50%
C = 2.340 (mm) Sq Rounded Rectangle 5%



PCB SOLDER MASK PATTERN

A = 0.225 x 0.261 (mm) Typ Rounded Rectangle 10%
B = 0.261 x 0.225 (mm) Typ Rounded Rectangle 10%
C = 0.900 (mm) Sq Typ Rounded Rectangle 10%



PCB STENCIL PATTERN

Thermal vias for center slug “C” should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, the power dissipation, and this electrical requirements. Example of the number and size of vias can be found on the RFMD evaluation board layout.

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